INTRODUCTION — CONTENTS

ALPHA NUMERIC INDEX 1

LEAD TAPE PACKAGING 2

POWER TRANSISTORS 3

SMALL SIGNAL BIPOLAR TRANSISTORS 4

FIELD EFFECT TRANSISTORS 5

THYRISTORS AND TRIGGER DEVICES 6

DIODES AND BRIDGES 7

OPTO DEVICES 8

EUROPEAN HOME ELECTRONICS Data Book

DISCRETE DEVICES

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INTRODUCTION

Since the publication of the Motorola Consumer Selection in 1977, the influence of electronics on the consumer has become more comprehensive and pervasive than anyone could have believed at that time.

Thus, for the sake of clarity, a certain amount of re-arrangement has been found desirable. Re-nemed European Home Electronics Data Book, the 1981—1982 edition encompasses all those applications found within the home: entertainment, appliances, tools, toys, etc.

To facilitate access whilst maintaining as large a selection as possible, the European Home Electronics Data Book is published in two volumes:

- DISCRETE DEVICES
- INTEGRATED CIRCUITS

As in the previous edition, this volume — DISCRETE DEVICES — has data set out by product group whilst an alpha-numeric index in Section 1 lists all devices recommended for use in home electronics. A synoptic table precedes each product section and lists major parameters and functions of the devices in that section.

The increasing number of new devices facing the designer makes the task of selection extremely difficult and time-consuming. We believe the arrangement of the Motorola Home Electronics Data Book will help alleviate this problem.

Naturally, the devices listed in this Data Book represent only a small part of the Motorola product range and in the event that you are unable to find the device to suit your particular application, please consult the comprehensive Motorola Data Library or your nearest Motorola Sales Office. A list of Motorola Sales Offices and Franchised Distributors is to be found in the final section of this volume.

Contents

SECTION 1 – ALPHA NUMERIC INDEX
- Index to devices contained within this volume

SECTION 2 – LEAD TAPE PACKAGING
- Lead tape packaging for axial lead components.

SECTION 3 – POWER TRANSISTORS
- Silicon power plastic.
- Silicon power metal.
- Uniwatt and Duowatt.
- Power MOS

SECTION 4 – SMALL SIGNAL BIPOLAR TRANSISTORS
- Metal and plastic encapsulated transistors for general purpose applications and for applications requiring:
  - low noise/high H_{FE} linearity;
  - high frequency;
  - high voltage;
  - high current.

SECTION 5 – FIELD EFFECT TRANSISTORS
- Metal and plastic encapsulated transistors for general purpose, switching and RF applications.

SECTION 6 – THYRISTORS AND TRIGGER DEVICES
- SCR's and Triacs.
- Unijunction and Programmable Unijunction transistors

SECTION 7 – DIODES AND BRIDGES
- Rectifier diodes:
  - soft, standard, fast, hot carrier, bridges, high voltage
- Reference diodes:
  - zener, voltage regulators for tuning diodes
- Variable capacitance tuning diodes.
- Hot carrier diodes.

SECTION 8 – OPTO DEVICES
- Opto couplers.
- IR emitting diodes.
- Photodarlingtons.
- Phototransistors.

SECTION 1
ALPHA NUMERIC INDEX

- **Index to devices contained within this volume**

Table of Contents

Device Number	Function	Page
BA157	Rectifier Diode	7-4
BA158	Rectifier Diode	7-4
BA159	Rectifier Diode	7-4
BB109	Voltage Variable Capacitance Diode	7-10
BC237	NPN Silicon Amplifier Transistor	4-3
BC238	NPN Silicon Amplifier Transistor	4-3
BC239	NPN Silicon Amplifier Transistor	4-3
BC307	PNP Silicon Amplifier Transistor	4-7
BC308	PNP Silicon Amplifier Transistor	4-7
BC309	PNP Silicon Amplifier Transistor	4-7
BC227	PNP Silicon Amplifier Transistor	4-11
BC238	PNP Silicon Amplifier Transistor	4-11
BC337	NPN Silicon Amplifier Transistor	4-14
BC338	NPN Silicon Amplifier Transistor	4-14
BC372	NPN Silicon Darlington Transistor	4-17
BC373	NPN Silicon Darlington Transistor	4-17
BC413	NPN Silicon Low Noise Transistor	4-20
BC414	NPN Silicon Low Noise Transistor	4-20
BC415	PNP Silicon Low Noise Transistor	4-27
BC416	PNP Silicon Low Noise Transistor	4-27
BC445	NPN Silicon High Voltage Transistor	4-34
BC446	PNP Silicon High Voltage Transistor	4-38
BC447	NPN Silicon High Voltage Transistor	4-34
BC448	PNP Silicon Voltage Transistor	4-38
BC449	NPN Silicon High Voltage Transistor	4-34
BC450	PNP Silicon High Voltage Transistor	4-38
BC485	NPN Silicon High Voltage Current Transistor	4-42
BC486	PNP Silicon High Voltage Current Transistor	4-46
BC487	NPN Silicon High Voltage Current Transistor	4-42
BC488	PNP Silicon High Voltage Current Transistor	4-46
BC489	NPN Silicon High Voltage Current Transistor	4-42
BC490	PNP Silicon High Voltage Current Transistor	4-46
BC546	NPN Silicon Amplifier Transistor	4-50
BC547	NPN Silicon Amplifier Transistor	4-50
BC548	NPN Silicon Amplifier Transistor	4-50
BC549	NPN Silicon Amplifier Transistor	4-56
BC550	NPN Silicon Amplifier Transistor	4-56
BC556	PNP Silicon Amplifier Transistor	4-63
BC557	PNP Silicon Amplifier Transistor	4-63
BC558	PNP Silicon Amplifier Transistor	4-63
BC559	PNP Silicon Low Noise Transistor	4-69
BC560	PNP Silicon Low Noise Transistor	4-69
BC650	NPN Silicon Low Noise Transistor	4-76
BC650,S	NPN Silicon Low Noise Transistor	4-76
BC651	NPN Silicon Low Noise Transistor	4-76
BC651,S	NPN Silicon Low Noise Transistor	4-76
BD135	NPN Silicon Power Transistor	3-4
BD136	PNP Silicon Power Transistor	3-6
BD137	NPN Silicon Power Transistor	3-4
BD138	PNP Silicon Power Transistor	3-6
BD139	NPN Silicon Power Transistor	3-4
BD140	PNP Silicon Power Transistor	3-6
BD165	NPN Silicon Power Transistor	3-8
BD166	PNP Silicon Power Transistor	3-10
BD167	NPN Silicon Power Transistor	3-8
BD168	PNP Silicon Power Transistor	3-10
BD169	NPN Silicon Power Transistor	3-8
BD170	PNP Silicon Power Transistor	3-10
BD175	NPN Silicon Power Transistor	3-12
BD176	PNP Silicon Power Transistor	3-14
BD177	NPN Silicon Power Transistor	3-12
BD178	PNP Silicon Power Transistor	3-14
BD179	NPN Silicon Power Transistor	3-12
BD180	PNP Silicon Power Transistor	3-14

TABLE OF CONTENTS (continued)

Device Number	Function	Page
BD185	NPN Silicon Power Transistor	3-16
BD186	PNP Silicon Power Transistor	3-18
BD187	NPN Silicon Power Transistor	3-16
BD188	PNP Silicon Power Transistor	3-18
BD189	NPN Silicon Power Transistor	3-16
BD190	PNP Silicon Power Transistor	3-18
BD232	NPN Silicon Power Transistor	3-20
BD233	NPN Silicon Power Transistor	3-22
BD234	PNP Silicon Power Transistor	3-24
BD235	NPN Silicon Power Transistor	3-22
BD236	PNP Silicon Power Transistor	3-24
BD237	NPN Silicon Power Transistor	3-22
BD238	PNP Silicon Power Transistor	3-24
BD239	NPN Silicon Power Transistor	3-26
BD240	PNP Silicon Power Transistor	3-26
BD241	NPN Silicon Power Transistor	3-28
BD242	PNP Silicon Power Transistor	3-28
BD243	NPN Silicon Power Transistor	3-32
BD243A	NPN Silicon Power Transistor	3-32
BD243B	NPN Silicon Power Transistor	3-32
BD243C	NPN Silicon Power Transistor	3-32
BD244	PNP Silicon Power Transistor	3-32
BD244A	PNP Silicon Power Transistor	3-32
BD244B	PNP Silicon Power Transistor	3-32
BD244C	PNP Silicon Power Transistor	3-32
BD311	NPN Silicon Power Transistor	3-36
BD312	PNP Silicon Power Transistor	3-36
BD313	NPN Silicon Power Transistor	3-39
BD314	PNP Silicon Power Transistor	3-39
BD315	NPN Silicon Power Transistor	3-42
BD316	PNP Silicon Power Transistor	3-42
BD317	NPN Silicon Power Transistor	3-42
BD318	PNP Silicon Power Transistor	3-42
BD385	NPN Silicon Duowatt Transistor	3-45
BD386	PNP Silicon Duowatt Transistor	3-49
BD387	NPN Silicon Duowatt Transistor	3-45
BD388	PNP Silicon Duowatt Transistor	3-49
BD389	NPN Silicon Duowatt Transistor	3-45
BD390	PNP Silicon Duowatt Transistor	3-49
BD411	NPN Silicon Darlington Duowatt Transistor	3-53
BD412	NPN Silicon Darlington Duowatt Transistor	3-53
BD413	PNP Silicon Darlington Duowatt Transistor	3-57
BD414	PNP Silicon Darlington Duowatt Transistor	3-57
BD433	NPN Silicon Power Transistor	3-61
BD434	PNP Silicon Power Transistor	3-64
BD435	NPN Silicon Power Transistor	3-61
BD436	PNP Silicon Power Transistor	3-64
BD437	NPN Silicon Power Transistor	3-61
BD438	PNP Silicon Power Transistor	3-64
BD439	NPN Silicon Power Transistor	3-61
BD440	PNP Silicon Power Transistor	3-64
BD441	NPN Silicon Power Transistor	3-61
BD442	PNP Silicon Power Transistor	3-64
BD533	NPN Silicon Power Transistor	3-67
BD534	PNP Silicon Power Transistor	3-67
BD535	NPN Silicon Power Transistor	3-67
BD536	PNP Silicon Power Transistor	3-67
BD537	NPN Silicon Power Transistor	3-67
BD538	PNP Silicon Power Transistor	3-67
BD675	NPN Silicon Darlington Power Transistor	3-71
BD675A	NPN Silicon Darlington Power Transistor	3-71
BD676	PNP Silicon Darlington Power Transistor	3-73
BD676A	PNP Silicon Darlington Power Transistor	3-73
BD677	NPN Silicon Darlington Power Transistor	3-71
BD677A	NPN Silicon Darlington Power Transistor	3-71

TABLE OF CONTENTS (continued)

Device Number	Function	Page
BD678	PNP Silicon Darlington Power Transistor	3-73
BD678A	PNP Silicon Darlington Power Transistor	3-73
BD679	NPN Silicon Darlington Power Transistor	3-71
BD679A	NPN Silicon Darlington Power Transistor	3-71
BD680	PNP Silicon Darlington Power Transistor	3-73
BD680A	PNP Silicon Darlington Power Transistor	3-73
BD681	NPN Silicon Darlington Power Transistor	3-71
BD682	PNP Silicon Darlington Power Transistor	3-73
BD785	NPN Silicon Power Transistor	3-75
BD786	PNP Silicon Power Transistor	3-75
BD787	NPN Silicon Power Transistor	3-75
BD788	PNP Silicon Power Transistor	3-75
BD789	NPN Silicon Power Transistor	3-79
BD790	PNP Silicon Power Transistor	3-79
BD791	NPN Silicon Power Transistor	3-79
BD792	PNP Silicon Power Transistor	3-79
BD795	NPN Silicon Power Transistor	3-83
BD796	PNP Silicon Power Transistor	3-85
BD797	NPN Silicon Power Transistor	3-83
BD798	PNP Silicon Power Transistor	3-85
BD799	NPN Silicon Power Transistor	3-83
BD800	PNP Silicon Power Transistor	3-85
BD801	NPN Silicon Power Transistor	3-83
BD802	PNP Silicon Power Transistor	3-85
BD805	NPN Silicon Power Transistor	3-87
BD806	PNP Silicon Power Transistor	3-89
BD807	NPN Silicon Power Transistor	3-87
BD808	PNP Silicon Power Transistor	3-89
BD809	NPN Silicon Power Transistor	3-87
BD810	PNP Silicon Power Transistor	3-89
BD895	NPN Silicon Darlington Power Transistor	3-91
BD895A	NPN Silicon Darlington Power Transistor	3-91
BD896	PNP Silicon Darlington Power Transistor	3-93
BD896A	PNP Silicon Darlington Power Transistor	3-93
BD897	NPN Silicon Darlington Power Transistor	3-91
BD897A	NPN Silicon Darlington Power Transistor	3-91
BD898	PNP Silicon Darlington Power Transistor	3-93
BD898A	PNP Silicon Darlington Power Transistor	3-93
BD899	NPN Silicon Darlington Power Transistor	3-91
BD899A	NPN Silicon Darlington Power Transistor	3-91
BD900	PNP Silicon Darlington Power Transistor	3-93
BD900A	PNP Silicon Darlington Power Transistor	3-93
BD901	NPN Silicon Darlington Power Transistor	3-91
BD902	PNP Silicon Darlington Power Transistor	3-93
BDV64	PNP Silicon Darlington Power Transistor	3-95
BDV64A	PNP Silicon Darlington Power Transistor	3-95
BDV64B	PNP Silicon Darlington Power Transistor	3-95
BDV65	NPN Silicon Darlington Power Transistor	3-95
BDV65A	NPN Silicon Darlington Power Transistor	3-95
BDV65B	NPN Silicon Darlington Power Transistor	3-95
BDW39	NPN Silicon Darlington Power Transistor	3-99
BDW40	NPN Silicon Darlington Power Transistor	3-99
BDW41	NPN Silicon Darlington Power Transistor	3-99
BDW42	NPN Silicon Darlington Power Transistor	3-99
BDW44	PNP Silicon Darlington Power Transistor	3-99
BDW45	PNP Silicon Darlington Power Transistor	3-99
BDW46	PNP Silicon Darlington Power Transistor	3-99
BDW47	PNP Silicon Darlington Power Transistor	3-99
BDX33	NPN Silicon Darlington Power Transistor	3-105
BDX33A	NPN Silicon Darlington Power Transistor	3-105
BDX33B	NPN Silicon Darlington Power Transistor	3-105
BDX33C	NPN Silicon Darlington Power Transistor	3-105
BDX34	PNP Silicon Darlington Power Transistor	3-105
BDX34A	PNP Silicon Darlington Power Transistor	3-105
BDX34B	PNP Silicon Darlington Power Transistor	3-105

TABLE OF CONTENTS (continued)

Device Number	Function	Page
BDX34C	PNP Silicon Darlington Power Transistor	3-105
BDX53	NPN Silicon Darlington Power Transistor	3-109
BDX53A	NPN Silicon Darlington Power Transistor	3-109
BDX53B	NPN Silicon Darlington Power Transistor	3-109
BDX53C	NPN Silicon Darlington Power Transistor	3-109
BDX54	PNP Silicon Darlington Power Transistor	3-109
BDX54A	PNP Silicon Darlington Power Transistor	3-109
BDX54B	PNP Silicon Darlington Power Transistor	3-109
BDX54C	PNP Silicon Darlington Power Transistor	3-109
BF198	NPN Silicon RF Transistor	4-80
BF199	NPN Silicon RF Transistor	4-82
BF240	NPN Silicon RF Transistor	4-85
BF241	NPN Silicon RF Transistor	4-85
BF245	N-Channel Junction Field Effect Transistor	5-3
BF245A	N-Channel Junction Field Effect Transistor	5-3
BF245B	N-Channel Junction Field Effect Transistor	5-3
BF245C	N-Channel Junction Field Effect Transistor	5-3
BF254	NPN Silicon RF Transistor	4-89
BF255	NPN Silicon RF Transistor	4-89
BF256	N-Channel Junction Field Effect Transistor	5-7
BF256A	N-Channel Junction Field Effect Transistor	5-7
BF256B	N-Channel Junction Field Effect Transistor	5-7
BF256C	N-Channel Junction Field Effect Transistor	5-7
BF257	NPN Silicon Amplifier Transistor	4-92
BF258	NPN Silicon Amplifier Transistor	4-92
BF259	NPN Silicon Amplifier Transistor	4-92
BF466	NPN Silicon Duowatt Transistor	3-114
BF467	NPN Silicon Duowatt Transistor	3-114
BF468	NPN Silicon Duowatt Transistor	3-114
BF491	PNP Silicon High Voltage Transistor	4-94
BF492	PNP Silicon High Voltage Transistor	4-94
BF493	PNP Silicon High Voltage Transistor	4-94
BF506	PNP Silicon VHF Transistor	4-97
BF509	PNP Silicon VHF Transistor	4-100
BF757	NPN Silicon Duowatt Transistor	3-118
BF758	NPN Silicon Duowatt Transistor	3-118
BF759	NPN Silicon Duowatt Transistor	3-118
BF760	PNP Silicon Duowatt Transistor	3-122
BF761	PNP Silicon Duowatt Transistor	3-122
BF762	PNP Silicon Duowatt Transistor	3-122
BF787	NPN Silicon Amplifier Transistor	4-104
BF788	NPN Silicon Amplifier Transistor	4-104
BF789	NPN Silicon Amplifier Transistor	4-104
BF790	PNP Silicon Amplifier Transistor	4-104
BF791	PNP Silicon Amplifier Transistor	4-104
BF792	PNP Silicon Amplifier Transistor	4-104
BF959	NPN Silicon RF Transistor	4-107
BT162-400	TRIAC	6-3
BT162-600	TRIAC	6-3
BU205	NPN Silicon Power Transistor	3-126
BU208	NPN Silicon Power Transistor	3-129
BU208A	NPN Silicon Power Transistor	3-129
BU208D	NPN Silicon Power Transistor	3-134
BU209	NPN Silicon power transistors	3-129
BU209A	NPN Silicon power transistors	3-129
BU323	NPN Silicon Carlington Power Transistor	3-136
BU323A	NPN Silicon Darlington Power Transistor	3-136
BU236	NPN Silicon Power Transistor	3-140
BU326,A	NPN Silicon Power Transistor	3-140
BU406	NPN Silicon Power Transistor	3-143
BU407	NPN Silicon Power Transistor	3-143
BU426	NPN Silicon Power Transistor	3-147
BU426A	NPN Silicon Power Transistor	3-147
BU522	NPN Silicon Darlington Power Transistor	3-151
BU522A	NPN Silicon Darlington Power Transistor	3-151

TABLE OF CONTENTS (continued)

Device Number	Function	Page
BU522B	NPN Silicon Darlington Power Transistor	3-151
BU800	NPN Silicon Power Transistor	3-154
BY126	Silicon Rectifier Diode	7-12
BY127	Silicon Rectifier Diode	7-12
BY133	Silicon Rectifier Diode	7-12
BY196	Silicon Rectifier Diode	7-16
BY197	Silicon Rectifier Diode	7-16
BY198	Silicon Rectifier Diode	7-16
BY199	Silicon Rectifier Diode	7-16
BY206	Silicon Rectifier Diode	7-22
BY207	Silicon Rectifier Diode	7-22
BY210-400	Silicon Rectifier Diode	7-28
BY210-600	Silicon Rectifier Diode	7-28
BY210-800	Silicon Rectifier Diode	7-28
BY251	Silicon Rectifier Diode	7-34
BY252	Silicon Rectifier Diode	7-34
BY253	Silicon Rectifier Diode	7-34
BY254	Silicon Rectifier Diode	7-34
BY255	Silicon Rectifier Diode	7-34
BY296	Silicon Rectifier Diode	7-39
BY297	Silicon Rectifier Diode	7-39
BY298	Silicon Rectifier Diode	7-39
BY299	Silicon Rectifier Diode	7-39
BY396	Silicon Rectifier Diode	7-43
BY397	Silicon Rectifier Diode	7-43
BY398	Silicon Rectifier Diode	7-43
BY399	Silicon Rectifier Diode	7-43
BY406	Silicon Rectifier Diode	7-51
BY407	Silicon Rectifier Diode	7-51
BY500-100	Silicon Rectifier Diode	7-57
BY500-200	Silicon Rectifier Diode	7-57
BY500-400	Silicon Rectifier Diode	7-57
BY500-600	Silicon Rectifier Diode	7-57
BY601	Silicon Rectifier Diode	7-65
BY602	Silicon Rectifier Diode	7-65
BY603	Silicon Rectifier Diode	7-65
BY604	Silicon Rectifier Diode	7-65
BY605	Silicon Rectifier Diode	7-65
BY606	Silicon Rectifier Diode	7-65
BY607	Silicon Rectifier Diode	7-65
BY608	Silicon Rectifier Diode	7-65
BYT25-50	Miniature Single Phase Full Wave Bridge Rectifier	7-69
BYT25-100	Miniature Single Phase Full Wave Bridge Rectifier	7-69
BYT25-200	Miniature Single Phase Full Wave Bridge Rectifier	7-69
BYT25-400	Miniature Single Phase Full Wave Bridge Rectifier	7-69
BYT25-500	Miniature Single Phase Full Wave Bridge Rectifier	7-69
BYT25-800	Miniature Single Phase Full Wave Bridge Rectifier	7-69
BYT25-1000	Miniature Single Phase Full Wave Bridge Rectifier	7-69
BYW20	Single Phase Full Wave Bridge Rectifier	7-72
BYW21	Single Phase Full Wave Bridge Rectifier	7-72
BYW22	Single Phase Full Wave Bridge Rectifier	7-72
BYW24	Single Phase Full Wave Bridge Rectifier	7-72
BYW26	Single Phase Full Wave Bridge Rectifier	7-72
BYW28	Single Phase Full Wave Bridge Rectifier	7-72
BYW29	Single Phase Full Wave Bridge Rectifier	7-72
BYX10	Silicon Rectifier Diode	7-72
BYX55-350	Silicon Rectifier Diode	7-79
BYX55-600	Silicon Rectifier Diode	7-79
BZX79C2V4 thru BZX79C200	Zener Diodes (500 mW – 2.4 V/200 V)	7-85
BZX83C2V7 thru BZX83C33	Zener Diodes (500 mW – 2.7 V/33 V)	7-88
J308	N-Channel Junction Field Effect Transistor	5-11

TABLE OF CONTENTS (continued)

Device Number	Function	Page
J309	N-Channel Junction Field Effect Transistor	5-11
J310	N-Channel Junction Field Effect Transistor	5-11
L14H1	NPN Silicon Photo Transistor	8-3
L14H2	NPN Silicon Photo Transistor	8-3
L14H3	NPN Silicon Photo Transistor	8-3
L14H4	NPN Silicon Photo Transistor	8-3
MAC15,A	TRIAC	6-7
MAC92-1	TRIAC	6-11
MAC220-221	TRIAC	6-53
MAC223	TRIAC	6-15
MAC228	TRIAC	6-18
MAC525,A	TRIAC	6-20
MBD101	Silicon Hot Carrier UHF Mixer Diode	7-90
MBD102	Silicon Hot Carrier UHF Mixer Diode	7-92
MBI101	Silicon Hot Carrier UHF Mixer Diode	7-94
MBR115P	Schottky Barrier Rectifier Diode	7-96
MBR120P	Schottky Barrier Rectifier Diode	7-96
MBR130P	Schottky Barrier Rectifier Diode	7-96
MBR140P	Schottky Barrier Rectifier Diode	7-96
MBR320P	Schottky Barrier Rectifier Diode	7-100
MBR330P	Schottky Barrier Rectifier Diode	7-100
MBR340P	Schottky Barrier Rectifier Diode	7-100
MCR100-3	Silicon Controlled Rectifier –100 V	6-21
MCR100-4	Silicon Controlled Rectifier –200 V	6-21
MCR100-5	Silicon Controlled Rectifier –300 V	6-21
MCR100-6	Silicon Controlled Rectifier –400 V	6-21
MCR100-7	Silicon Controlled Rectifier –500 V	6-21
MCR100-8	Silicon Controlled Rectifier –600 V	6-21
MCR106-1	Silicon Controlled Rectifier –30 V	6-23
MCR106-2	Silicon Controlled Rectifier –60 V	6-23
MCR106-3	Silicon Controlled Rectifier –100 V	6-23
MCR106-4	Silicon Controlled Rectifier –200 V	6-23
MCR106-6	Silicon Controlled Rectifier –400 V	6-23
MCR106-8	Silicon Controlled Rectifier –600 V	6-23
MCR220-5	Silicon Controlled Rectifier –300 V	6-25
MCR220-7	Silicon Controlled Rectifier –500 V	6-25
MCR220-9	Silicon Controlled Rectifier –700 V	6-25
MCR221-5	Silicon Controlled Rectifier –300 V	6-29
MCR221-7	Silicon Controlled Rectifier –500 V	6-29
MCR221-9	Silicon Controlled Rectifier –700 V	6-29
MDA200	Single Phase Full Wave Bridge Rectifier 50 V	7-104
MDA201	Single Phase Full Wave Bridge Rectifier 100 V	7-104
MDA202	Single Phase Full Wave Bridge Rectifier 200 V	7-104
MDA204	Single Phase Full Wave Bridge Rectifier 400 V	7-104
MDA206	Single Phase Full Wave Bridge Rectifier 600 V	7-104
MDA208	Single Phase Full Wave Bridge Rectifier 800 V	7-104
MDA210	Single Phase Full Wave Bridge Rectifier 1000 V	7-104
MDA920A1	Single Phase Full Wave Bridge Rectifier 25 V	7-106
MDA920A2	Single Phase Full Wave Bridge Rectifier 50 V	7-106
MDA920A3	Single Phase Full Wave Bridge Rectifier 100 V	7-106
MDA920A4	Single Phase Full Wave Bridge Rectifier 200 V	7-106
MDA920A5	Single Phase Full Wave Bridge Rectifier 300 V	7-106
MDA920A6	Single Phase Full Wave Bridge Rectifier 400 V	7-106
MDA920A7	Single Phase Full Wave Bridge Rectifier 600 V	7-106
MDA920A8	Single Phase Full Wave Bridge Rectifier 800 V	7-106
MDA920A9	Single Phase Full Wave Bridge Rectifier 1000 V	7-106
MFE130	N-Channel Dual Gate MOS Field Effect Transistor	5-13
MFE131	N-Channel Dual Gate MOS Field Effect Transistor	5-13
MFE132	N-Channel Dual Gate MOS Field Effect Transistor	5-13
MFE140	N-Channel Dual Gate MOS Field Effect Transistor	5-17
MJ802	NPN Silicon Power Transistor	3-156
MJ900	PNP Silicon Darlington Power Transistor	3-158
MJ901	PNP Silicon Darlington Power Transistor	3-158
MJ1000	NPN Silicon Darlington Power Transistor	3-158
MJ1001	NPN Silicon Darlington Power Transistor	3-158

TABLE OF CONTENTS (continued)

Device Number	Function	Page
MJ2500	PNP Silicon Darlington Power Transistor	3-160
MJ2501	PNP Silicon Darlington Power Transistor	3-160
MJ2955	PNP Silicon Power Transistor	3-162
MJ3000	NPN Silicon Darlington Power Transistor	3-160
MJ3001	NPN Silicon Darlington Power Transistor	3-160
MJ3055	NPN Silicon Power Transistor	3-162
MJ4030	PNP Silicon Darlington Power Transistor	3-166
MJ4031	PNP Silicon Darlington Power Transistor	3-166
MJ4032	PNP Silicon Darlington Power Transistor	3-166
MJ4033	NPN Silicon Darlington Power Transistor	3-166
MJ4034	NPN Silicon Darlington Power Transistor	3-166
MJ4035	NPN Silicon Darlington Power Transistor	3-166
MJ8500	NPN Silicon Power Transistor	3-168
MJ8501	NPN Silicon Power Transistor	3-168
MJ8502	NPN Silicon Power Transistor	3-174
MJ8503	NPN Silicon Power Transistor	3-174
MJ15011	NPN Silicon Power Transistor	3-205
MJ15012	PNP Silicon Power Transistor	3-205
MJ15022	NPN Silicon Power Transistor	3-207
MJ15023	PNP Silicon Power Transistor	3-210
MJ15024	NPN Silicon Power Transistor	3-207
MJ15025	PNP Silicon Power Transistor	3-210
MJE340	NPN Silicon Power Transistor	3-180
MJE350	PNP Silicon Power Transistor	3-182
MJE700,T	PNP Silicon Darlington Power Transistor	3-184
MJE703,T	PNP Silicon Darlington Power Transistor	3-184
MJE800,T	NPN Silicon Darlington Power Transistor	3-184
MJE803,T	NPN Silicon Darlington Power Transistor	3-184
MJE2955	PNP Silicon Power Transistor	3-189
MJE2955T	PNP Silicon Power Transistor	3-189
MJE3055	NPN Silicon Power Transistor	3-191
MJE3055T	NPN Silicon Power Transistor	3-191
MJE8500	NPN Silicon Power Transistor	3-193
MJE8501	NPN Silicon Power Transistor	3-193
MJE8502	NPN Silicon Power Transistor	3-199
MJE8503	NPN Silicon Power Transistor	3-199
MJE15028	NPN Silicon Power Transistor	3-213
MJE15029	PNP Silicon Power Transistor	3-213
MJE15030	NPN Silicon Power Transistor	3-213
MJE15031	PNP Silicon Power Transistor	3-213
MLED92	Infrared-Emitting Diode	8-5
MLED93	Infrared-Emitting Diode	8-7
MLED94	Infrared-Emitting Diode	8-7
MLED95	Infrared-Emitting Diode	8-7
MOC3009	Opto Coupled Isolator	8-9
MOC3010	Opto Coupled Isolator	8-9
MOC3011	Opto Coupled Isolator	8-9
MOC3020S	Opto Coupled Isolator	8-13
MOC3021S	Opto Coupled Isolator	8-13
MOC3030	Opto Coupled Isolator	8-17
MOC3031	Opto Coupled Isolator	8-17
MPF102	N-Channel Junction Field Effect Transistor	5-23
MPF130	N-Channel Dual Gate MOS Field Effect Transistor	5-13
MPF131	N-Channel Dual Gate MOS Field Effect Transistor	5-13
MPF132	N-Channel Dual Gate MOS Field Effect Transistor	5-13
MPF4391	N-Channel Junction Field Effect Transistor	5-24
MPF4392	N-Channel Junction Field Effect Transistor	5-24
MPF4393	N-Channel Junction Field Effect Transistor	5-24
MPS-A05	NPN Silicon Amplifier Transistor	4-110
MPS-A06	NPN Silicon Amplifier Transistor	4-110
MPS-A13	NPN Silicon Darlington Amplifier Transistor	4-116
MPS-A14	NPN Silicon Darlington Amplifier Transistor	4-116
MPS-A16	NPN Silicon Amplifier Transistor	4-119
MPS-A17	NPN Silicon Amplifier Transistor	4-119
MPS-A55	PNP Silicon Amplifier Transistor	4-110

TABLE OF CONTENTS (continued)

Device Number	Function	Page
MPS-A56	PNP Silicon Amplifier Transistor	4-110
MPS-A62	PNP Silicon Darlington Amplifier Transistor	4-121
MPS-A63	PNP Silicon Darlington Amplifier Transistor	4-121
MPS-A64	PNP Silicon Darlington Amplifier Transistor	4-121
MPS-L01	NPN Silicon Amplifier Transistor	4-125
MR1-1000	Silicon Rectifier Diode	7-110
MR1-1200	Silicon Rectifier Diode	7-110
MR1-1400	Silicon Rectifier Diode	7-110
MR1-1600	Silicon Rectifier Diode	7-110
MR250-1	Silicon Rectifier Diode	7-113
MR250-2	Silicon Rectifier Diode	7-113
MR250-3	Silicon Rectifier Diode	7-113
MR250-4	Silicon Rectifier Diode	7-113
MR250-5	Silidon Rectifier Diode	7-113
MR500	Silicon Rectifier Diode	7-115
MR501	Silicon Rectifier Diode	7-115
MR502	Silicon Rectifier Diode	7-115
MR504	Silicon Rectifier Diode	7-115
MR506	Silicon Rectifier Diode	7-115
MR508	Silicon Rectifier Diode	7-115
MR510	Silicon Rectifier Diode	7-115
MR751	Silicon Rectifier Diode	7-121
MR752	Silicon Rectifier Diode	7-121
MR754	Silicon Rectifier Diode	7-121
MR756	Silicon Rectifier Diode	7-121
MR758	Silicon Rectifier Diode	7-121
MR760	Silicon Rectifier Diode	7-121
MR810	Silicon Rectifier Diode	7-125
MR911	Silicon Rectifier Diode	7-125
MR812	Silicon Rectifier Diode	7-125
MR813	Silicon Rectifier Diode	7-125
MR814	Silicon Rectifier Diode	7-125
MR816	Silicon Rectifier Diode	7-125
MR817	Silicon Rectifier Diode	7-125
MR818	Silicon Rectifier Diode	7-125
MR850	Silicon Rectifier Diode	7-131
MR851	Silicon Rectifier Diode	7-131
MR852	Silicon Rectifier Diode	7-131
MR854	Silicon Rectifier Diode	7-131
MR856	Silicon Rectifier Diode	7-131
MR910	Silicon Rectifier Diode	7-139
MR911	Silicon Rectifier Diode	7-139
MR912	Silicon Rectifier Diode	7-139
MR913	Silicon Rectifier Diode	7-139
MR914	Silicon Rectifier Diode	7-139
MR916	Silicon Rectifier Diode	7-139
MR917	Silicon Rectifier Diode	7-139
MR918	Silicon Rectifier Diode	7-139
MTM474	N-Channel TMOS Power FET	3-215
MTM475	N-Channel TMOS Power FET	3-215
MTM564	N-Channel TMOS Power FET	3-221
MTM565	N-Channel TMOS Power FET	3-221
MTM1224	N-Channel TMOS Power FET	3-227
MTM1225	N-Channel TMOS Power FET	3-227
MTP474	N-Channel TMOS Power FET	3-215
MTP475	N-Channel TMOS Power FET	3-215
MTP564	N-Channel TMOS Power FET	3-221
MTP565	N-Channel TMOS Power FET	3-221
MTP1224	N-Channel TMOS Power FET	3-227
MTP1225	N-Channel TMOS Power FET	3-227
MV104	Dual Variable Capacitance Tuning Diode	7-143
MV209	Variable Capitance Tuning Diode	7-145
MVAM115	Variable Capitance Tuning Diode	7-147
MVAM125	Variable Capitance Tuning Diode	7-147
MVS240	Tuning Diode — Voltage Reference Diode	7-149

TABLE OF CONTENTS (continued)

Device Number	Function	Page
MVS460	Tuning Diode – Voltage Reference Diode	7-151
MZD3.9 thru	Zener Diodes (1.3 W – 3.9 V/200 V)	7-153
MZD200	Zener Diodes (1.3 W – 3.9 V/200 V)	7-153
MZPD2.7 thru	Zener Diodes (500 mW – 2.7 V/33 V)	7-88
MZDP33	Zener Diodes (500 mW – 2.7 V/33 V)	7-88
TIP47	NPN Silicon Power Transistor	3-233
TIP48	NPN Silicon Power Transistor	3-233
TIP49	NPN Silicon Power Transistor	3-233
TIP 50	NPN Silicon power Transistor	3-233
1N4001,S	Silicon Rectifier Diode	7-157
1N4002,S	Silicon Rectifier Diode	7-157
1N4003,S	Silicon Rectifier Diode	7-157
1N4004,S	Silicon Rectifier Diode	7-157
1N4005,S	Silicon Rectifier Diode	7-157
1N4006,S	Silicon Rectifier Diode	7-157
1N4007,S	Silicon Rectifier Diode	7-157
1N4933	Silicon Rectifier Diode	7-158
1N4934	Silicon Rectifier Diode	7-158
1N4935	Silicon Rectifier Diode	7-158
1N4936	Silicon Rectifier Diode	7-158
1N4937	Silicon Rectifier Diode	7-158
1N5333 thru	Zener Diodes (5 W – 3.3 V/200 V)	7-164
1N5388	Zener Diodes (5 W – 3.3 V/200 V)	7-164
1N5400	Silicon Rectifier Diode	7-168
1N5401	Silicon Rectifier Diode	7-168
1N5402	Silicon Rectifier Diode	7-168
1N5404	Silicon Rectifier Diode	7-168
1N5406	Silicon Rectifier Diode	7-168
1N5407	Silicon Rectifier Diode	7-168
1N5817	Schottky Barrier Rectifier Diode	7-96
1N5818	Schottky Barrier Rectifier Diode	7-96
1N5820	Schottky Barrier Rectifier Diode	7-100
1N5821	Schottky Barrier Rectifier Diode	7-100
2N2646	Silicon Unijunction Transistor	6-33
2N2647	Silicon Unijunction Transistor	6-33
2N3773	NPN Silicon Power Transistor	3-237
2N4117	N-Channel Junction Field Effect Transistor	5-28
2N4117A	N-Channel Junction Field Effect Transistor	5-28
2N4118	N-Channel Junction Field Effect Transistor	5-28
2N4118A	N-Channel Junction Field Effect Transistor	5-28
2N4119	N-Channel Junction Field Effect Transistor	5-28
2N4119A	N-Channel Junction Field Effect Transistor	5-28
2N4351	N-Channel MOS Field Effect Transistor	5-30
2N4352	P-Channel MOS Field Effect Transistor	5-34
2N4416	N-Channel Junction Field Effect Transistor	5-38
2N4870	Unijunction Transistor	6-35
2N4871	Unijunction Transistor	6-35
2N5060	Silicon Controlled Rectifier	6-39
2N5061	Silicon Controlled Rectifier	6-39
2N5062	Silicon Controlled Rectifier	6-39
2N5063	Silicon Controlled Rectifier	6-39
2N5064	Silicon Controlled Rectifier	6-39
2N5457	N-Channel Junction Field Effect Transistor	5-44
2N5458	N-Channel Junction Field Effect Transistor	5-44
2N5459	N-Channel Junction Field Effect Transistor	5-44
2N5460	P-Channel JUnction Field Effect Transistor	5-45
2N5461	P-Channel Junction Field Effect Transistor	5-45
2N5462	P-Channel Junction Field Effect Transistor	5-45
2N5463	P-Channel Junction Field Effect Transistor	5-45
2N5464	P-Channel Junction Field Effect Transistor	5-45
2N5465	P-Channel Junction Field Effect Transistor	5-45
2N5484	N-Channel Junction Field Effect Transistor	5-48

TABLE OF CONTENTS (continued)

Device Number	Function	Page
2N5485	N-Channel Junction Field Effect Transistor	5-48
2N5486	N-Channel Junction Field Effect Transistor	5-48
2N5638	N-Channel Junction Field Effect Transistor	5-50
2N5639	N-Channel Junction Field Effect Transistor	5-50
2N5640	N-channel Junction Field Effect Transistor	5-50
2N5777	NPN Silicon Photo Darlington Transistor	8-20
2N5778	NPN Silicon Photo Darlington Transistor	8-20
2N5779	NPN Silicon Photo Darlington Transistor	8-20
2N5780	NPN Silicon Photo Darlington Transistor	8-20
2N6027	Programmable Unijunction Transistor	6-43
2N6028	Programmable Unijunction Transistor	6-43
2N6068	TRIAC	6-47
2N6069	TRIAC	6-47
2N6070	TRIAC	6-47
2N6071	TRIAC	6-47
2N6072	TRIAC	6-47
2N6073	TRIAC	6-47
2N6074	TRIAC	6-47
2N6075	TRIAC	6-47
2N6236	Silicon Controlled Rectifier	6-51
2N6237	Silicon Controlled Rectifier	6-51
2N6238	Silicon Controlled Rectifier	6-51
2N6239	Silicon Controlled Rectifier	6-51
2N6240	Silicon Controlled Rectifier	6-51
2N6241	Silicon Controlled Rectifier	6-51
2N6241	Silicon Controlled Rectifier	6-51
2N6342	TRIAC	6-53
2N6342A	TRIAC	6-57
2N6343	TRIAC	6-53
2N6343A	TRIAC	6-57
2N6344	TRIAC	6-53
2N6344A	TRIAC	6-57
2N6345	TRIAC	6-53
2N6345A	TRIAC	6-57
2N6346	TRIAC	6-53
2N6346A	TRIAC	6-57
2N6347	TRIAC	6-53
2N6347A	TRIAC	6-57
2N6348	TRIAC	6-53
2N6348A	TRIAC	6-57
2N6349	TRIAC	6-53
2N6349A	TRIAC	6-57
2N6394	Silicon Controlled Rectifier	6-25
2N6395	Silicon Controlled Rectifier	6-25
2N6396	Silicon Controlled Rectifier	6-25
2N6397	Silicon Controlled Rectifier	6-25
2N6398	Silicon Controlled Rectifier	6-25
2N6399	Silicon Controlled Rectifier	6-25
2N6400	Silicon Controlled Rectifier	6-29
2N6401	Silicon Controlled Rectifier	6-29
2N6402	Silicon Controlled Rectifier	6-29
2N6403	Silicon Controlled Rectifier	6-29
2N6404	Silicon Controlled Rectifier	6-29
2N6405	Silicon Controlled Rectifier	6-29
2N6486	NPN Silicon Power Transistor	3-242
2N6487	NPN Silicon Power Transistor	3-242
2N6488	NPN Silicon Power Transistor	3-242
2N6489	PNP Silicon Power Transistor	3-242
2N6490	PNP Silicon Power Transistor	3-242
2N6491	PNP Silicon Power Transistor	3-242
2N6504	TRIAC	6-61
2N6505	TRIAC	6-61
2N6506	TRIAC	6-61
2N6508	TRIAC	6-61
2N6509	TRIAC	6-61

TABLE OF CONTENTS (continued)

Device Number	Function	Page
2N6609	PNP Silicon Power Transistor	3-237
3N201	N-Channel Dual Gate MOS Field Effect Transistor	5-52
3N202	N-Channel Dual Gate MOS Field Effect Transistor	5-52
3N203	N-Channel Dual Gate MOS Field Effect Transistor	5-52
3N211	N-Channel Dual Gate MOS Field Effect Transistor	5-58
3N212	N-Channel Dual Gate MOS Field Effect Transistor	5-58
3N213	N-Channel Dual Gate MOS Field Effect Transistor	5-58
3N253	Single Phase Full Wave Bridge Rectifier	7-104
3N254	Single Phase Full Wave Bridge Rectifier	7-104
3N255	Single Phase Full Wave Bridge Rectifier	7-104
3N256	Single Phase Full Wave Bridge Rectifier	7-104
3N237	Single Phase Full Wave Bridge Rectifier	7-104
3N258	Single Phase Full Wave Bridge Rectifier	7-104
3N259	Single Phase Full Wave Bridge Rectifier	7-104
4N25,A	Opto Coupled Isolator	8-22
4N26	Opto Coupled Isolator	8-22
4N27	Opto Coupled Isolator	8-22
4N28	Opto Coupled Isolator	8-22
4N29	Opto Coupled Isolator	8-26
4N30	Opto Coupled Isolator	8-26
4N31	Opto Coupled Isolator	8-26
4N32	Opto Coupled Isolator	8-26
4N33	Opto Coupled Isolator	8-26
4N38	Opto Coupled Isolator	8-30
4N38A	Opto Coupled Isolator	8-30

SECTION 2
LEAD TAPE PACKAGING

- **Lead tape packaging for axial lead components**

Lead tape packaging standards for axial-lead components

1.0. SCOPE

This section covers packaging requirements for the following axial-lead components for use in automatic testing and assembly equipment: Motorola Case 51 (DO-7), Case 52 (DO-13), Case 59 (DO-41), Case 267, Case 299 (DO-35), Case 59-04, Case 169-02 and Case 17. Packaging, as covered in this document, shall consist of axial-lead components mounted by their leads on pressure-sensitive tape, either wound onto a reel of folded in an oriented manner in a container (ammunition pack).

2.0. PURPOSE

This document establishes Motorola standard practices for lead-tape packaging of axial-lead components and meets the requirements of EIA Standard RS-296-C, "Reel Packaging of Components with Axial Leads".

3.0. REQUIREMENTS

3.1. *Component Leads*

3.1.1. Component leads shall not be bent beyond dimension E from their nominal position. See Figure 2.

3.1.2. The "C" dimension shall be governed by the overall length of the reel packaged component. The distance between flanges shall be 0.318 cm to 0.635 cm greater than the overall component length. See Figures 2 and 3.

3.2. *Orientation*

All polarized components must be oriented in one diretion. The cathode lead tape shall be blue, and the anode tape shall be white. See Figure 1.

3.3. *Reeling*

3.3.1. Components on any reel shall not represent more than two date codes when date code identification is required.

3.3.2. Component leads shall be positioned perpendicularly between pairs of 0.635 cm tape. See Figure 2.

3.3.3. A minimum 30.5 cm leader of tape shall be provided before the first and last component on the reel.

3.3.4. 50 lb. Kraft paper must be wound between layers of components as far as necessary for component protection. Width of paper is 0.158 cm to 1.905 cm less than "C" dimension of reel. See Figure 3.

3.3.5. A row of components must be centered between the tapes ±0.119 cm. In addition, individual components may deviate from center of component row ±0.079 cm. See Figure 2.

3.3.6. Staples shall not be used for splicing. No more than 4 layers of tape shall be used in any splice area and no tape shall be offset from another by more than 0.079 cm noncumulative. Tape splices shall overlap at least 15.24 cm for butt joints and at least 7.62 cm for lap joints, and shall not be weaker than unspliced tape.

3.3.7. Quantity per reel shall be as indicated in Table 1. When reeling quantity is less than the established minimum of a suitable sized reel, an ammunition pack will be used. Quantities less than the ammunition pack munimum will not be lead-taped.

3.3.8. A maximum of 10 components may be missing from any 3 metre section. A maximum of 2 consecutive components may be missing, provided this gap is followed by 6 consecutive components.

3.3.9. The single face roll pad shall be placed around the finished reel and taped securely. Each reel shall then be placed in an appropriate container.

3.4. *Marking*

Minimum reel and carton marking shall consist of the following: See Figure 3.

Customer Part Number
Purchase Order Number
Quantity
Date of Reeling (when applicable)
Manufacturer's Name
Electrical Value (when applicable)
Date Codes (when applicable; see Note 3.3.1.)
Tape (when applicable)

4.0. EXCEPTIONS

Requirements differing from this Motorola standard shall be negotiated with the factory.
Complies with DIN 40810 for Case 59.04, Case 267 Rectifier Diodes.

TABLE 1 – PACKAGING

Component Type (Case)	Quantity Per Reel Min/Max	Ammunition Pack Quantity Min	Component Spacing A	Tape Spacing B	Reel Dimensions C	Reel Dimensions D(Max)	Max. Off Alignment E
Case 51 (DO-7) Case 299 (DO-35)	1000/3000	500	0.508 ± 0.079	5.16 ± 0.079	7.62	26.67	0.158
Case 17 Case 59 (DO-41) Case 59-04 Case 169-02	1000/5500	500	0.508 ± 0.038	5.16 ± 0.079	7.62	35.56	0.119
Case 52 (DO-13)	500/1500	250	0.953 ± 0.038	6.033 ± 0.051	9.68	35.56	0.119
Case 267	500/1500	250	0.953 ± 0.038	0.953 ± 0.079	7.62	35.56	0.119

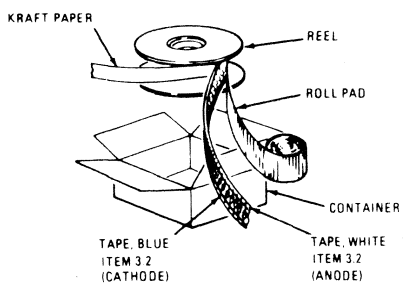


FIGURE 1 – REEL PACKING

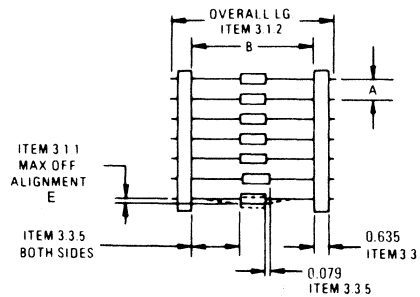


FIGURE 2 – COMPONENT SPACING

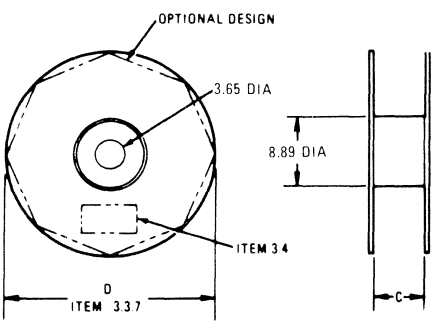


FIGURE 3 – REEL DIMENSIONS

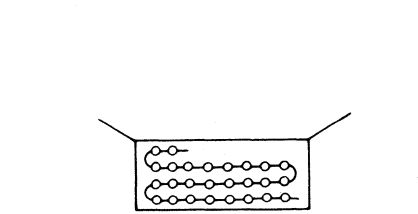


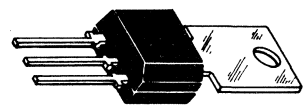
FIGURE 4 – AMMUNITION PACK

SECTION 3
POWER TRANSISTORS

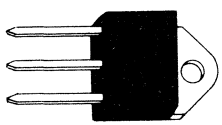
- **Silicon power plastic**
- **Silicon power metal**
- **Uniwatt and Duowatt**
- **Power MOS**

Section 3—Packages

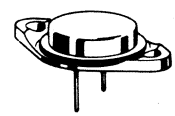
Case 77.04



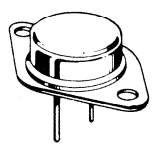
Case 306.04



TO 220
Case 340



Case 11
Case 11.01
Case 11.03
TO 3



Case 1.05
TO 3

3

POWER TRANSISTORS

Power Plastic Transistors (in order of I_C max.)

Device	Designation	I_C (cont.) A	H_{FE} @ → (min.)	I_C → A	V_{CE} V	P_D W	V_{CEO} V	Polarity	Package	Page
BD 232	TV Power Output and Line Driving	0.5	25	0.05	5	20	300	NPN	77.04	3- 20
MJE 340	High Voltage General	0.5	30	0.05	10	20,8,3	300	NPN	77.04	3-380
MJE 350	High Voltage General	0.5	30	0.05	10	20	300	PNP	77.04	3-182
TIP47,48,49,50	High Voltage General	1	30	0.3	10	40	250-400	NPN	TO-220	3-233
BD 135, 137, 139	Audio Amplifier and Driver	1.5	25	0.5	2	12.5	45-80	NPN	77.04	3- 4
BD 136, 138, 140	Audio Amplifier and Driver	1.5	25	0.5	2	12.5	45-80	PNP	77.04	3- 6
BD 165, 167, 169	Audio Amplifier and Driver	1.5	40	0.15	2	20	45-80	NPN	77.04	3- 8
BD 166, 168, 170	Audio Amplifier and Driver	1.5	40	0.15	2	20	45-80	PNP	77.04	3- 10
BD 233, 235, 237	Audio Amplifier and Driver	2	40	0.15	2	25	45-80	NPN	77.04	3- 22
BD 234, 236, 238	Audio Amplifier and Driver	2	40	0.15	2	25	45-80	PNP	77.04	3- 24
BD 239	General Purpose	2	40	0.2	4	2	45	NPN	TO220	3- 26
BD 240	General Purpose	2	40	0.2	4	2	45	PNP	TO220	3- 26
MJE 8500, 8501	Power Switching	2.5	7.5	0.5	5	65	700-800	NPN	TO220	3-193
BD 175, 177, 179	Audio Amplifier and Driver	3	40	0.15	2	30	45-80	NPN	77.04	3- 12
BD 176, 178, 180	Audio Amplifier and Driver	3	40	0.15	2	30	45-80	PNP	77.04	3- 14
BD 241	General Purpose	3	25	1	4	40	45	NPN	TO220	3- 28
BD 242	General Purpose	3	25	1	4	40	45	PNP	TO220	3- 28
BD 185, 187, 189	Audio Amplifier	4	40	0.5	2	40	30-60	NPN	77.04	3- 16
BD 186, 188, 190	Audio Amplifier	4	40	0.5	2	40	30-60	PNP	77.04	3- 18
BD 433, 435, 437	Switching and Amplifier	4	15-40	10	5	36	20-80	NPN	77.04	3- 61
BD 439, 444										3- 61
BD 434, 436, 438	Switching and Amplifier	4	15-40	10	5	36	22-80	PNP	77.04	3- 64
BD 440, 442										3- 64
BD 533, 535, 537	General Purpose	4	15-20	10	5	50	45-80	NPN	TO220	3- 67
BD 534, 536, 538	General Purpose	4	15-20	10	5	50	45-80	PNP	TO220	3- 67
BD 675, 677, 679, 681	General Purpose Darlington	4	750	1.5	3	40	45-100	NPN	77.04	3- 71
BD 676, 678, 680, 682	General Purpose Darlington	4	750	1.5	3	40	45-100	PNP	77.04	3- 73
BD 785, 787	Switch and Amplifier	4	40	0.2	3	15	45-60	NPN	77.04	3- 75
BD 786, 788	Switch and Amplifier	4	40	0.2	3	15	45-60	PNP	77.04	3- 75
BD 789, 791	High Speed Switching and Audio	4	40	0.2	3	15	80-100	NPN	77.04	3- 79
BD 790, 792	High Speed Switching and Audio	4	40	0.2	3	15	80-100	PNP	77.04	3- 79
MJE 700T, 703T	General Purpose	4	750	1.5(2)	3	40-50	60-80	PNP	TO220	3-184
MJE 800T, 803T	General Purpose	4	750	1.5(2)	3	40-50	60-80	NPN	TO220	3-184
MJE 8502, 8503	Power Switching	5	7.5	1	5	80	700-800	NPN	TO220	3-199
BD 243	Switching and Amplifier	6	30	0.3	4	65	45-100	NPN	TO-220	3- 32
BD 244	Switching and Amplifier	6	30	0.3	4	65	45-100	PNP	TO-220	3- 32
BU 406, 407	TV Horizontal Deflection	7	-	-	-	60	150-200	NPN	TO-220	3-143
BD 795, 797, 799, 801	Audio Amplifier, General	8	30/40	1	2	65	45-100	NPN	TO-220	3- 83
BD 796, 798, 800, 802	Audio Amplifier, General	8	30/40	1	2	65	45-100	PNP	TO-220	3- 85
BD 895, 897, 899, 901	General Purpose Darlington	8	750	3	3	70	45-100	NPN	TO-220	3- 91
BD 896, 898, 900, 902	General Purpose Darlington	8	750	3	3	70	45-100	PNP	TO-220	3- 93
BDX 53	General Purpose Darlington	8	750	3	3	60	60-100	NPN	TO 220	3-109
BDX 54	General Purpose Darlington	8	750	3	3	60	60-100	PNP	TO-220	3-109
MJE 15028, 15030	Audio Amplifier HF Driver	8	40	0.1	2	50	120-150	NPN	TO-220	3-213
MJE 15029, 15031	Audio Amplifier HF Driver	8	40	0.1	2	50	120-150	PNP	TO-220	3-213
BD 805, 807, 809	High Power Audio Amplifier	10	30	2	2	90	45-80	NPN	TO-220	3- 87
BD 806, 808, 810	High Power Audio Amplifier	10	30	2	2	90	45-80	PNP	TO-220	3- 89
BDV 64, 64A, 64B	General Purpose	10	1000	5	4	125	60-100	NPN	340	3- 95
BDV 65, 65A, 65B	General Purpose	10	1000	5	4	125	60-100	PNP	340	3- 95
BDX 33	General Purpose	10	750	4(3)	3	70	45-100	NPN	TO-220	3-105
BDX 34	General Purpose	10	750	4(3)	3	70	45-100	PNP	TO-220	3-105
MJE 2955, 2955T	General Purpose	10	20	4	4	75/90	60	PNP	90/TO-220	3-189
MJE 3055, 3055T	General Purpose	10	20	4	4	75/90	60	NPN	90/TO-220	3-191
BDW 39, 40, 41, 42	General Purpose	15	1000	5	4	85	45-100	NPN	TO-220	3- 99
BDW 44, 45, 46, 47	General Purpose	15	1000	5	4	85	45-100	PNP	TO-220	3- 99
2N 6486, 6487	General Purpose	15	20	5	4	75	40-80	NPN	TO-220	3-242
2N 6488										3-242
2N 6489, 6490	General Purpose	15	20	5	4	75	40-80	PNP	TO-220	3-242
2N 6491										3-242

POWER TRANSISTORS CONTINUED

Power Metal Transistors (in order I_C max.)

Device	Designation	I_C (cont.) A	H_{FE} @ → I_C → (min.)	A	V_{CE} V	P_D W	V_{CEO} V	Polarity	Package	Page
MJ8500, 8501	Power Switching	2.5	7.5	0.5	5	125	700-800	NPN	TO3	3-168
BU208, 208A	TV Horizontal Deflection		2.25	4.5	5	20	700	NPN	11.03	3-129
BU208D	TV Horizontal Deflection	5	–	–	–	60	700	NPN	TO3	3-134
MJ8502, 8503	Power Switching	5	7.5	1	5	150	700-800	NPN	TO3	3-174
BU326, 326 A	Switch Mode Power Supplies	6	30	0.6	5	90	375-400	NPN	1.05	3-140
MJ900, 901	Amplifier Output Darlington	8	1000	3	3	90	60-80	PNP	11.01	3-158
MJ1000, 1001		8	1000	3	3	90	60-80	NPN	11.01	3-158
BD311, 313	Audio Amplifier Output	10	25	5	4	115	60-80	NPN	11	3- 36
BD312, 314		10	25	5	4	115	60-80	PNP	11	3- 36
BU323, 323A	Switching and Control	10	50	10	6	175	350-600	NPN	1.05	3-136
MJ2500, 2501	Amplifier Darlington	10	1000	5	3	150	60-80	PNP	11.01	3-160
MJ3000, 3001		10	1000	5	3	150	60-80	NPN	11.01	3-160
MJ15011	Power Switching	10	20	2	2	200	250	NPN	11.01	3-205
MJ15012	Power Switching	10	20	2	2	200	250	PNP	11.01	3-205
MJ2955	Switching and Amplifier	15	20	4	4		60	PNP	11.01	3-162
BD315, 317	Audio Amplifier Output	16	15	10	4	200	80-100	NPN	11	3- 42
BD316, 318		16	15	10	4	200	80-100	PNP	11	3-166
MJ4030, 4031	General Purpose Amplifier O/P	16	1000	10	3	150	60-100	PNP	11.01	3-166
MJ4032										
MJ4033, 4034	General Purpose Amplifier O/P	16	1000	10	3	150	60-100	NPN	11.01	3-166
MJ4035										
MJ15022,15024	High Power Audio	16	15	8	4	250	200-250	NPN	11.01	3-166
MJ15023, 15025	High Power Audio	16	15	8	4	250	200-250	PNP	11.01	3-207
2N3773	High Power Audio, Switching	16	15	8	4	150	140	NPN	11.01	3-210
2N6609		16	15	8	4	150	140	PNP	11.01	3-237
BU205	TV Horizontal Deflection	25	2	2	5	175	700	NPN	11	3-126
MJ802	Audio Amplifier Output	30	25	7.5	2	200	90	NPN	11.01	3-156

Uniwatt and Duowatt Transistors

Device	Designation	I_C (cont.) A	H_{FE} @ → I_C → (min.)	mA	V_{CE} V	P_D W	V_{CEO} V	Polarity	Package	Page
BD385, 387, 389	General Purpose	1	80	50	1	2	60-100	NPN	306.04	3- 45
BD386, 388, 390		1	80	50	1	2	60-100	PNP	306.04	3- 49
BD411, 412	Amplifier and Driver Darlington	2	15, 25K	200	5	2	40	NPN	306.04	3- 53
BD413, 414		2	15, 25K	200	5	2	40	PNP	306.04	3- 57
BF466, 467, 468	TV Horizontal Deflection Driver	1	40	10	10	2	150-250	NPN	306.04	3-114
BF757, 758, 759	TV Video and Chroma Output	0.5	40	30	10	2	250-350	NPN	306.04	3-118
BF760, 761, 762		0.5	40	30	10	2	250-350	PNP	306.04	3-122

Power MOS (Power Switching)

Device	Continuous current I_D (Amps)	Breakdown voltage $V_{(BR)DSS}$ (Volts)	Drain-Source on resistance $r_{DS(on)}$ max. (Ohms)	@ I_D (Amps)	Trans-conductance g_{fs} min. (Mhos)	@ I_D (Amps)	Gate Threshold Voltage $V_{GS(th)}$ @ I_D = 1 mA min/max (Volts)	Resistive Switching max. @ T_J = 100° C t_{on} (ns)	t_{of} (ns)	I_D (Amps)	Package	Page
MTM475	4	500	2.25	2.0	1.5	2.0	1.5/4.0	150	300	2.0	TO-3	3-215
MTP475											TO-220	3-215
MTM474		450									TO-3	3-215
MTP474											TO-220	3-215
MTM565	5	400	1.5	2.5	2.0	2.5				2.5	TO-3	3-221
MTP565											TO-220	3-221
MTM564		350									TO-3	3-221
MTP564											TO-220	3-221
MTM1225	12	100	0.25	6.0	3.0	6.0				6.0	TO-3	3-227
MTP1225											TO-220	3-227
MTM1224		60									TO-3	3-227
MTP1224											TO-220	3-227

BD135, -6, -10, -16
BD137, -6, -10, -16
BD139, -6, -10, -16

PLASTIC MEDIUM POWER
SILICON NPN TRANSISTOR

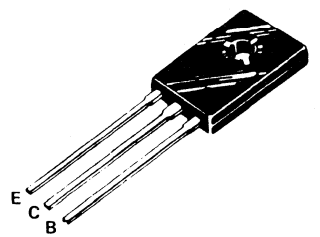
. . . designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- Available in H_{FE} groups -6, -10, -16
- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 135, 137, 139 are complementary with BD 136, 138, 140

1.5 AMPERE
POWER TRANSISTOR

NPN SILICON

45, 60, 80 VOLTS
10 WATTS



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 135 BD 137 BD 139	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 135 BD 137 BD 139	45 60 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		1.5	Adc
Base Current	I_B		0.5	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D		1.25 10	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		12.5 100	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−55 to +150	°C

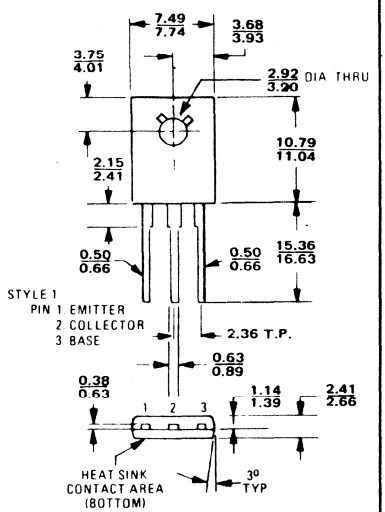
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	10	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	100	°C/W

ELECTRICAL CHARACTERISTICS (T_C 25 C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.03 Adc, I_B = 0)	BV_{CEO}*	BD 135 BD 137 BD 139	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0) (V_{CB} = 30 Vdc, I_E = 0, T_C = 125° C)	I_{CBO}		— — —	0.1 10	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	10	μAdc
DC Current Gain (I_C = 0.005A, V_{CE} = 2 V) (I_C = 0.15A, V_{CE} = 2 V) (I_C = 0.5A V_{CE} = 2 V)	h_{FE}*		25 40 25	— 250 —	—
Collector-Emitter Saturation Voltage* (I_C = 0.5 Adc, I_B = 0.05 Adc)	$V_{CE(sat)}$*		—	0.5	Vdc
Base-Emitter On Voltage* (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1	Vdc

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%



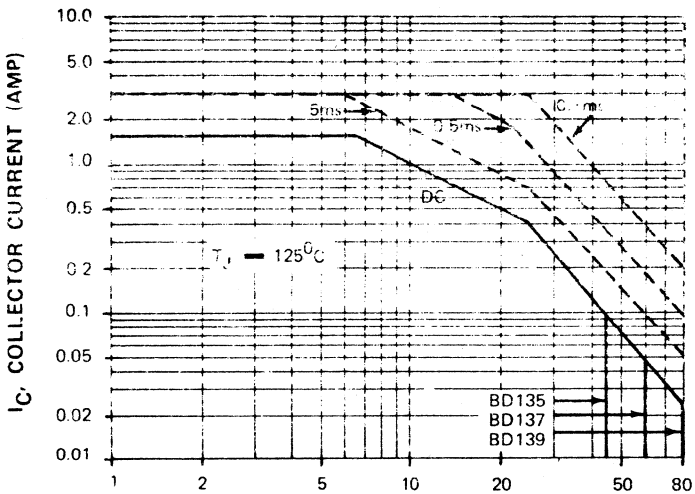
When mounting the device, torque not to exceed 0.07 m-kg

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend

All dimensions in millimeters

CASE 77-04

FIGURE 1 – ACTIVE REGION SAFE OPERATING AREA



		Min.	Max.
Available in H_{FE} groups (At I_C = 0.15 A, V_{CE} = 2 V) H_{FE} group:	-6	40	100
	-10	63	160
	-16	100	250

3

BD136, -6, -10, -16
BD138, -6, -10, -16
BD140, -6, -10, -16

PLASTIC MEDIUM POWER
SILICON PNP TRANSISTOR

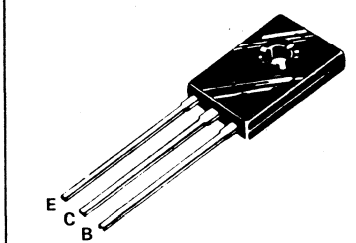
. . . designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- Available in H_{FE} groups -6, -10, -16
- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 136, 138, 140 are complementary with BD 135, 137, 139

1.5 AMPERE
POWER TRANSISTOR

PNP SILICON

45, 60, 80 VOLTS
10 WATTS



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 136 BD 138 BD 140	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 136 BD 138 BD 140	45 60 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		1.5	Adc
Base Current	I_B		0.5	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D		1.25 10	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		12.5 100	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−55 to +150	°C

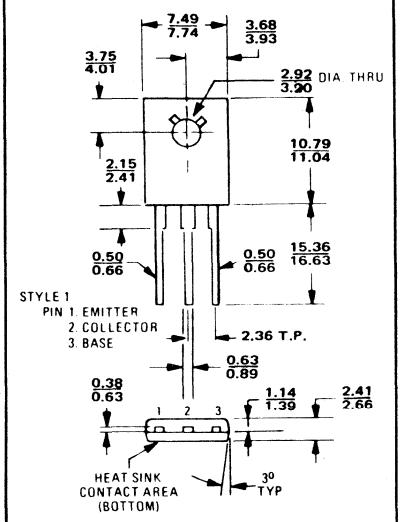
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	10	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	100	°C/W

ELECTRICAL CHARACTERISTICS (T_C 25 C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.03 Adc, I_B = 0)	BV_{CEO}*	BD 136 BD 138 BD 140	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0) (V_{CB} = 30 Vdc, I_E = 0, T_C = 125° C)	I_{CBO}		— — —	0.1 10	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	10	μAdc
DC Current Gain (I_C = 0.005A, V_{CE} = 2 V) (I_C = 0.15A, V_{CE} = 2 V) (I_C = 0.5A, V_{CE} = 2 V)	h_{FE}*		25 40 25	— 250 —	—
Collector-Emitter Saturation Voltage* (I_C = 0.5 Adc, I_B = 0.05 Adc)	$V_{CE(sat)}$*		—	0.5	Vdc
Base-Emitter On Voltage* (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1	Vdc

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



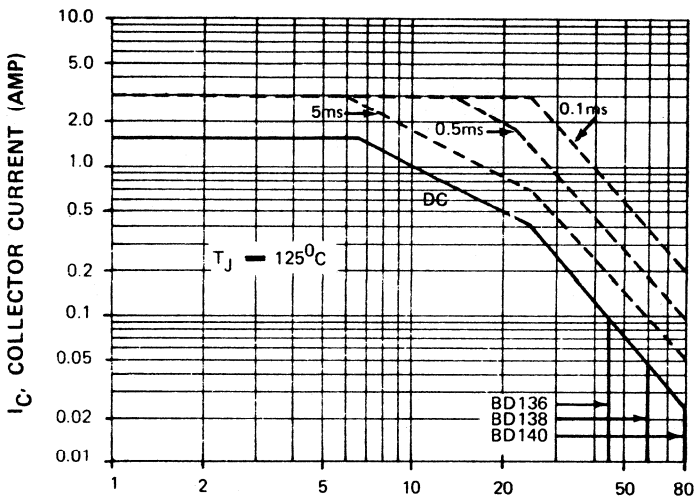
When mounting the device, torque not to exceed 0.07 m-kg

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

All dimensions in millimeters

CASE 77-04

FIGURE 1 – ACTIVE REGION SAFE OPERATING AREA



Available in H_{FE} groups (at I_C = 0.15 A, V_{CE} 2 V) H_{FE} group:		Min.	Max.
	-6	40	100
	-10	63	160
	-16	100	250

3

BD 165
BD 167
BD 169

PLASTIC MEDIUM POWER
SILICON NPN TRANSISTOR

. . . designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

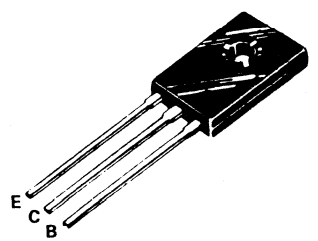
- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 165, 167, 169 are complementary with BD 166, 168, 170

1.5 AMPERE
POWER TRANSISTOR

NPN SILICON

45, 60, 80 VOLTS
20 WATTS

DECEMBER 1971 – E-038R1



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 165 BD 167 BD 169	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 165 BD 167 BD 169	45 60 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		1.5	Adc
Base Current	I_B		0.5	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D		1.25 8	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		20 160	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−65 to +150	°C

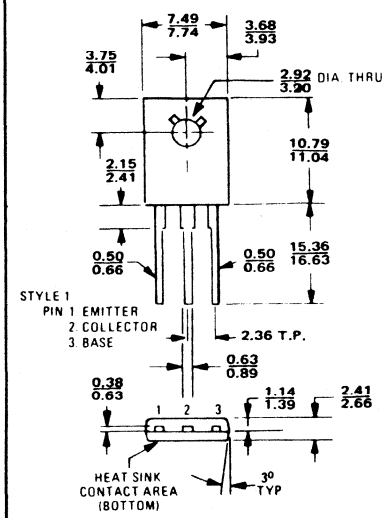
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	100	°C/W

ELECTRICAL CHARACTERISTICS (T_C 25 C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}*	BD 165 BD 167 BD 169	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	BD 165 BD 167 BD 169	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 0.15 A, V_{CE} = 2 V) (I_C = 0.5 A, V_{CE} = 2 V)	h_{FE}*		40 15	— —	
Collector-Emitter Saturation Voltage* (I_C = 0.5 Adc, I_B = 0.05 Adc)	$V_{CE(sat)}$*		—	0.5	Vdc
Base-Emitter On Voltage* (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	0.95	Vdc
Current-Gain-Bandwidth Product (I_C = 500 mAdc, V_{CE} = 2 Vdc, f = 1.0 MHz)	f_T		6.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



When mounting the device, torque not to exceed 0.07 m-kg

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend

All dimensions in millimeters

CASE 77-04

FIGURE 1 – P_n–T_c DERATING CURVE

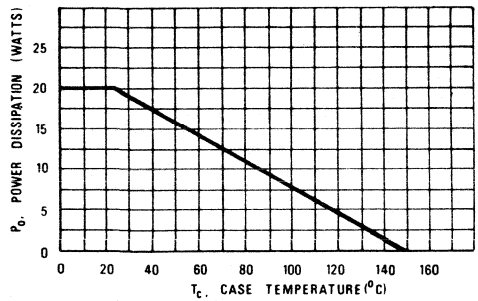
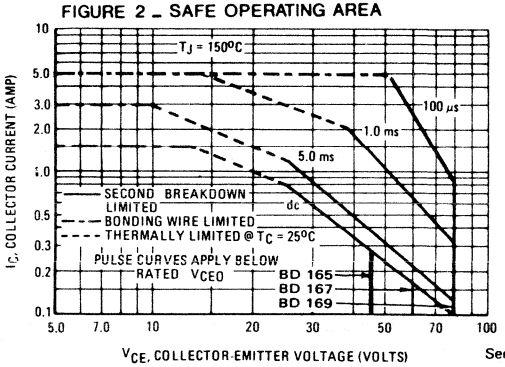


FIGURE 2 – SAFE OPERATING AREA



See Note 1

FIGURE 3 – COLLECTOR SATURATION REGION

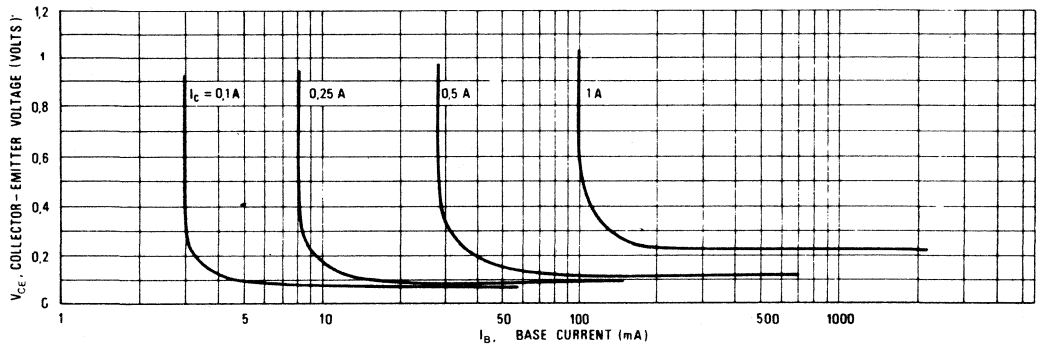


FIGURE 4 – CURRENT GAIN

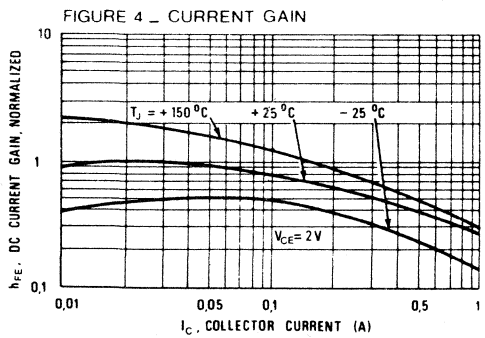
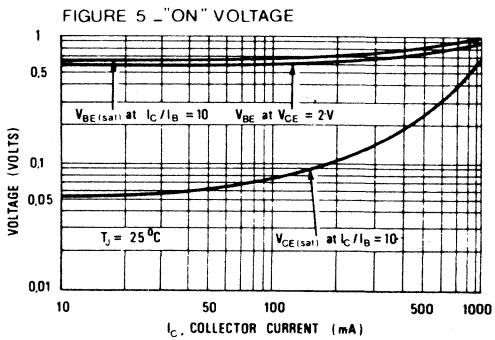


FIGURE 5 – "ON" VOLTAGE



Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ ≤150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

3

BD 166
BD 168
BD 170

PLASTIC MEDIUM POWER SILICON PNP TRANSISTOR

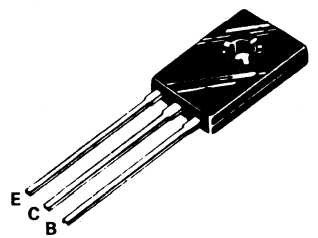
. . . designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 166, 168, 170 are complementary with BD 165, 167, 169

1.5 AMPERE POWER TRANSISTOR

PNP SILICON

45, 60, 80 VOLTS
20 WATTS



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 166 BD 168 BD 170	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 166 BD 168 BD 170	45 60 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		1.5	Adc
Base Current	I_B		0.5	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D		1.25 10	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		20 160	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−65 to +150	°C

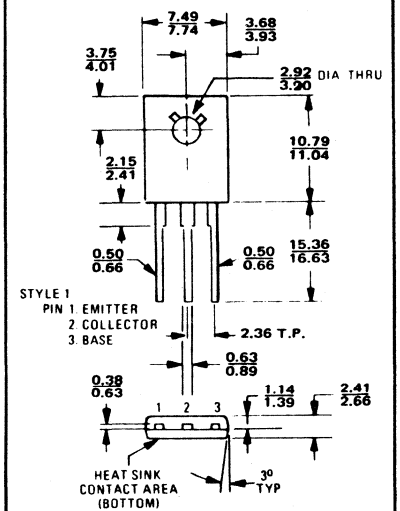
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	100	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}	BD 166 BD 168 BD 170	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	BD 166 BD 168 BD 170	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 0.15 A, V_{CE} = 2 V) (I_C = 0.5 A, V_{CE} = 2 V)	h_{FE}*		40 15	— —	
Collector-Emitter Saturation Voltage* (I_C = 0.5 Adc, I_B = 0.05 Adc)	$V_{CE(sat)}$		—	0.5	Vdc
Base-Emitter On Voltage* (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$		—	0.95	Vdc
Current-Gain-Bandwidth Product (I_C = 500 mAdc, V_{CE} = 2 Vdc, f = 1.0 MHz)	f_T		6.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



When mounting the device, torque not to exceed 0.07 m-kg

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

All dimensions in millimeters

CASE 77-04

FIGURE 1 – P_D–T_C DERATING CURVE

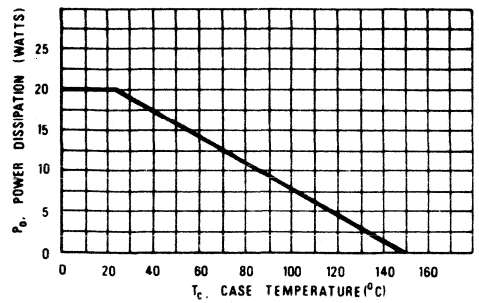
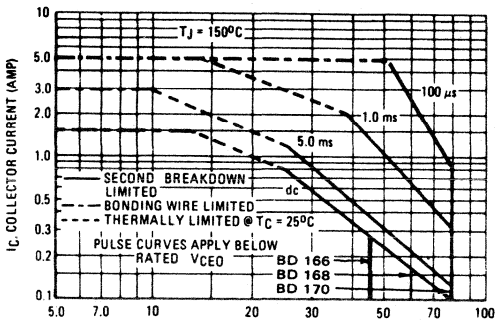


FIGURE 2 – SAFE OPERATING AREA



See Note 1

FIGURE 3 – COLLECTOR SATURATION REGION

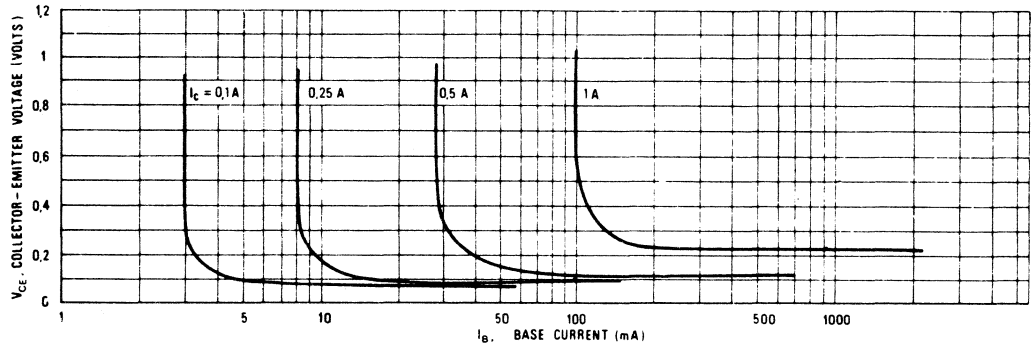


FIGURE 4 – CURRENT GAIN

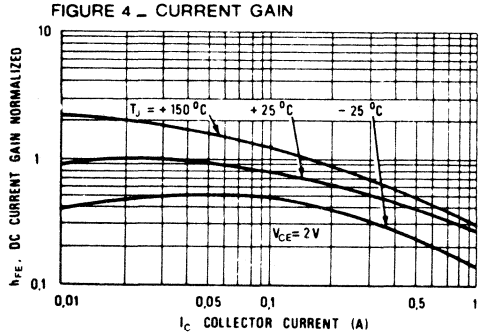
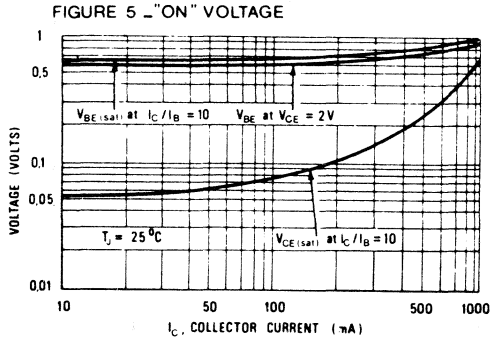


FIGURE 5 – "ON" VOLTAGE



Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

BD175,-6,-10,-16
BD177,-6,-10
BD179,-6,-10

PLASTIC MEDIUM POWER
SILICON NPN TRANSISTOR

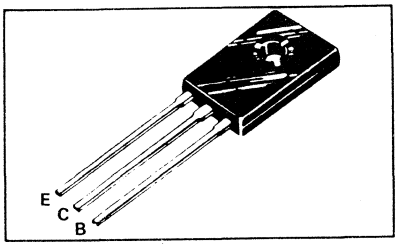
. . . designed for use in 5 to 10 Watt audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 175, 177, 179 are complementary with BD 176, 178, 180
- Available in H_{FE} groups -6, -10, -16

3 AMPERE
POWER TRANSISTOR

NPN SILICON

45, 60, 80 VOLTS
30 WATTS



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 175 BD 177 BD 179	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 175 BD 177 BD 179	45 60 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		3.0	Adc
Base Current	I_B		1.0	Adc
Total Device Dissipation T_C=25°C Derate above 25°C	P_D		30 240	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		—65 to +150	°C

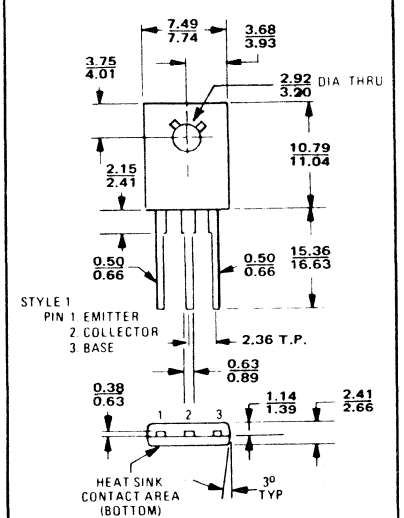
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		4.16	° C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}*	BD 175 BD 177 BD 179	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	BD 175 BD 177 BD 179	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 0.15 A, V_{CE} = 2 V) group -6 group -10 group -16 (I_C = 1 A, V_{CE} = 2 V)	h_{FE}*		40 63 100 15	100 160 250	
Collector-Emitter Saturation Voltage* (I_C = 1 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$*		—	0.8	Vdc
Base-Emitter On Voltage* (I_C = 1 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.3	Vdc
Current-Gain-Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		3.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



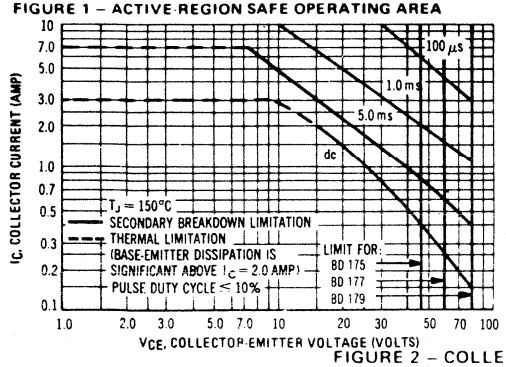
When mounting the device, torque not to exceed 0.07 m-kg

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend

All dimensions in millimeters

CASE 77-04

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – COLLECTOR SATURATION REGION

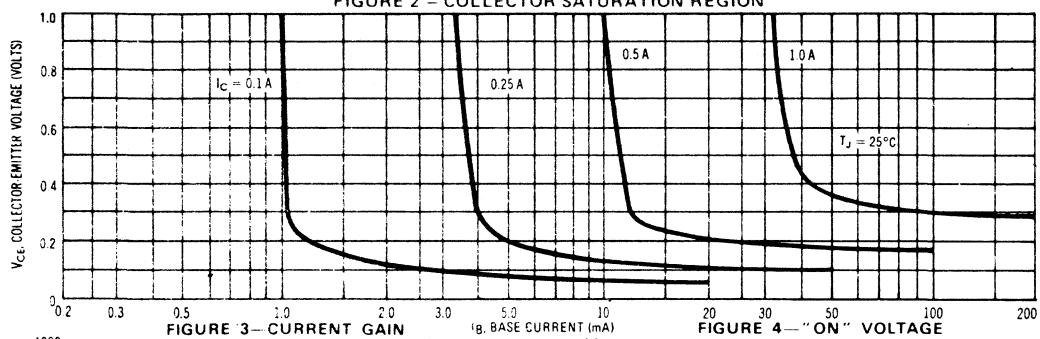


FIGURE 3 – CURRENT GAIN

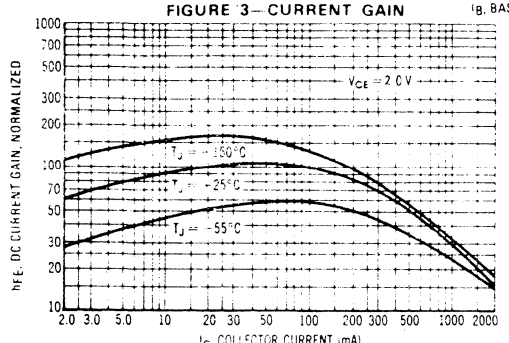


FIGURE 4 – "ON" VOLTAGE

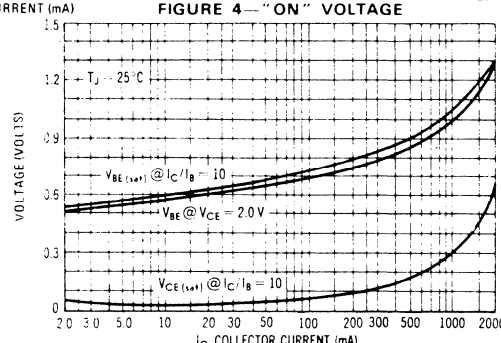
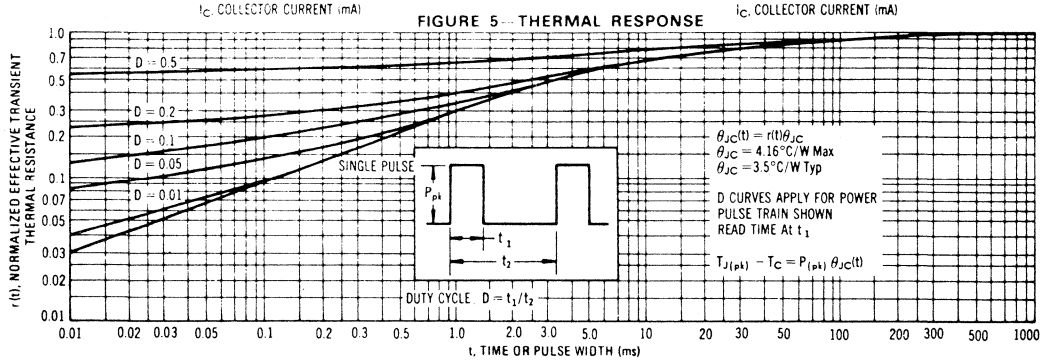


FIGURE 5 – THERMAL RESPONSE



3

BD 176,-6,-10,-16
BD178,-6,-10
BD180,-6,-10

PLASTIC MEDIUM POWER
SILICON PNP TRANSISTOR

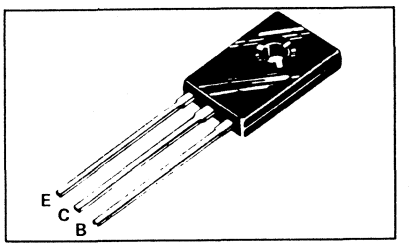
. . . designed for use in 5 to 10 Watt audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 176, 178, 180 are complementary with BD 175, 177, 179
- Available in H_{FE} groups -6, -10, -16

3 AMPERE
POWER TRANSISTOR

PNP SILICON

45, 60, 80 VOLTS
30 WATTS



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 176 BD 178 BD 180	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 176 BD 178 BD 180	45 60 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		3.0	Adc
Base Current	I_B		1.0	Adc
Total Device Dissipation T_C=25°C Derate above 25°C	P_D		30 240	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−65 to +150	°C

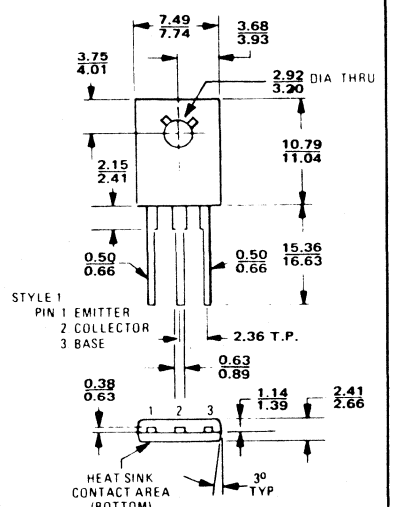
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		4.16	° C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}*	BD 176 BD 178 BD 180	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	BD 176 BD 178 BD 180	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC Current Gain (I_C = 0.15 A, V_{CE} = 2 V) group -6 group -10 group -16 (I_C = 1 A, V_{CE} = 2 V)	h_{FE}*		40 63 100 15	100 160 250	
Collector-Emitter Saturation Voltage* (I_C = 1 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$*		—	0.8	Vdc
Base-Emitter On Voltage* (I_C = 1 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.3	Vdc
Current-Gain-Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		3.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



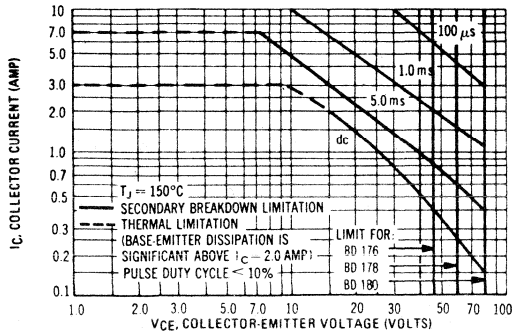
When mounting the device, torque not to exceed 0.07 m-kg

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend

All dimensions in millimeters

CASE 77-04

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – COLLECTOR SATURATION REGION

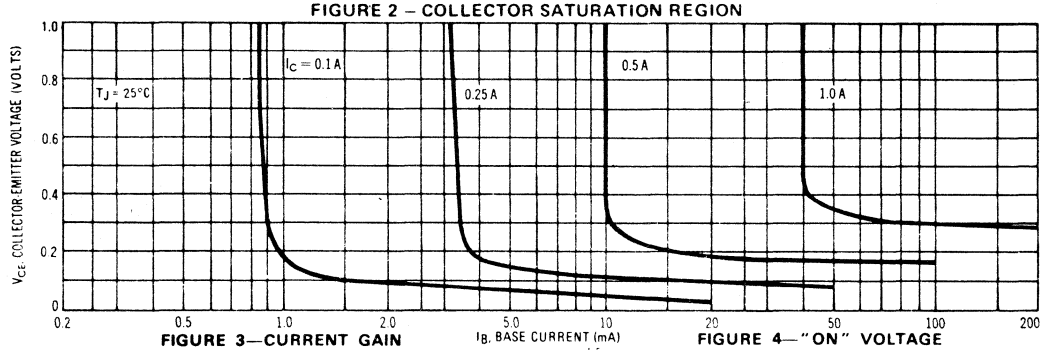


FIGURE 3—CURRENT GAIN

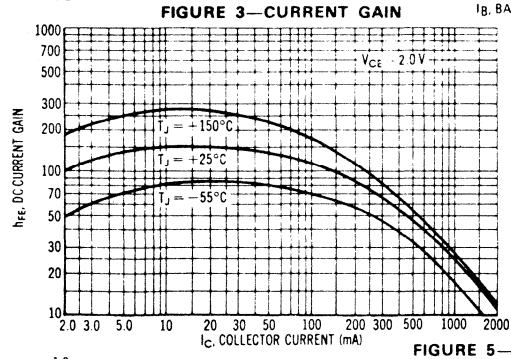


FIGURE 4—"ON" VOLTAGE

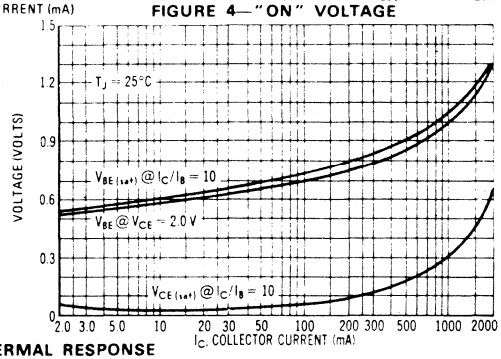
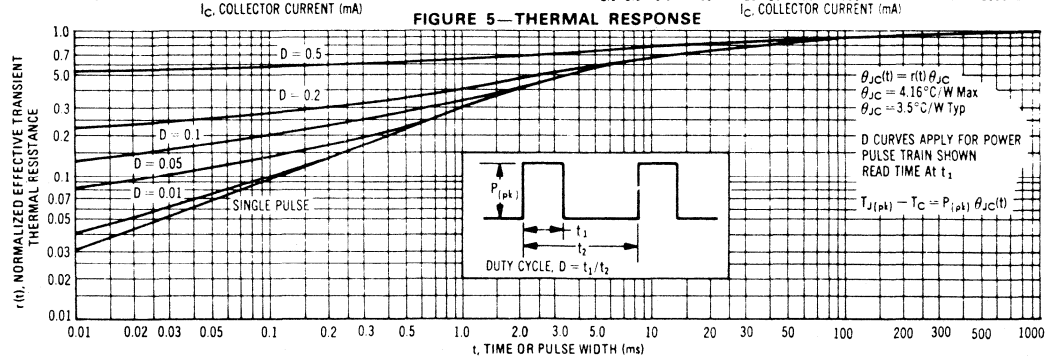


FIGURE 5—THERMAL RESPONSE



BD 185
BD 187
BD 189

PLASTIC MEDIUM POWER
SILICON NPN TRANSISTOR

. . . designed for use in 5 to 10 Watt audio amplifiers utilizing complementary or quasi complementary circuits.

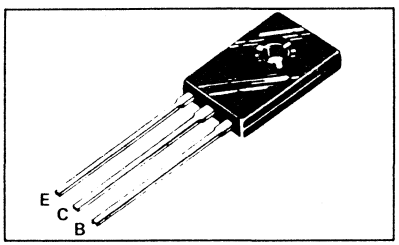
- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 0.5 Adc
- BD 185, 187, 189 are complementary with BD 186, 188, 190

4 AMPERE
POWER TRANSISTOR

NPN SILICON

30, 45, 60 VOLTS
40 WATTS

MARCH 1970—E-003



MAXIMUM RANGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 185 BD 187 BD 189	30 45 60	Vdc
Collector-Base Voltage	V_{CBO}	BD 185 BD 187 BD 189	40 55 70	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		4.0	Adc
Base Current	I_B		2.0	Adc
Total Device Dissipation T_C=25°C Derate above 25°C	P_D		40 320	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		—65 to +150	°C

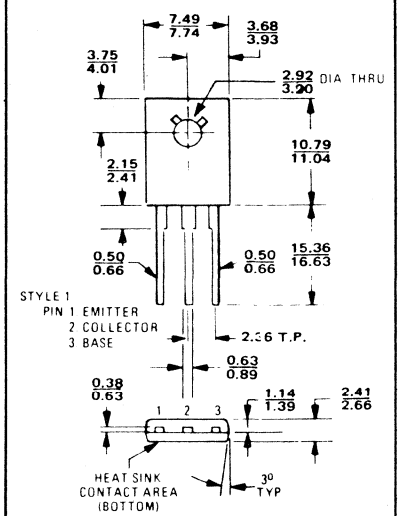
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		3.12	° C/W

ELECTRICAL CHARACTERISTICS (T_c = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}*	BD 185 BD 187 BD 189	30 45 60	— — —	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 55 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0)	I_{CBO}	BD 185 BD 187 BD 189	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 0.5 A, V_{CE} = 2 V) (I_C = 2A, V_{CE} = 2 V)	h_{FE}*		40 15	— —	
Collector-Emitter Saturation Voltage* (I_C = 2Adc, I_B = 0.2 Adc)	$V_{CE(sat)}$*		—	1.0	Vdc
Base-Emitter On Voltage* (I_C = 2Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.5	Vdc
Current-Gain-Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		2.0	—	MHz

* Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0%.



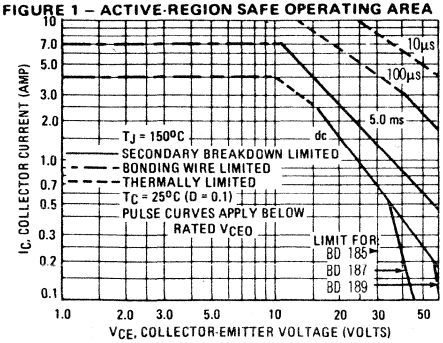
When mounting the device, torque not to exceed 0.07 m-kg.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

All dimensions in millimeters.

CASE 77-04

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – COLLECTOR SATURATION REGION

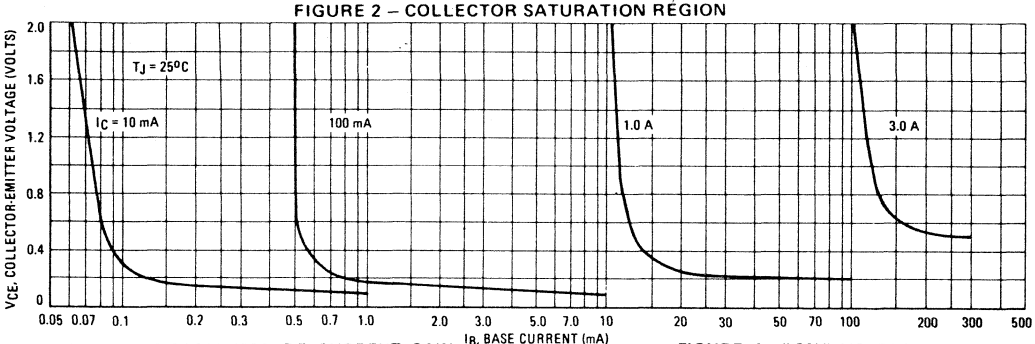


FIGURE 3—NORMALIZED DE CURRENT GAIN

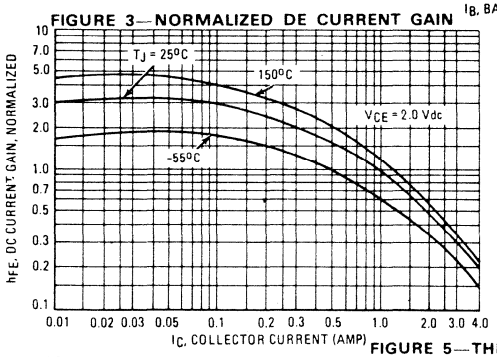


FIGURE 4—"ON" VOLTAGE

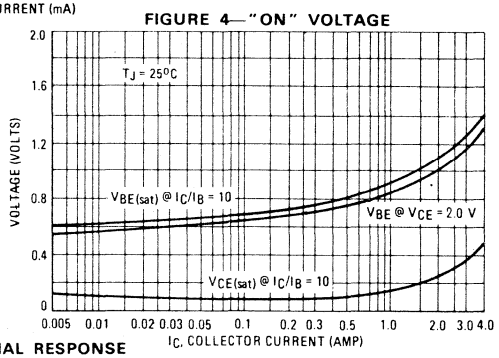
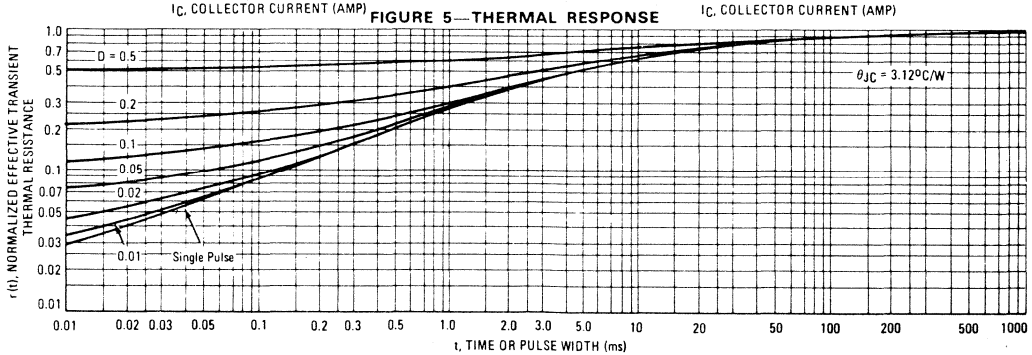


FIGURE 5—THERMAL RESPONSE



3

BD 186
BD 188
BD 190

PLASTIC MEDIUM POWER
SILICON PNP TRANSISTOR

. . . designed for use in 5 to 10 Watt audio amplifiers utilizing complementary or quasi complementary circuits.

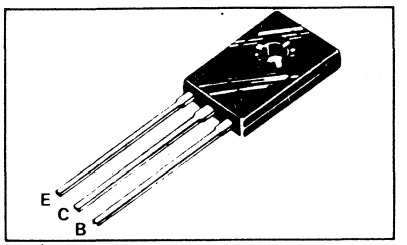
- DC Current—h_{FE} = 40 (Min) @ I_C = 0.5 Adc
- BD 186, 188, 190 are complementary with BD 185, 187, 189

4 AMPERE
POWER TRANSISTOR

PNP SILICON

30, 45, 60 VOLTS
40 WATTS

MARCH 1970—E-005



MAXIMUM RANGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 186 BD 188 BD 190	30 45 60	Vdc
Collector-Base Voltage	V_{CBO}	BD 186 BD 188 BD 190	40 55 70	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		4.0	Adc
Base Current	I_B		2.0	Adc
Total Device Dissipation T_C=25°C Derate above 25°C	P_D		40 320	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		—65 to +150	°C

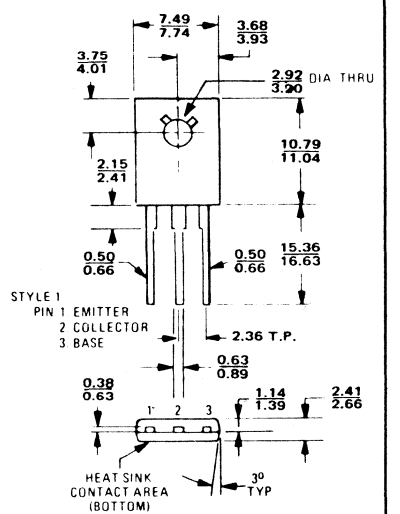
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		3.12	° C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}*	BD 186 BD 188 BD 190	30 45 60	— — —	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 55 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0)	I_{CBO}	BD 186 BD 188 BD 190	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 0.5 A, V_{CE} = 2 V) (I_C = 2 A, V_{CE} = 2 V)	h_{FE}*		40 15	— —	
Collector-Emitter Saturation Voltage* (I_C = 2.0 Adc, I_B = 0.2 Adc)	$V_{CE(sat)}$*		—	1.0	Vdc
Base-Emitter On Voltage* (I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.5	Vdc
Current-Gain-Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		2.0	—	MHz

* Pulse Test: Pulse Width ≦ 300 μs. Duty Cycle ≦ 2.0%.



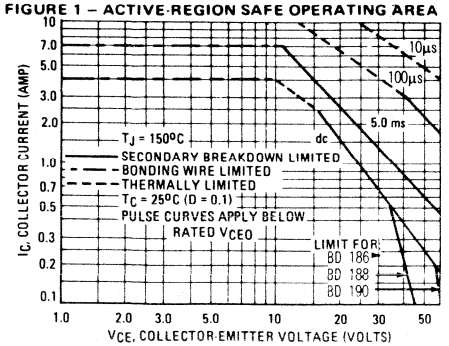
When mounting the device, torque not to exceed 0.07 m-kg

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend

All dimensions in millimeters

CASE 77-04

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – COLLECTOR SATURATION REGION

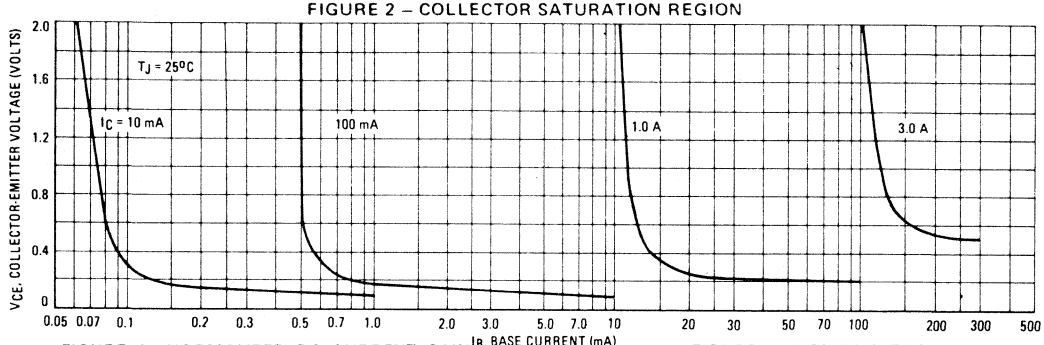


FIGURE 3—NORMALIZED DC CURRENT GAIN

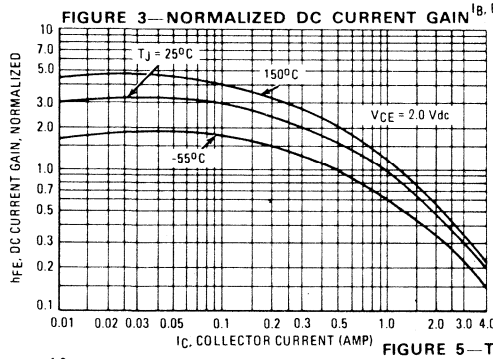


FIGURE 4—"ON" VOLTAGE

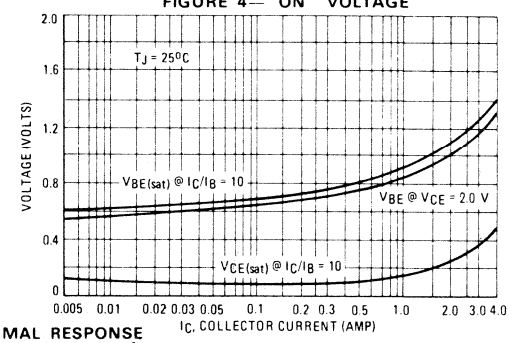
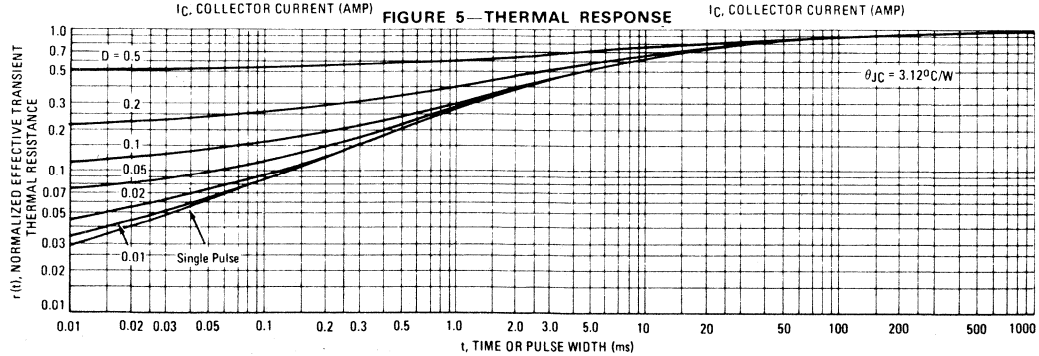


FIGURE 5—THERMAL RESPONSE



3

BD232

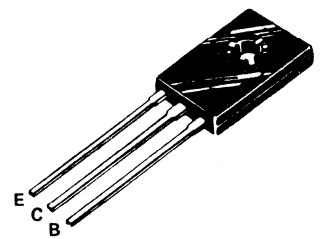
NPN SILICON MEDIUM POWER TRANSISTORS

- For Power Ouput Stages and Line Driver in Television Receivers

0.5 AMPERES

NPN SILICON POWER TRANSISTOR

300 VOLTS
20 WATTS



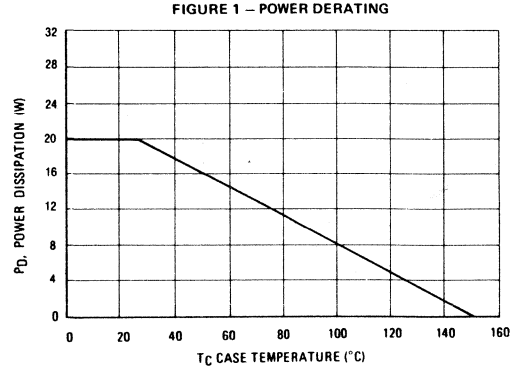
MAXIMUM RATINGS

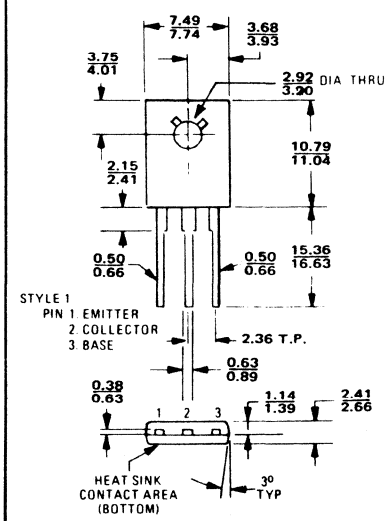
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	300	Vdc
Collector-Emitter Voltage	V_{CES}	500	Vdc
Emitter-Base Voltage	V_{EBO}	5	Vdc
Collector Current – Continuous	I_C	0.5	Adc
Base Current	I_B	0.25	Adc
Total Device Dissipation @ $T_c = 25^oC$ Derate above 25^oC	P_D	20 160	Watts W/^oC
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to 150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W

FIGURE 1 – POWER DERATING





When mounting the device, torque not to exceed 0.07 m-kg

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend

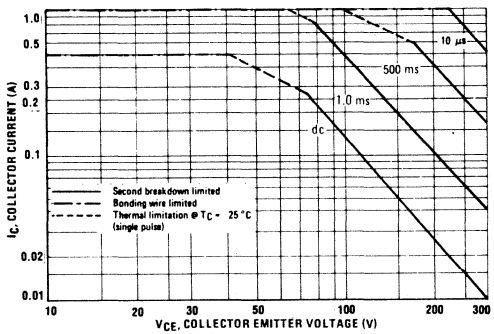
All dimensions in millimeters

CASE 77-04

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS (1)				
Collector-Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	300	–	Vdc
Collector Cutoff Current (V_{CE} = 500 Vdc, V_{BE} = 0)	I_{CES}	–	0.1	mAdc
Base-Emitter Voltage (V_{CE} = 5 Vdc, I_C = 150 mA)	V_{BE}	–	1.0	Vdc
DC Current Gain (V_{CE} = 5 V, I_C = 50 mA) (V_{CE} = 5 V, I_C = 150 mA)	h_{FE}	25 20	150	
Collector Emitter Saturation Voltage (I_C = 150 mA, I_B = 15 mA)	$V_{CE(sat)}$	–	1.0	Vdc

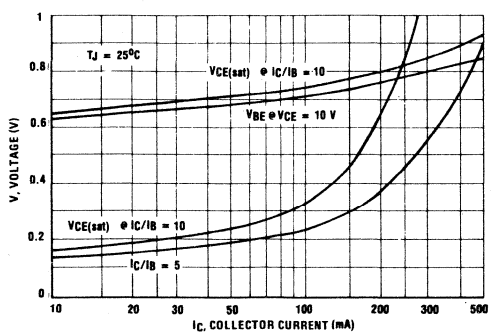
FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 6 is based on $T_{J(pk)}$ = 150°C, T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in figure 7. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A)

FIGURE 3 – "ON" VOLTAGES



BD 233
BD 235
BD 237

PLASTIC MEDIUM POWER
SILICON NPN TRANSISTOR

. . . designed for use in 5 to 10 Watt audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

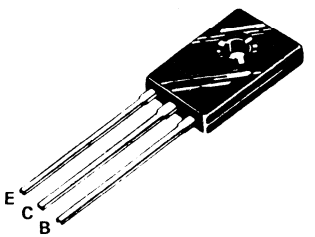
- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 233, 235, 237 are complementary with BD 234, 236, 238

2 AMPERE
POWER TRANSISTOR

NPN SILICON

45, 60, 80 VOLTS
25 WATTS

DECEMBER 1971 – E - 061



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 233 BD 235 BD 237	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 233 BD 235 BD 237	45 60 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		2.0	Adc
Base Current	I_B		1.0	Adc
Total Device Dissipation T_C=25°C	P_D		25	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}		55 to +150	°C

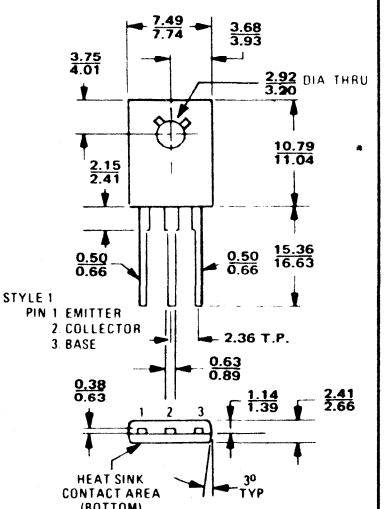
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		5 0	° C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}	BD 233 BD 235 BD 237	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	BD 233 BD 235 BD 237	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 0.15 A, V_{CE} = 2 V) (I_C = 1 A, V_{CE} = 2 V)	h_{FE1} h_{FE2}		40 25	— —	
Collector-Emitter Saturation Voltage* (I_C = 1 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$*		—	0.6	Vdc
Base-Emitter On Voltage* (I_C = 1 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.3	Vdc
Current-Gain-Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		3.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



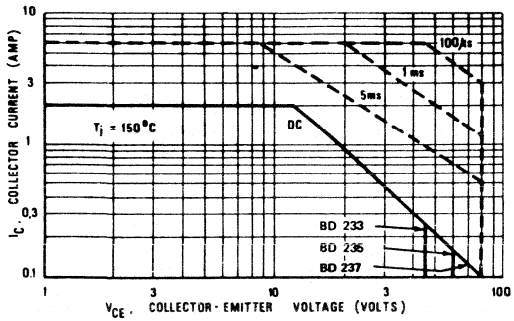
When mounting the device, torque not to exceed 0.07 m-kg

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend

All dimensions in millimeters

CASE 77-04

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catestrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – COLLECTOR SATURATION REGION

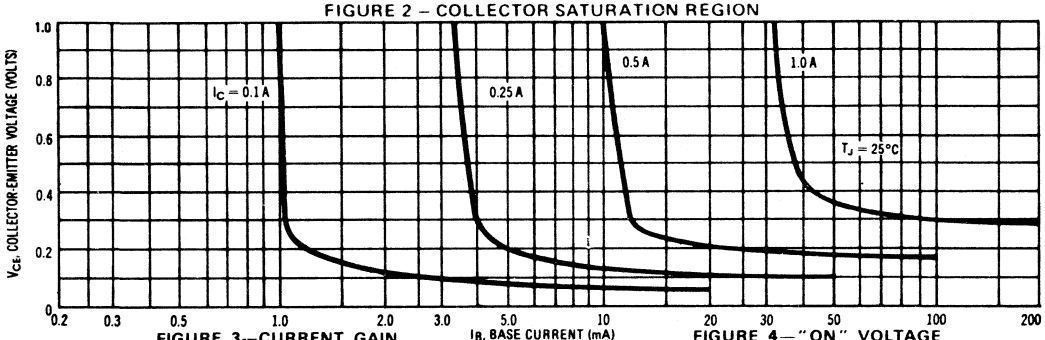


FIGURE 3—CURRENT GAIN

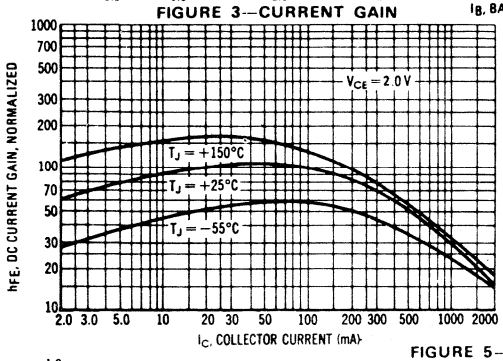


FIGURE 4—"ON" VOLTAGE

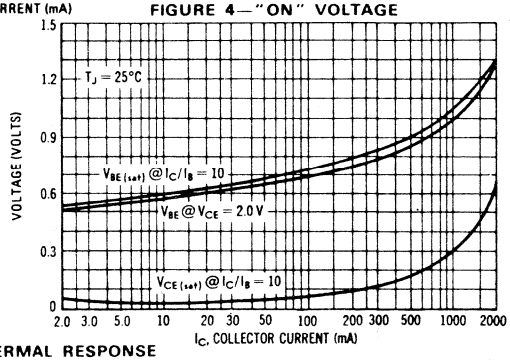
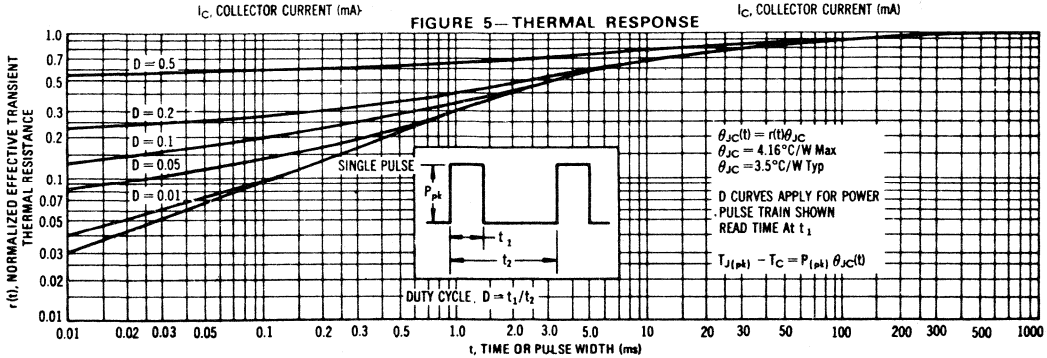


FIGURE 5—THERMAL RESPONSE



3

BD 234
BD 236
BD 238

PLASTIC MEDIUM POWER
SILICON PNP TRANSISTOR

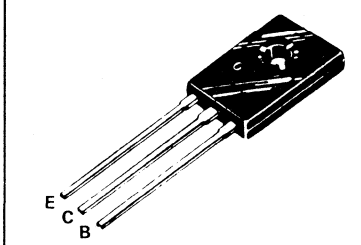
designed for use in 5 to 10 Watt audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 234, 236, 238 are complementary with BD 233, 235, 237

2 AMPERE
POWER TRANSISTOR

PNP SILICON

45, 60, 80 VOLTS
25 WATTS



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 234 BD 236 BD 238	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 234 BD 236 BD 238	45 60 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		2.0	Adc
Base Current	I_B		1.0	Adc
Total Device Dissipation T_C=25°C	P_D		25	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}		—55 to +150	°C

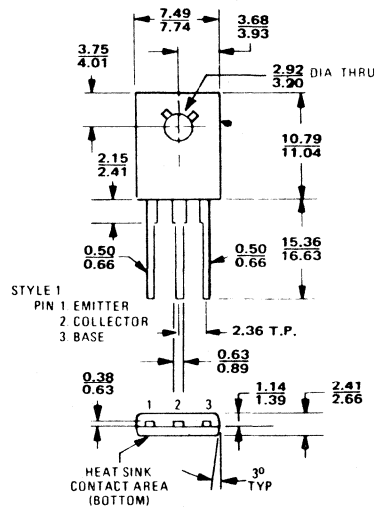
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		5.0	° C/W

ELECTRICAL CHARACTERISTICS (T_c = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}*	BD 234 BD 236 BD 238	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	BD 234 BD 236 BD 238	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 0.15 A, V_{CE} = 2 V) (I_C = 1 A, V_{CE} = 2 V)	h_{FE1} h_{FE2}		40 25	— —	
Collector-Emitter Saturation Voltage* (I_C = 1 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$*		—	0.6	Vdc
Base-Emitter On Voltage* (I_C = 1 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.3	Vdc
Current-Gain-Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		3.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



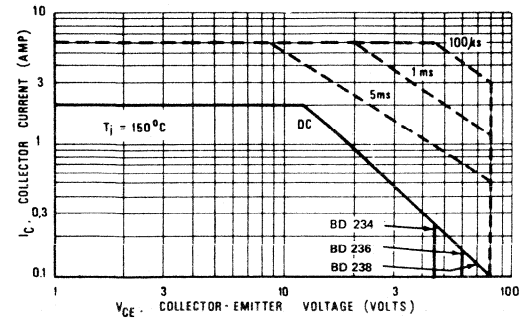
When mounting the device, torque not to exceed 0.07 m-kg

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

All dimensions in millimeters

CASE 77-04

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – COLLECTOR SATURATION REGION

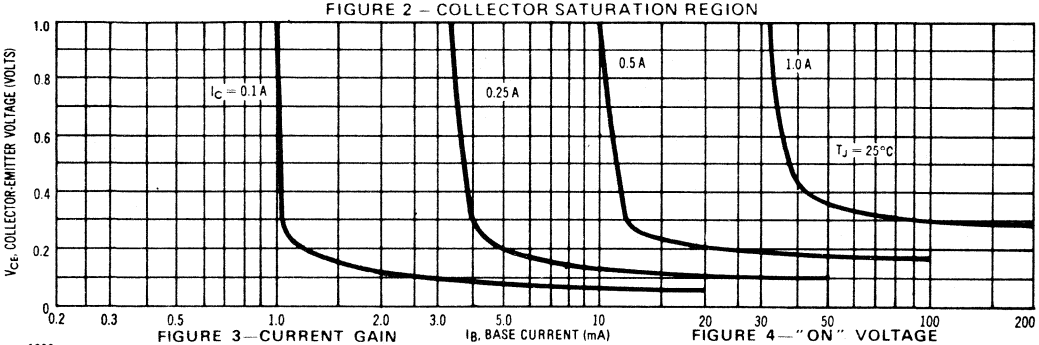


FIGURE 3—CURRENT GAIN

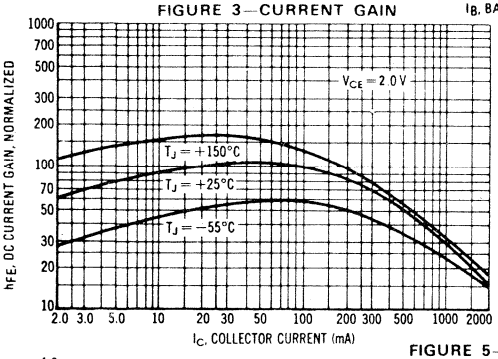


FIGURE 4—"ON" VOLTAGE

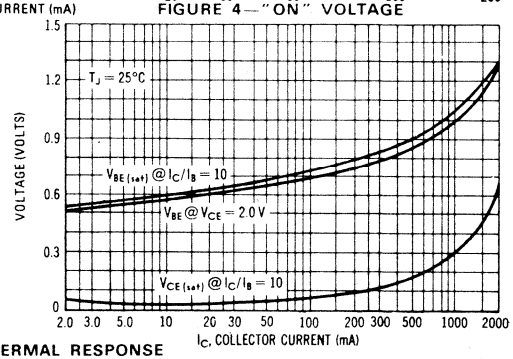
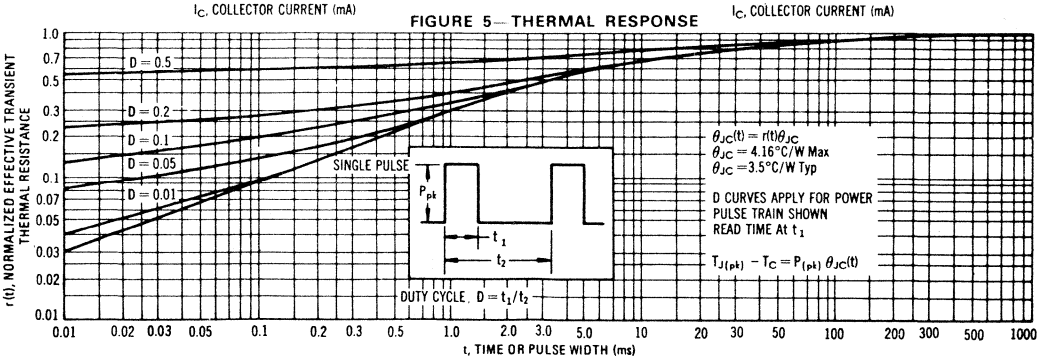


FIGURE 5—THERMAL RESPONSE



3

NPN PNP

BD239 BD240
BD239A BD240A
BD239B BD240B
BD239C BD240C

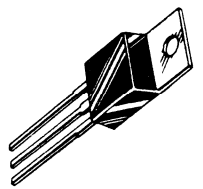
COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in general purpose amplifier and switching applications. Compact TO-220 AB package. TO-66 leadform also available ordered with "66" suffix.

2 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

45, 60, 80, 100 VOLTS
30 WATTS



MAXIMUM RATINGS

Rating	Symbol	BD239 BD240	BD239A BD240A	BD239B BD240B	BD239C BD240C	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Emitter Voltage	V_{CB}	55	70	90	115	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current — Continuous	I_C	2				Adc
Peak		4				
Base Current	I_B	0.6				Adc
Total Device Dissipation @ T_C = 25°C	P_D	30				Watts
Derate above 25°C		0.24				W/°C
Total Device Dissipation @ T_A = 25°C	P_D	2.0				Watts
Derate above 25°C		0.016				W/°C
Unclamped Inductive Load Energy (See Note 3)	E	32				mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150				°C

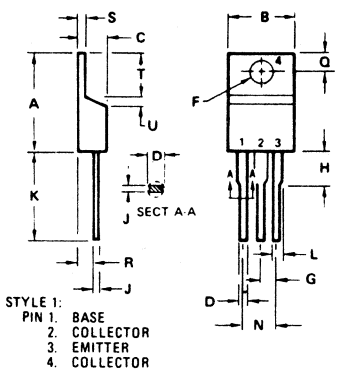
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.167	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	BD239, BD240	$V_{CEO(sus)}$	45	–	Vdc
	BD239A, BD240A		60	–	
	BD239B, BD240B		80	–	
	BD239C, BD240C		100	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	BD239A, BD240A		–	0.3	
(V_{CE} = 60 Vdc, I_B = 0)	BD239B,C, BD240B, C		–	0.3	
Collector Cutoff Current		I_{CES}			μAdc
(V_{CE} = 45 Vdc, V_{EB} = 0)	BD239, BD240		–	200	
(V_{CE} = 60 Vdc, V_{EB} = 0)	BD239A, BD240A		–	200	
(V_{CE} = 80 Vdc, V_{EB} = 0)	BD239B, BD240A		–	200	
(V_{CE} = 100 Vdc, V_{EB} = 0)	BD239C, BD240C		–	200	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 0.2 Adc, V_{CE} = 4.0 Vdc)			40	–	
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)			15		
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 200 mAdc)		$V_{CE(sat)}$	–	0.7	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	1.3	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (2) (I_C = 200 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	3.0	–	MHz
Small-Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1 kHz)		h_{fe}	20	–	–

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \cdot f_{test}$
(3) This rating based on testing with L_C = 20 mH, R_{BE} = 100 Ω, R_E = 0.1 Ω, I_C = 1.8 A.



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

FIGURE 1 – DC CURRENT GAIN

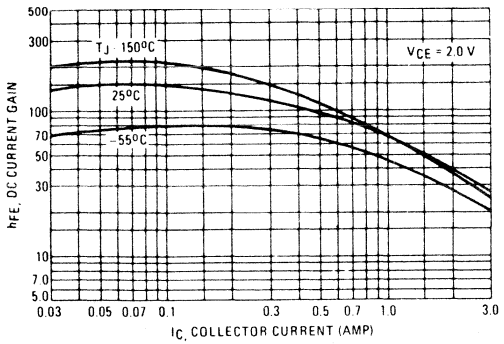


FIGURE 2 – TURN-OFF TIME

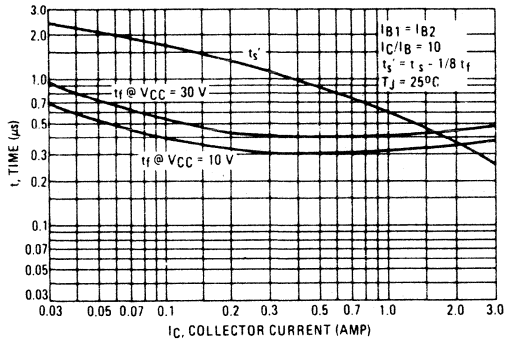


FIGURE 3 – SWITCHING TIME EQUIVALENT CIRCUIT

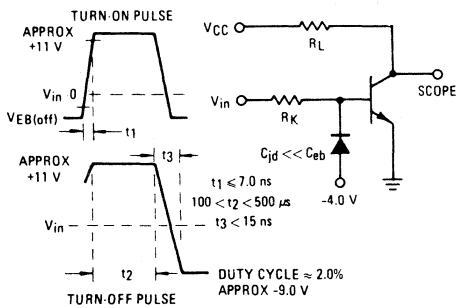


FIGURE 4 – TURN-ON TIME

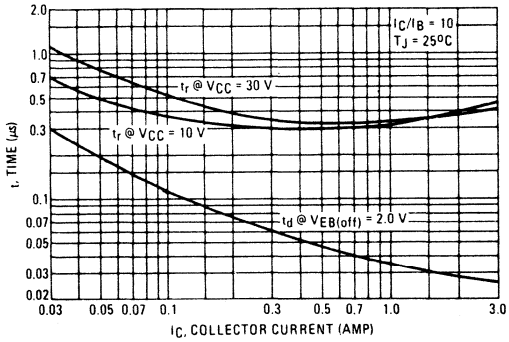
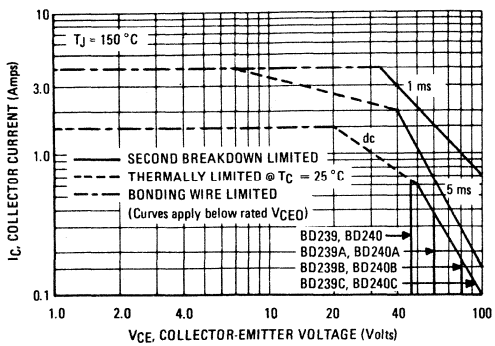


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

3

NPN PNP

BD241 BD242
BD241A BD242A
BD241B BD242B
BD241C BD242C

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

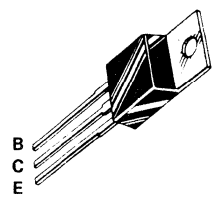
. . . designed for use in general purpose amplifier and switching applications.

- Collector-Emitter Saturation Voltage –
  V_{CE} = 1.2 Vdc (Max) @ I_C = 3.0 Adc
- Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 45 Vdc (Min.) BD241, BD242
  = 60 Vdc (Min.) BD241A, BD242A
  = 80 Vdc (Min.) BD241B, BD242B
  = 100 Vdc (Min.) BD241C, BD242C
- High Current Gain – Bandwidth Product
  f_T = 3.0 MHz (Min) @ I_C = 500 mAdc
- Compact TO-220 AB Package
- TO-66 Leadform Also Available ordered with "–66" suffix.

3 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

45, 60, 80, 100 VOLTS
40 WATTS



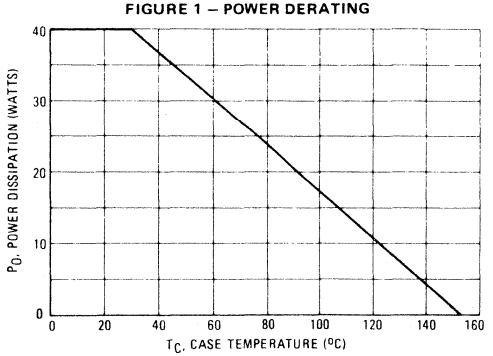
MAXIMUM RATINGS

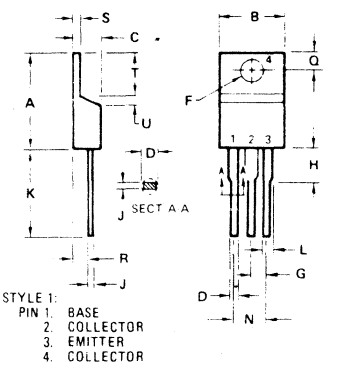
Rating	Symbol	BD241 BD242	BD241A BD242A	BD241B BD242B	BD241C BD242C	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Emitter Voltage	V_{CES}	55	70	90	115	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current - Continuous	I_C	3.0				Adc
Peak		5.0				Adc
Base Current	I_B	1.0				Adc
Total Device Dissipation @ T_C = 25°C	P_D	40				Watts
Derate above 25°C		0.32				W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic		Symbol	Min.	Max.	Unit.
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage[1] (I_C = 30 mAdc, I_B = 0)	BD241, BD242	V_{CEO}	45		Vdc
	BD241A, BD242A		60		
	BD241B, BD242B		80		
	BD241C, BD242C		100		
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	BD241, BD241A, BD242, BD242A,			0.3	
(V_{CE} = 60 Vdc, I_B = 0)	BD241B, BD241C, BD242B, BD242C			0.3	
Collector Cutoff Current		I_{CES}			μAdc
(V_{CE} = 45 Vdc, V_{EB} = 0)	BD241, BD242			200	
(V_{CE} = 60 Vdc, V_{EB} = 0)	BD241A, BD242A			200	
(V_{CE} = 80 Vdc, V_{EB} = 0)	BD241B, BD242B			200	
(V_{CE} = 100 Vdc, V_{EB} = 0)	BD241C, BD242C			200	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}		1.0	mAdc
ON CHARACTERISTICS[1]					
DC Current Gain		h_{FE}			
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)			25		
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)			10		
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 600 Adc)		$V_{CE(sat)}$		1.2	Vdc
Base-Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$		1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product[2] (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	3.0		MHz
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1kHz)		h_{fe}	20		

[1] Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%
[2] $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIME EQUIVALENT CIRCUIT

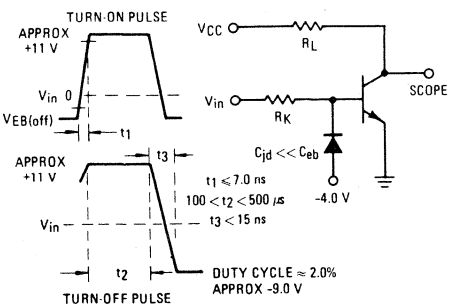
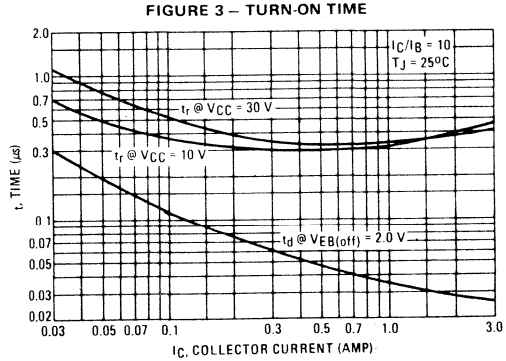


FIGURE 3 – TURN-ON TIME



3

FIGURE 4 – THERMAL RESPONSE

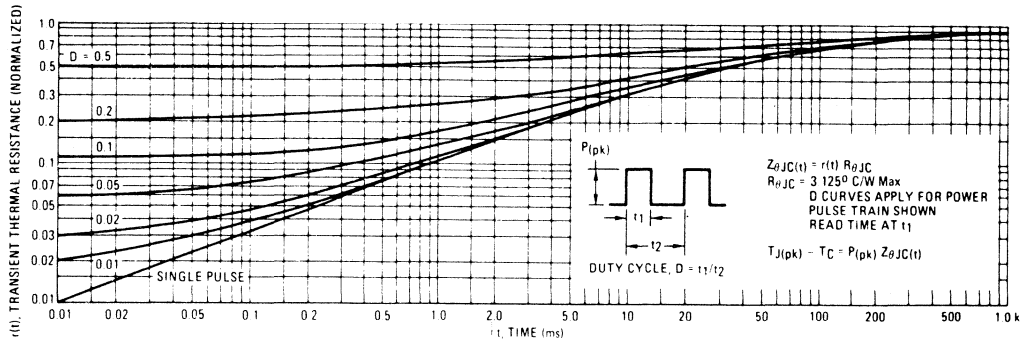
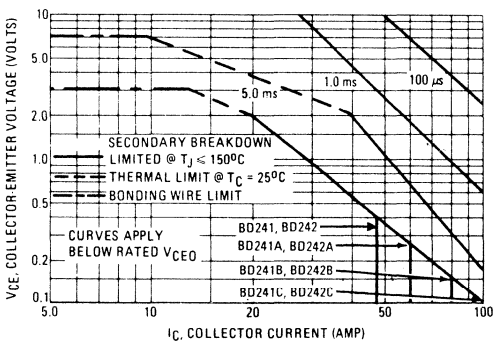


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

FIGURE 6 – TURN-OFF TIME

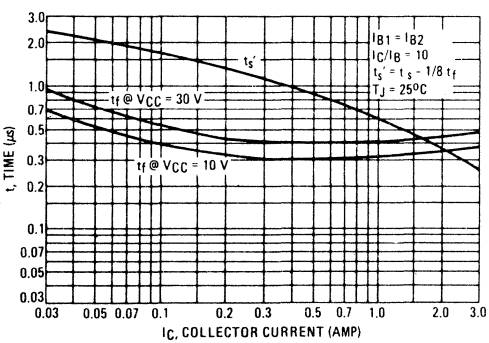


FIGURE 7 – CAPACITANCE

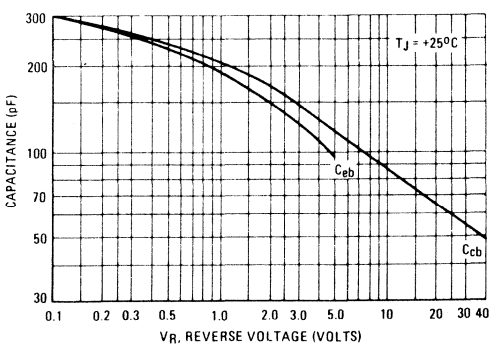


FIGURE 8 – DC CURRENT GAIN

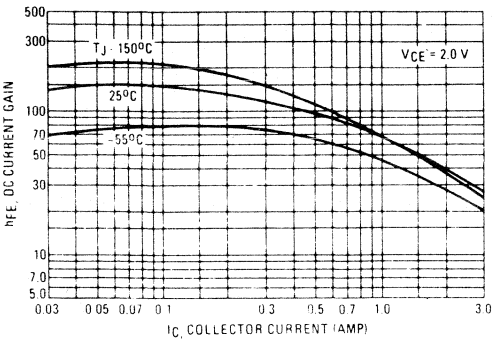


FIGURE 9 – COLLECTOR SATURATION REGION

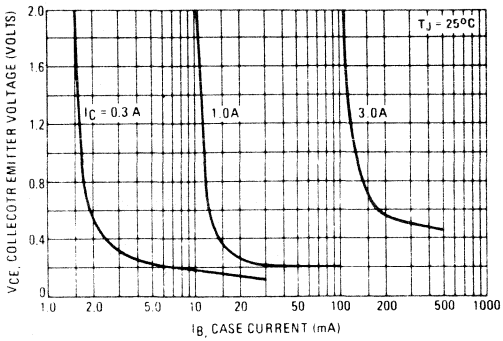


FIGURE 10 – "ON" VOLTAGES

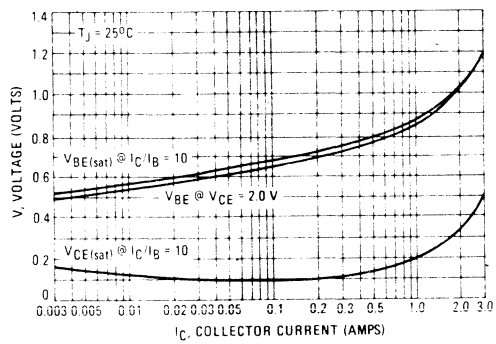


FIGURE 11 – TEMPERATURE COEFFICIENTS

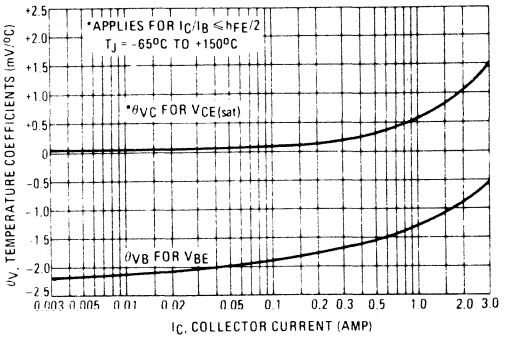


FIGURE 12 – COLLECTOR CUT-OFF REGION

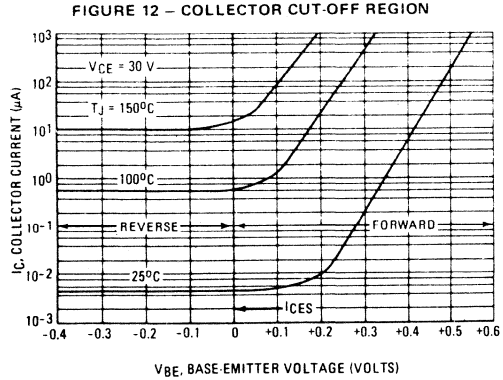
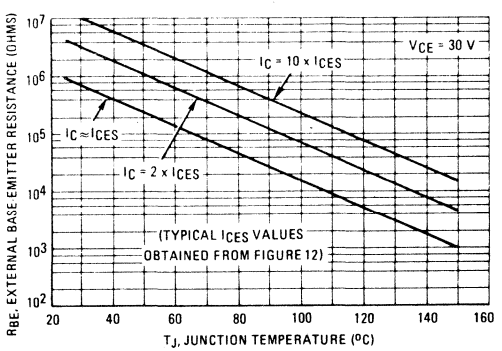


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



3

BD243, 243A, 243B, 243C
BD244, 244A, 244B, 244C

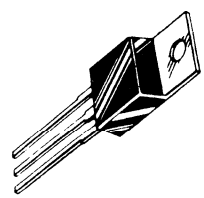
COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in general purpose amplifier and switching applications.

- Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.5 Vdc (Max) @ I_C = 6.0 Adc
- Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 45 Vdc (Min) — BD243, BD244
  = 60 Vdc (Min) — BD243A, BD244A
  = 80 Vdc (Min) — BD243B, BD244B
  = 100 Vdc (Min) — BD243C, BD244C
- High Current Gain – Bandwidth Product
  f_T = 3.0 MHz (Min) @ I_C = 500 mAdc
- Compact TO-220 AB Package

6 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON

45-60-80-100 VOLTS
65 WATTS



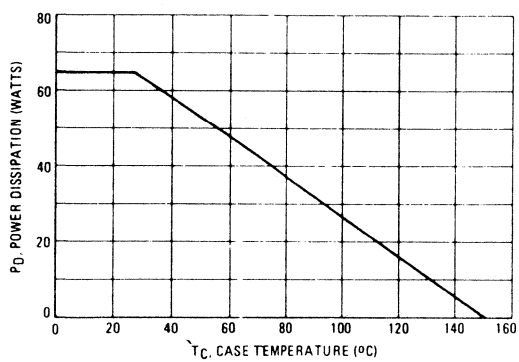
*MAXIMUM RATINGS

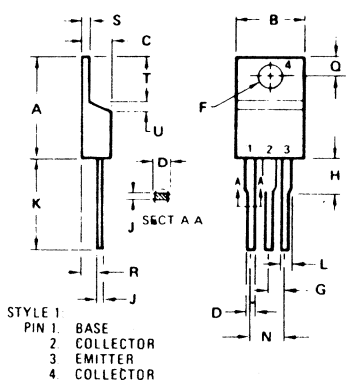
Rating	Symbol	BD243 BD244	BD243A BD244A	BD243B BD244B	BD243C BD244C	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current Continuous	I_C	6				Adc
Peak		10				
Base Current	I_B	2.0				Adc
Total Device Dissipation @ T_C = 25°C	P_D	65				Watts
Derate above 25°C		0.52				W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W

FIGURE 1 – POWER DERATING





STYLE 1
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
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T	5.97	6.48	0.235	0.255
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CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

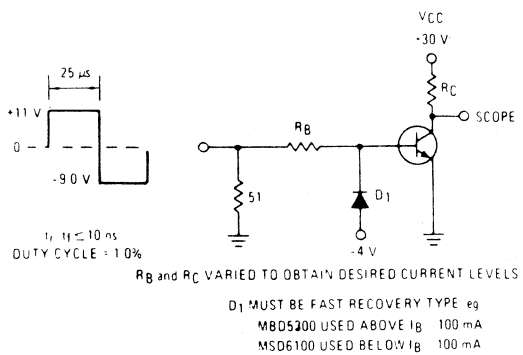
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	BD243, BD244	$V_{CEO(sus)}$	45	–	Vdc
	BD243A, BD244A		60	–	
	BD243B, BD244B		80	–	
	BD243C, BD244C		100	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	BD243, BD243A, BD244, BD244A		–	0.7	
(V_{CE} = 60 Vdc, I_B = 0)	BD243B, BD243C, BD244B, BD244C		–	0.7	
Collector Cutoff Current		I_{CES}			μAdc
(V_{CE} = 45 Vdc, V_{EB} = 0)	BD243, BD244		–	400	
(V_{CE} = 60 Vdc, V_{EB} = 0)	BD243A, BD244A		–	400	
(V_{CE} = 80 Vdc, V_{EB} = 0)	BD243B, BD244B		–	400	
(V_{CE} = 100 Vdc, V_{EB} = 0)	BD243C, BD244C		–	400	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 0.3 Adc, V_{CE} = 4.0 Vdc)			30	–	
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)			15	–	
Collector-Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 1 Adc)		$V_{CE(sat)}$	–	1.5	Vdc
Base-Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	3.0	–	MHz
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 kHz)		h_{fe}	20	–	–

(1) Pulse Test: Pulsewidth ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = h_{fe} \bullet f_{test}$

3

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



RB and RC VARIED TO OBTAIN DESIRED CURRENT LEVELS

D1 MUST BE FAST RECOVERY TYPE eg
MBD5200 USED ABOVE IB 100 mA
MSD6100 USED BELOW IB 100 mA

FIGURE 3 – TURN-ON TIME

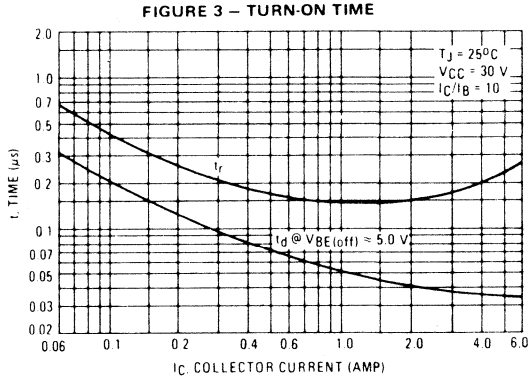


FIGURE 4 – THERMAL RESPONSE

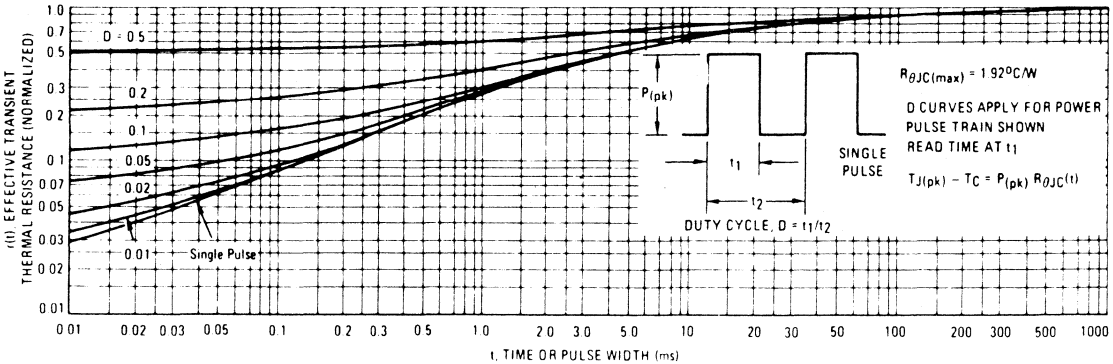
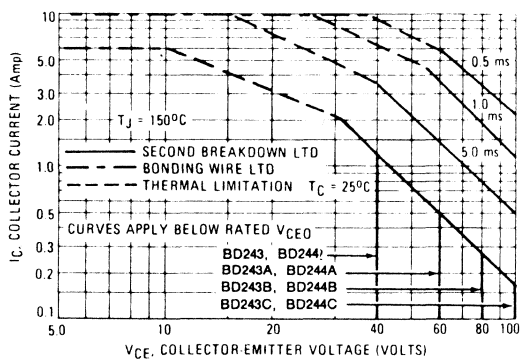


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

FIGURE 6 – TURN-OFF TIME

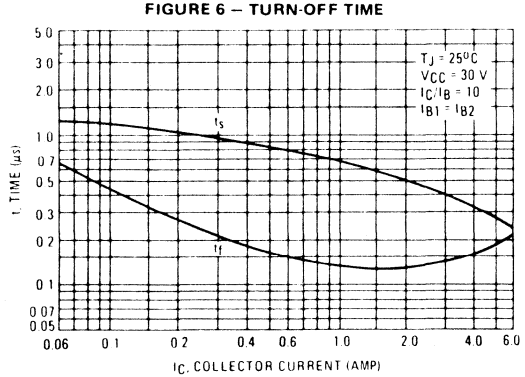


FIGURE 7 – CAPACITANCE

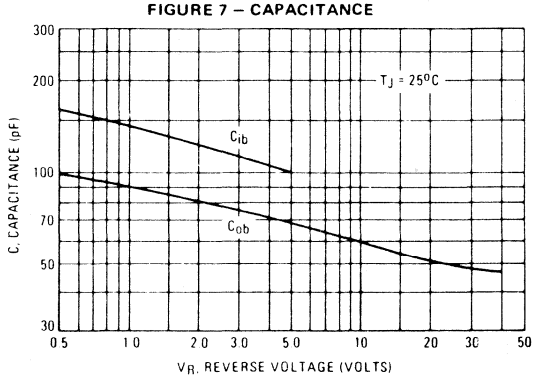


FIGURE 8 – DC CURRENT GAIN

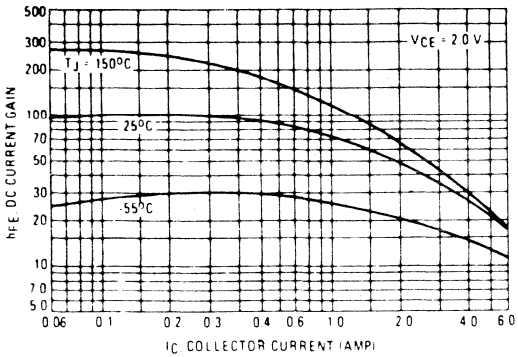


FIGURE 9 – COLLECTOR SATURATION REGION

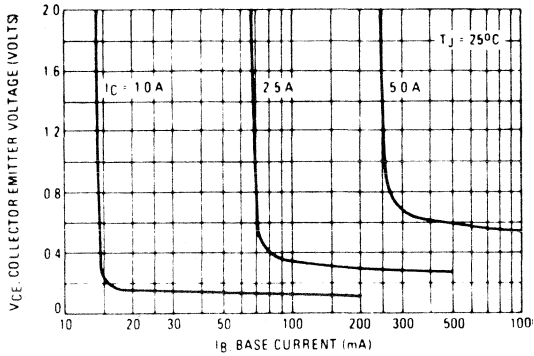


FIGURE 10 – "ON" VOLTAGES

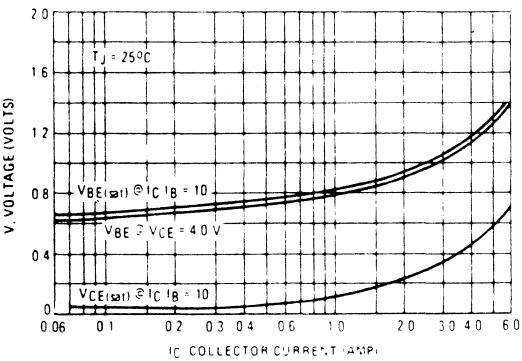


FIGURE 11 – TEMPERATURE COEFFICIENTS

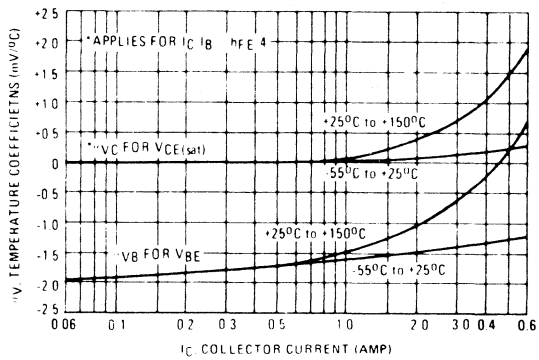


FIGURE 12 – COLLECTOR CUT-OFF REGION

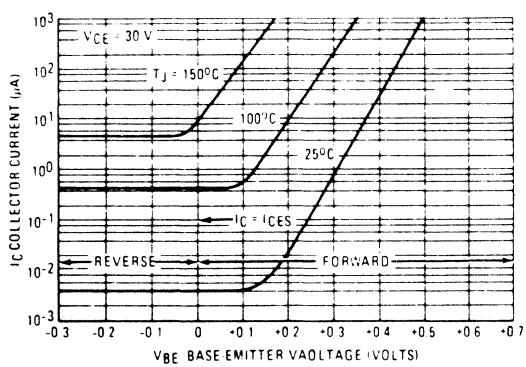
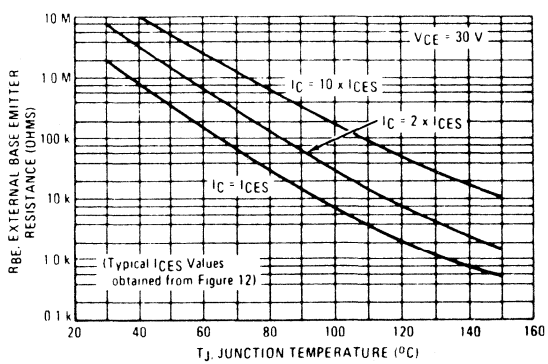


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



3

NPN

BD311

PNP

BD312

COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

. . . designed for high quality amplifiers operating up to 60 Watts into 4 ohm load.

- High DC Current Gain
- Excellent Safe Operating Area
- High Current Gain – Bandwidth Product – Typical
  f_T = 4.0 MHz @ I_C = 0.5 A

10 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

60 VOLTS 115 WATTS

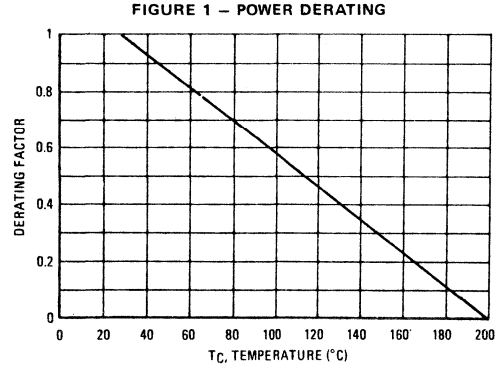
MAXIMUM RATINGS

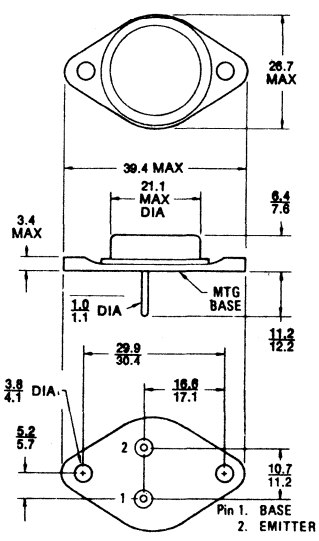
Rating	Symbol	BD311/312	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous Peak	I_C	10 20	Adc
Base Current	I_B	4.0	Adc
Total Device Dissipation @ T_C = 25 °C Derate above 25 °C	P_D	115 0.658	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit.
Thermal Resistance, Junction to Case	θ_{JC}	1.52	°C/W

FIGURE 1 – POWER DERATING





Dimensions in millimeters
Collector connected to case

CASE 11
TO-3

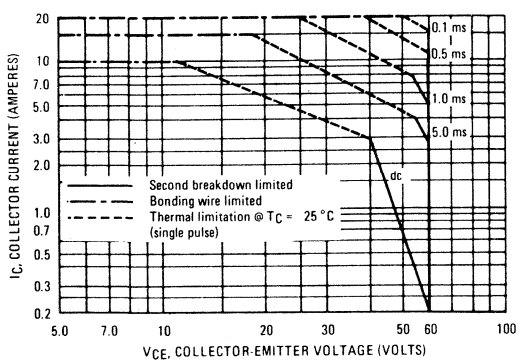
ELECTIRCAL CHARACTERISTICS* (T_C = 25 °C unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit.
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage[1] (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	60		Vdc
Collector-Base Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)	I_{CBO}		1.0	mAdc
Emitter-Base Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}		1.0	mAdc
ON CHARACTERISTICS[1]				
DC Current Gain (I_C = 5.0 Vdc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	H_{FE}	25 5		–
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.5 Adc)	$V_{CE(sat)}$		1.0	Vdc
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.5 Adc)	$V_{BE(sat)}$		1.8	Vdc
Base-Emitter On Voltage (I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS[1]				
Current-Gain – Bandwidth Product[2] (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T	4.0		MHz
SECOND BREAKDOWN				
Second Breakdown Collector Current (V_{CE} = 39 Vdc, t = 0.5 sec.) (V_{CE} = 50 Vdc, t = 0.5 sec.)	$I_{S/B}$	2.95 0.60		Adc

[1] Pulse test: Pulse width ≤ 300 μs, Duty Cycle ≥ 2%

[2] $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.
Second breakdown pulse limits are valid for duty cycles to 10%.

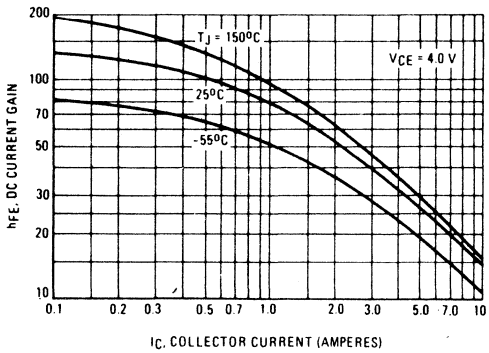
At high case temperatures, thermal limitation may reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

PNP DEVICE
BD312

NPN DEVICE
BD311

FIGURE 3 – DC CURRENT GAIN



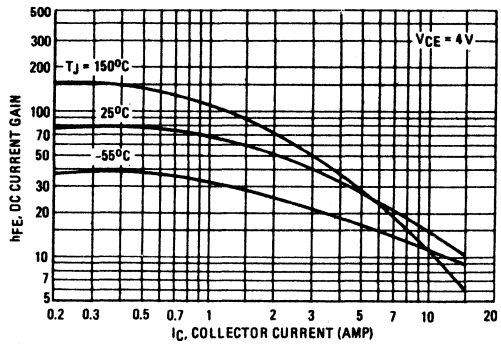
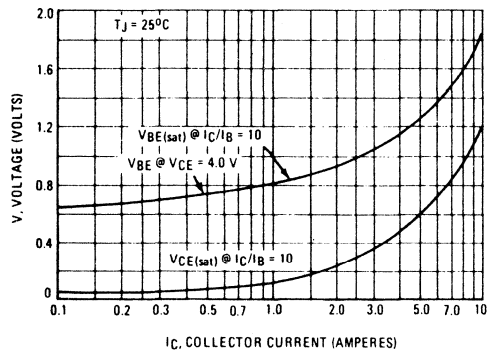
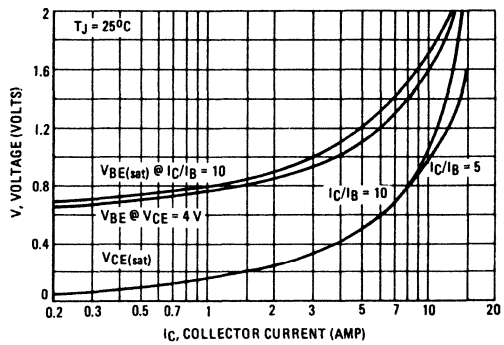


FIGURE 4 – "ON" VOLTAGES





NPN

BD313

PNP

BD314

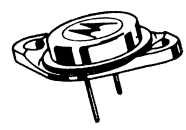
COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

. . . designed for high quality amplifiers operating up to 60 Watts into 8 ohm load.

- High DC Current Gain
- Excellent Safe Operating Area
- High Current Gain – Bandwidth Product – Typical
  f_T = 4.0 MHz @ I_C = 0.5 A

10 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

80 VOLTS 150 WATTS



3

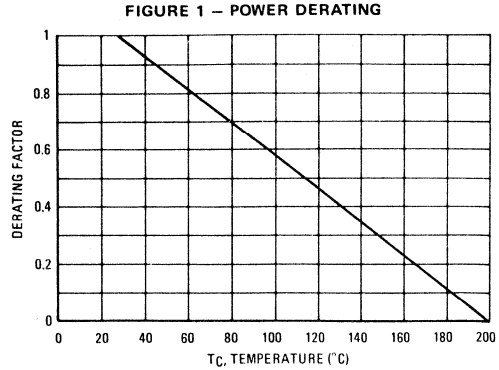
MAXIMUM RATINGS

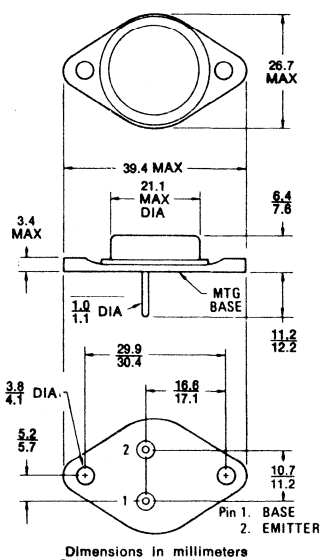
Rating	Symbol	BD313/314	Unit
Collector-Emitter Voltage	V_{CEO}	80	Vdc
Collector-Base Voltage	V_{CB}	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous Peak	I_C	10 20	Adc
Base Current	I_B	4.0	Adc
Total Device Dissipation @ T_C = 25 °C Derate above 25 °C	P_D	150 0.857	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit.
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

FIGURE 1 – POWER DERATING





Dimensions in millimeters
Collector connected to case

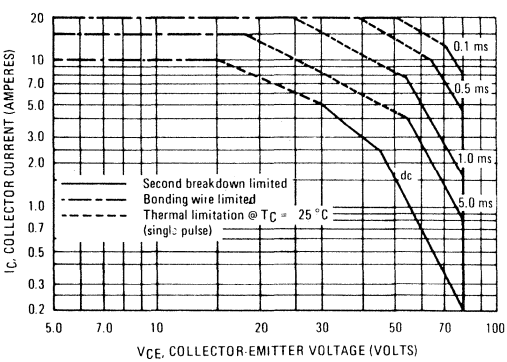
CASE 11
TO-3

ELECTIRCAL CHARACTERISTICS* (T_C = 25 °C unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit.
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage[1] (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	80		Vdc
Collector-Base Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)	I_{CBO}		1.0	mAdc
Emitter-Base Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}		1.0	mAdc
ON CHARACTERISTICS[1]				
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	H_{FE}	25 5		–
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.5 Adc)	$V_{CE(sat)}$		1.0	Vdc
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.5 Adc)	$V_{BE(sat)}$		1.8	Vdc
Base-Emitter On Voltage (I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS[1]				
Current-Gain – Bandwidth Product[2] (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T	4.0		MHz
SECOND BREAKDOWN				
Second Breakdown Collector Current (V_{CE} = 30 Vdc, t = 0.5 sec.) (V_{CE} = 50 Vdc, t = 0.e sec.)	$I_{S/B}$	5 1.5		Adc

[1] Pulse test: Pulse width ⩽ 300 μs, Duty Cycle ⩾2%
[2] $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



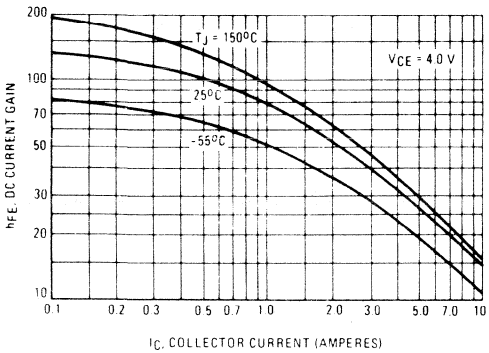
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.
Second breakdown pulse limits are valid for duty cycles to 10%.

At high case temperatures, thermal limitation may reduce the power that can be handled to values less than the limitations imposed by second breakdown.

PNP DEVICE
BD314

NPN DEVICE
BD313

FIGURE 3 – DC CURRENT GAIN



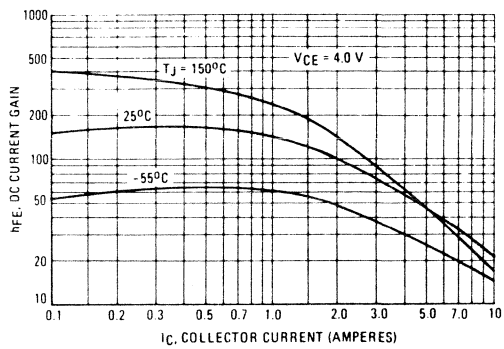
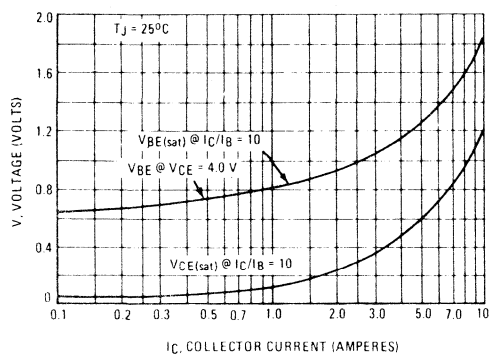
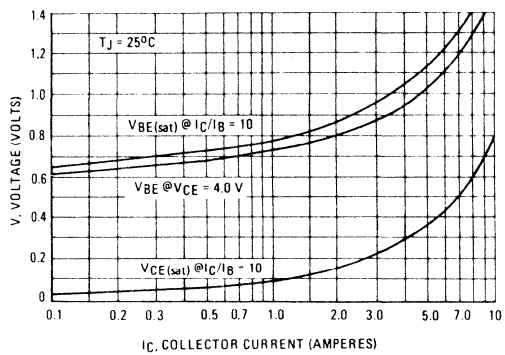


FIGURE 4 – "ON" VOLTAGES





3

BD315 • BD316
BD317 • BD318

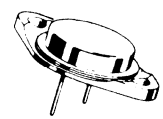
COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

... designed for high quality amplifiers operating up to 100 Watts into 4 ohm load with BD315, BD316 and into 8 ohm load with BD317, BD318.

- High DC Current Gain
- Excellent Safe Operating Area
- High Current Gain — Bandwidth Product — Typical f_T = 2.0 MHz @ I_C = 1.0 A

16 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

80-100 VOLTS 200 WATTS



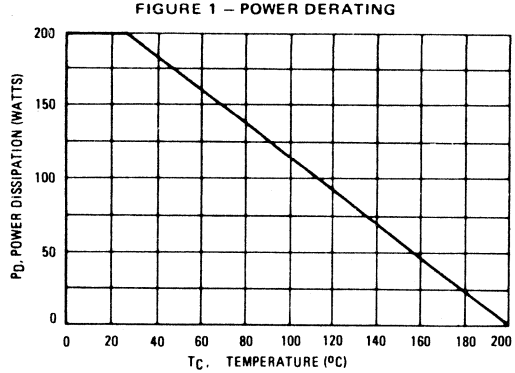
MAXIMUM RATINGS

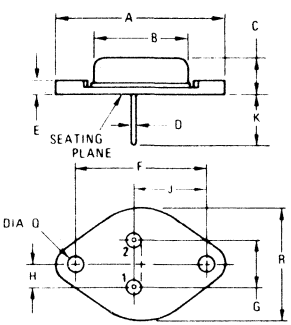
Rating	Symbol	BD315 BD316	BD317 BD318	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	7.0		Vdc
Collector Current — Continuous Peak	I_C	16 20		Adc
Base Current — Continuous	I_B	5.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

FIGURE 1 – POWER DERATING





STYLE 1
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE
1. DIM "Q" IS DIA

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A		39.37	–	1.550
B		21.08		0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E		3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R		26.67	–	1.050

Collector connected to case

CASE 11 (TO-3)

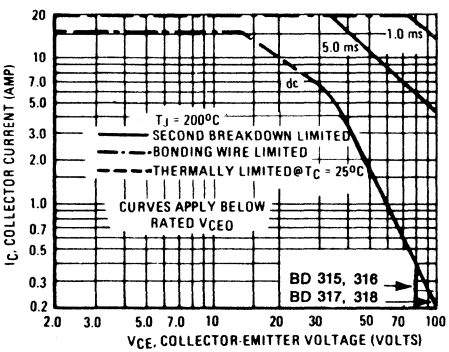
*** ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	BD315, BD316 BD317, BD318	$V_{CEO(sus)}$	 80 100	 — —	Vdc
Collector-Base Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	—	1.0	mAdc
Emitter-Base Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain I_C = 5.0 Adc, V_{CE} = 4.0 Vdc I_C = 8.0 Adc, V_{CE} = 4.0 Vdc I_C = 10 Adc, V_{CE} = 4.0 Vdc	 BD317, BD318 BD315, BD316 All Types	h_{FE}	 25 25 15		—
Collector-Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 0.8 Adc)		$V_{CE(sat)}$	—	1.0	Vdc
Base-Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 0.8 Adc)		$V_{BE(sat)}$	—	1.8	Vdc
Base-Emitter On Voltage (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)		f_T	1.0	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≥ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$.

3

FIGURE 2 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C — V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ <200°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415).

PNP DEVICES
BD316 and BD318

NPN DEVICES
BD315 and BD317

FIGURE 3 — DC CURRENT GAIN

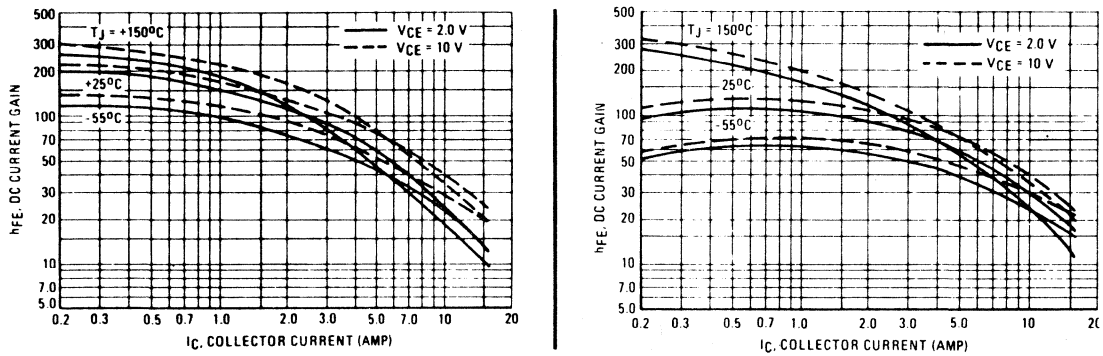
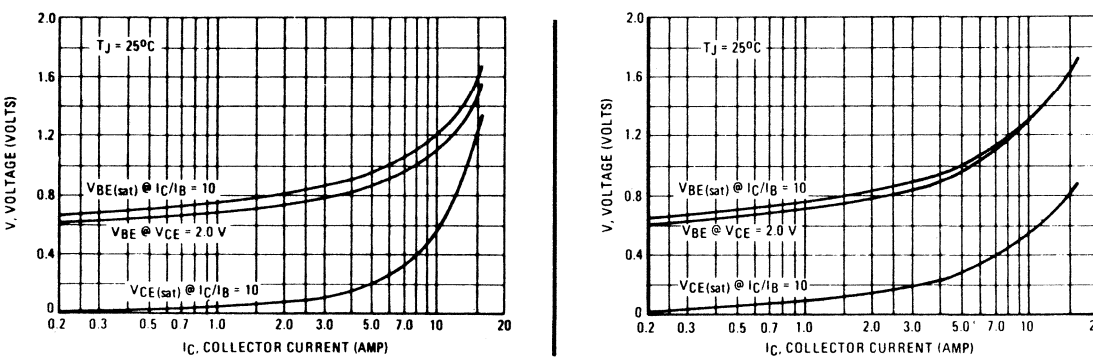


FIGURE 4 — "ON" VOLTAGES



BD385
BD387
BD389

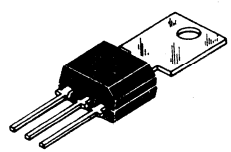
NPN SILICON ANNULAR♦ AMPLIFIER TRANSISTORS

. . . designed for general-purpose, medium-voltage, medium power amplifier and driver applications; series, shunt and switching regulators, and low and high frequency inverters and converters.

- High Collector-Emitter Breakdown Voltage – BV_{CEO} = 100 Vdc (Min.) @ I_C = 1.0 mAdc – BD389
- Duowatt Package – 2 Watts Free Air Dissipation @ T_A = 25°C
- Complements to PNP BD386, BD388, BD390

DUOWATT

NPN SILICON AMPLIFIER TRANSISTORS



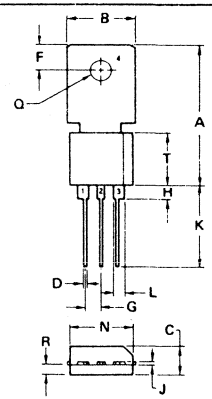
MAXIMUM RATINGS

Rating	Symbol	BD385	BD387	BD389	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CBO}	60	80	100	Vdc
Emitter-Base Voltage	V_{EBO}	← 5.0 →			Vdc
Collector Current – Continuous	I_C	← 1.0 →			Adc
– Peak (1)		← 2.0 →			
Base Current	I_B	← 100 →			mAdc
Total Power Dissipation @ T_A = 25°C	P_D	← 2.0 →			Watts
Derate above 25°C		← 16 →			mW/°C
Total Power Dissipation @ T_C = 25°C	P_D	← 10 →			Watts
Derate above 25°C		← 80 →			mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	← -55 to +150 →			°C
Solder Temperature, 1/16" from Case for 10 Seconds	–	← 260 →			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R\theta_{JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R\theta_{JC}$	12.5	°C/W

(1) ≤10 ms, ≤ 50% Duty Cycle



STYLE 2
PIN 1. EMITTER
2. COLLECTOR
3. BASE
4. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

CASE 306-04

3

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage		BV_{CEO}			Vdc
(I_C = 1.0 mAdc, I_B = 0)	BD385		60	–	
	BD387		80	–	
	BD389		100	–	
Collector-Base Breakdown Voltage		BV_{CBO}			Vdc
(I_C = 100 μAdc, I_E = 0)	BD385		60	–	
	BD387		80	–	
	BD389		100	–	
Emitter-Base Breakdown Voltage		BV_{EBO}	5.0	–	Vdc
(I_E = 100 μAdc, I_C = 0)					
Collector Cutoff Current		I_{CBO}			nAdc
(V_{CB} = 40 Vdc, I_E = 0)	BD385		–	100	
(V_{CB} = 60 Vdc, I_E = 0)	BD387		–	100	
(V_{CB} = 80 Vdc, I_E = 0)	BD389		–	100	
Emitter Cutoff Current		I_{EBO}	–	100	nAdc
(V_{EB} = 4.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)			60	–	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)			80	300	
(I_C = 250 mAdc, V_{CE} = 1.0 Vdc)			60	–	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			25	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 250 mAdc, I_B = 10 mAdc)			–	0.5	
(I_C = 1.0 Adc, I_B = 100 mAdc)			–	1.0	
Base-Emitter On Voltage		$V_{BE(on)}$	–	1.2	Vdc
(I_C = 250 mAdc, V_{CE} = 5.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product		f_T	75	350	MHz
(I_C = 100 mAdc, V_{CE} = 5.0 Vdc, f = 20 MHz)					
Collector-Base Capacitance		C_{cb}	–	18	pF
(V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)					

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

TYPICAL CHARACTERISTICS

FIGURE 1 – CURRENT-GAIN – BANDWIDTH PRODUCT

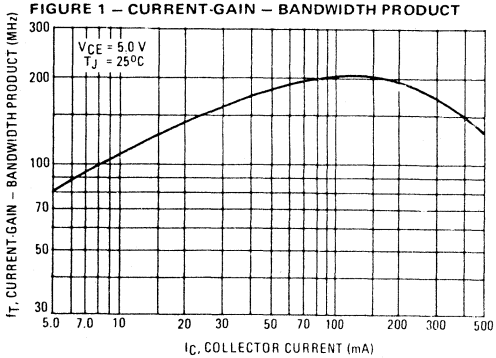
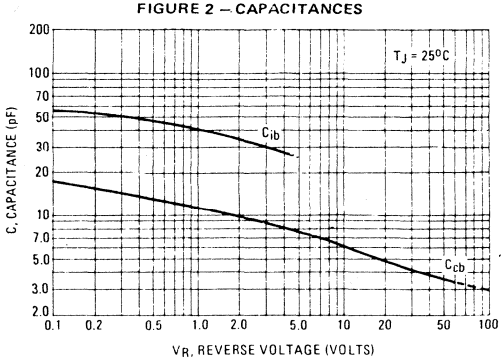


FIGURE 2 – CAPACITANCES



TYPICAL CHARACTERISTICS (continued)

FIGURE 3 – DC CURRENT GAIN

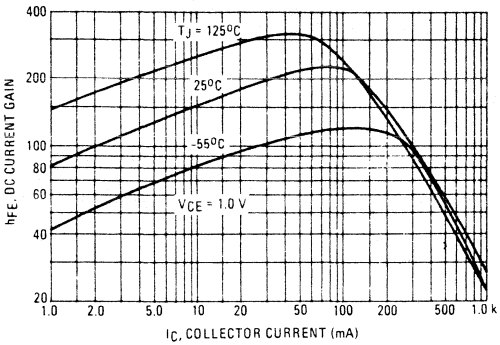


FIGURE 4 – "ON" VOLTAGE

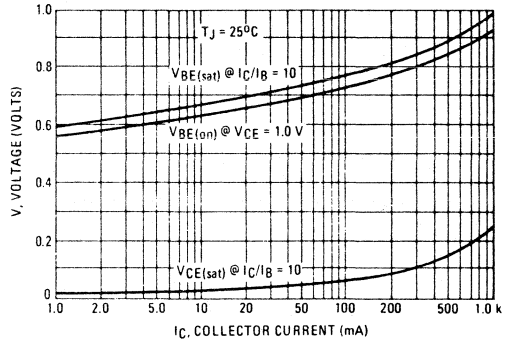


FIGURE 5 – COLLECTOR SATURATION REGION

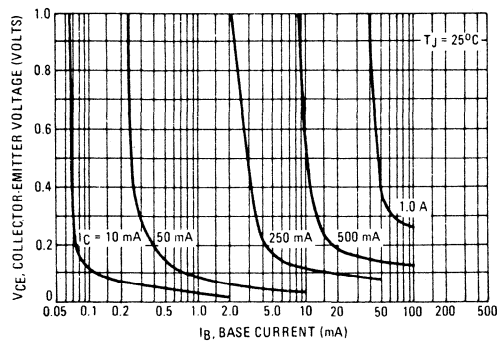


FIGURE 6 – TEMPERATURE COEFFICIENTS

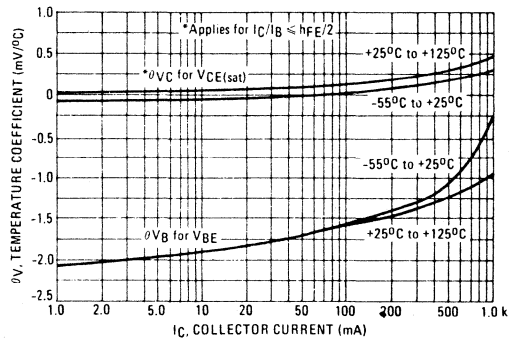


FIGURE 7 – COLLECTOR CHARACTERISTICS

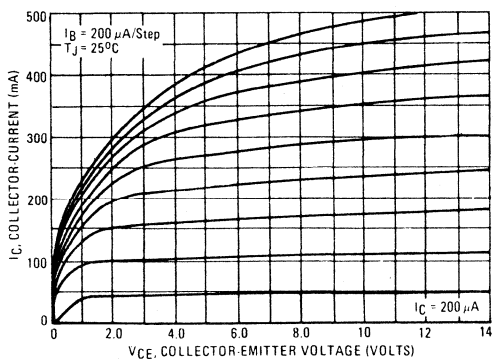
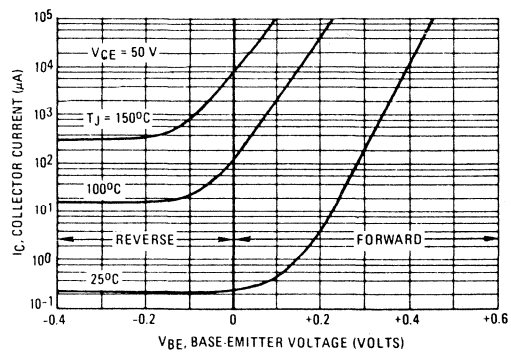


FIGURE 8 – COLLECTOR CUTOFF REGION



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TYPICAL CHARACTERISTICS (continued)

FIGURE 9 – THERMAL RESPONSE

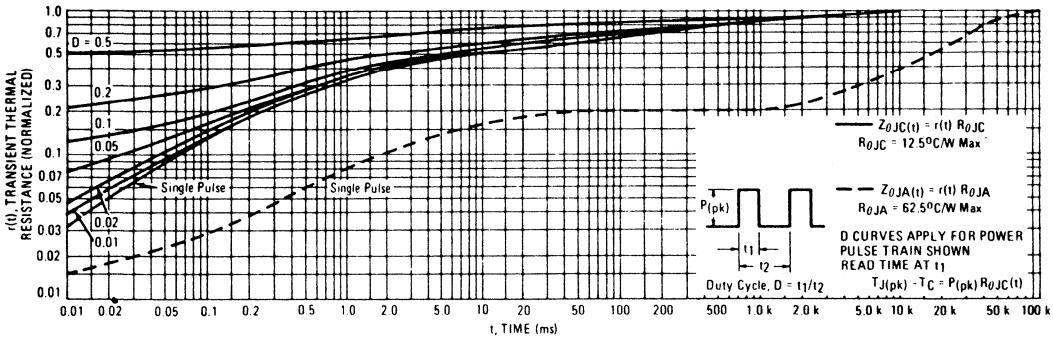
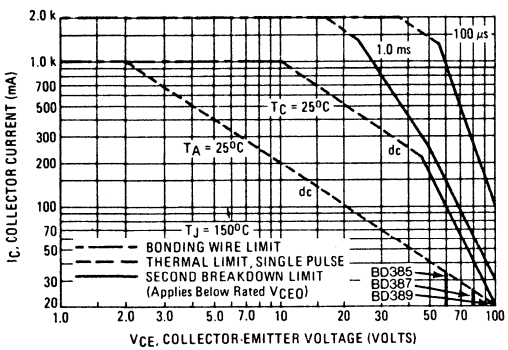


FIGURE 10 – ACTIVE-REGION SAFE-OPERATING AREA

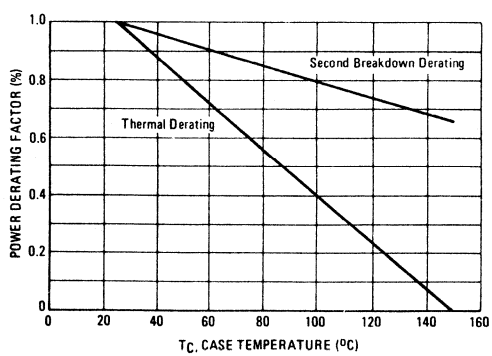


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 11 – POWER DERATING



BD386
BD388
BD390

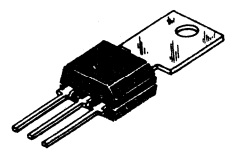
PNP SILICON ANNULAR◆ AMPLIFIER TRANSISTORS

. . . designed for general-purpose, medium-voltage, medium power amplifier and driver applications; series, shunt and switching regulators, and low and high frequency inverters and converters.

- High Collector-Emitter Breakdown Voltage – BV_{CEO} = 100 Vdc (Min) @ I_C = 1.0 mAdc – BD390
- Duowatt Package – 2 Watts Free Air Dissipation @ T_A = 25°C
- Complements to NPN BD385/BD387/BD389

DUOWATT

PNP SILICON AMPLIFIER TRANSISTORS

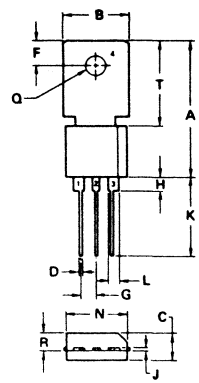


MAXIMUM RATINGS

Rating	Symbol	BD386	BD388	BD390	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CBO}	60	80	100	Vdc
Emitter-Base Voltage	V_{EBO}	← 5.0 →			Vdc
Collector Current – Continuous	I_C	← 1.0 →			Adc
Peak		← 2.0 →			
Base Current	I_B	← 100 →			mAdc
Total Power Dissipation @ T_A = 25°C	P_D	← 2.0 →			Watts
Derate above 25°C		← 16 →			mW/°C
Total Power Dissipation @ T_C = 25°C	P_D	← 10 →			Watts
Derate above 25°C		← 80 →			mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	← −55 to +150 →			°C
Solder Temperature, 1/16" from Case for 10 Seconds	–	← 260 →			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W



STYLE 2
PIN 1. EMITTER
2. COLLECTOR
3. BASE
4. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

CASE 306-04

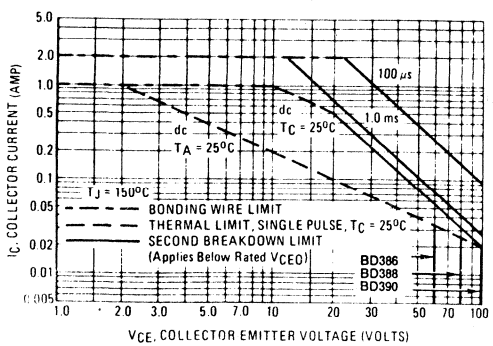
3

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BD386	BV_{CEO}	60	–	Vdc
	BD388		80	–	
	BD390		100	–	
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BD386	BV_{CBO}	60	–	Vdc
	BD388		80	–	
	BD390		100	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	5.0	–	Vdc
Collector Cutoff Current		I_{CBO}			nAdc
(V_{CB} = 40 Vdc, I_E = 0)	BD386		–	100	
(V_{CB} = 60 Vdc, I_E = 0)	BD388		–	100	
(V_{CB} = 80 Vdc, I_E = 0)	BD390		–	100	
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)		I_{EBO}	–	100	nAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)			60	–	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)			80	300	
(I_C = 250 mAdc, V_{CE} = 1.0 Vdc)			60	–	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			25	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 250 mAdc, I_B = 10 mAdc)			–	0.5	
(I_C = 1.0 Adc, I_B = 100 mAdc)			–	1.0	
Base-Emitter On Voltage (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	–	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 100 mAdc, V_{CE} = 5.0 Vdc, f = 20 MHz)		f_T	75	350	MHz
Collector-Base Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)		C_{cb}		18	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

FIGURE 1 – ACTIVE-REGION SAFE-OPERATING AREA

TYPICAL CHARACTERISTICS (continued)

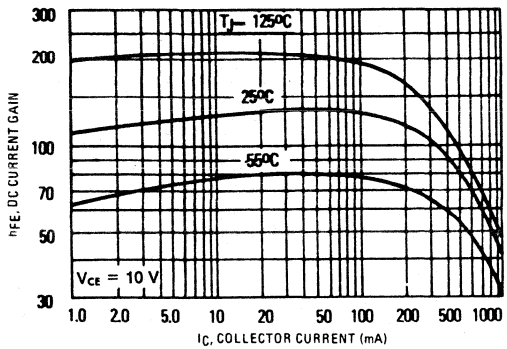


FIGURE 2 – DC CURRENT GAIN

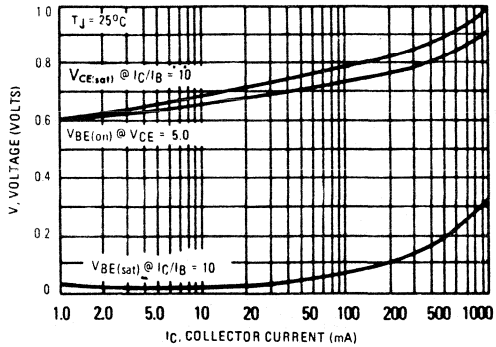


FIGURE 3 – "ON" VOLTAGES

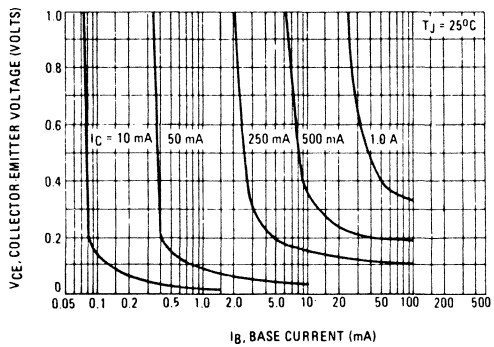


FIGURE 4 – COLLECTOR SATURATION REGION

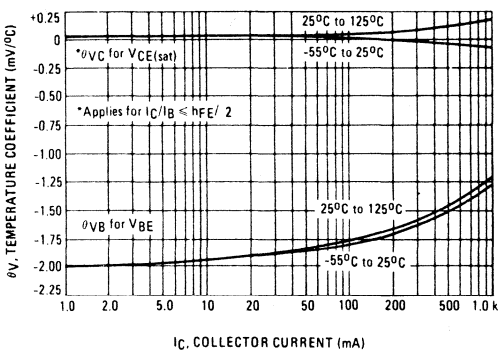


FIGURE 5 – TEMPERATURE COEFFICIENTS

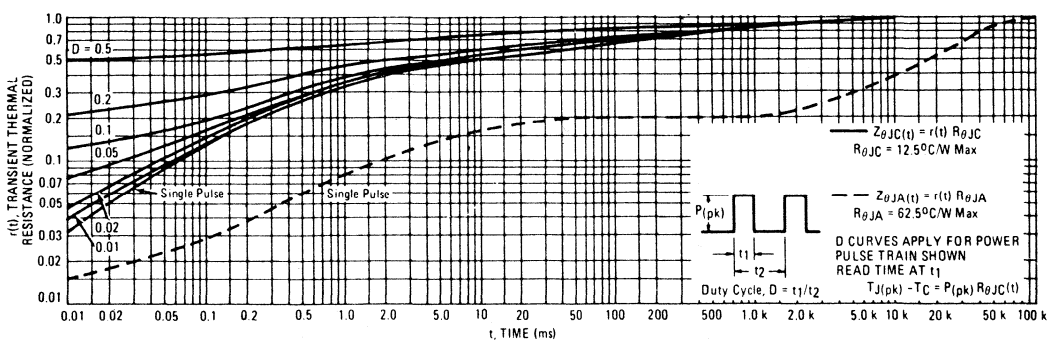


FIGURE 6 – THERMAL RESPONSE

TYPICAL CHARACTERISTICS (continued)

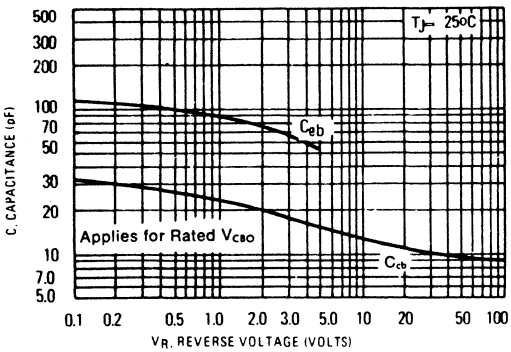


FIGURE 7 – CAPACITANCE

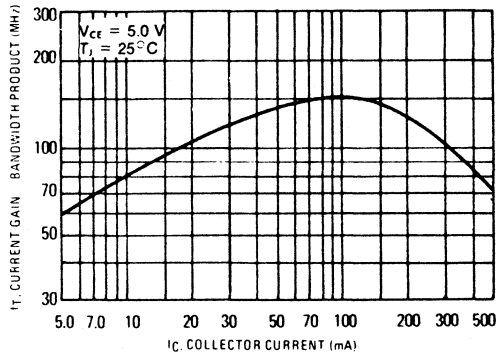


FIGURE 8 – CURRENT-GAIN – BANDWIDTH PRODUCT

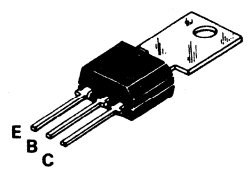
BD411
BD412

NPN SILICON DARLINGTON AMPLIFIER TRANSISTORS

. . . designed for amplifier and driver applications where high gain is an essential requirement, low power lamp and relay drivers and power drivers for high-current applications such as voltage regulators.

- High DC Current Gain –
  h_{FE} = 25,000 (Min) @ I_C = 200 mAdc – **BD 411**
  = 15,000 (Min) @ I_C = 500 mAdc – **BD 411**
- Collector-Emitter Breakdown Voltage –
  BV_{CES} = 40 Vdc (Min) @ I_C = 100 μAdc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.5 Vdc (Max) @ I_C = 1.0 Adc
- Duowatt Package –
  2 Watts Free Air Dissipation @ T_A = 25°C
- **Complements to PNP BD 413/414**

NPN SILICON DARLINGTON AMPLIFIER TRANSISTORS

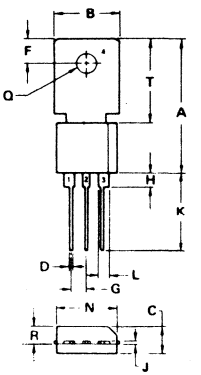


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Emitter Voltage	V_{CES}	40	Vdc
*Collector-Base Voltage	V_{CBO}	50	Vdc
*Emitter-Base Voltage	V_{EBO}	12	Vdc
*Collector Current – Continuous	I_C	2.0	Adc
*Base Current – Continuous	I_B	100	mAdc
*Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 16	Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80	Watts mW/°C
*Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C
*Solder Temperature, 1/16" from Case for 10 Seconds	–	260	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W



STYLE 1
PIN 1 EMITTER
2 BASE
3 COLLECTOR
4 COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

CASE 306-04

3

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

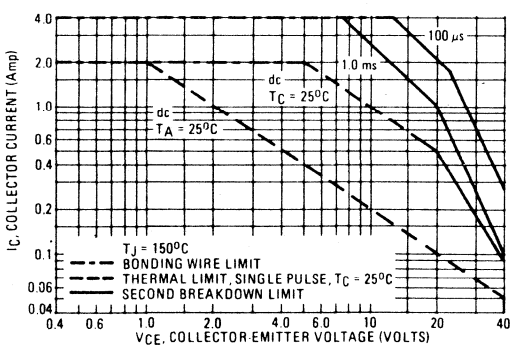
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 100 μAdc, V_{BE} = 0)		BV_{CES}	40	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)		BV_{CBO}	50	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)		BV_{EBO}	12	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)		I_{CBO}	–	100	nAdc
Emitter Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)		I_{EBO}	–	100	nAdc
ON CHARACTERISTICS(1)					
DC Current Gain		h_{FE}			–
(I_C = 200 mAdc, V_{CE} = 5.0 Vdc)	BD411		25,000	150,000	
	BD412		15,000	150,000	
(I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	BD411		15,000	–	
	BD412		10,000	–	
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	BD411		5,000	–	
	BD412		3,000	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 1.0 Adc, I_B = 2.0 mAdc)			–	1.5	
(I_C = 2.0 Adc, I_B = 4.0 mAdc)			–	2.0	
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 2.0 mAdc)		$V_{BE(sat)}$	–	2.0	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	–	2.0	Vdc
DYNAMIC CHARACTERISTICS					
High Frequency Current Gain (I_C = 200 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)		$\|h_{fe}\|$	1.0	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	–	7.0	pF
Small-Signal Current Gain		h_{fe}			–
(I_C = 50 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	BD411		20,000	–	
	BD412		15,000	–	

* Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

TYPICAL CHARACTERISTICS

FIGURE 1 – ACTIVE-REGION SAFE-OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

TYPICAL CHARACTERISTICS (continued)

FIGURE 2 – DC CURRENT GAIN

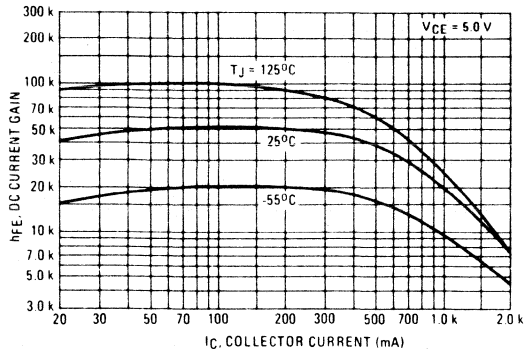


FIGURE 3 – "ON" VOLTAGES

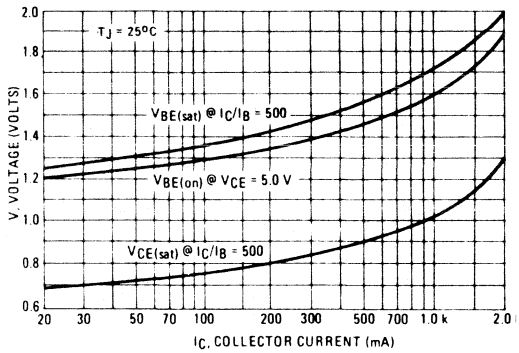


FIGURE 4 – COLLECTOR SATURATION REGION

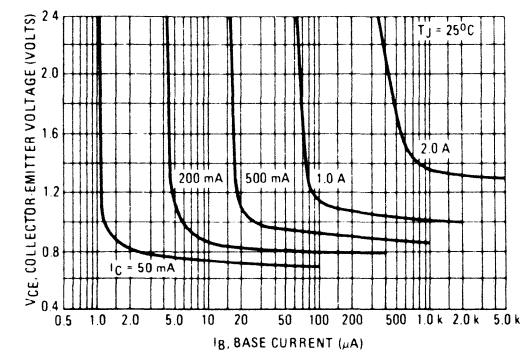


FIGURE 5 – TEMPERATURE COEFFICIENT

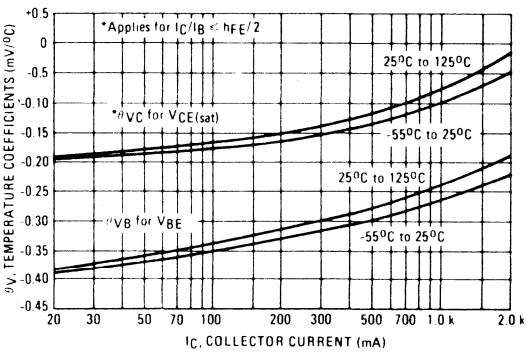
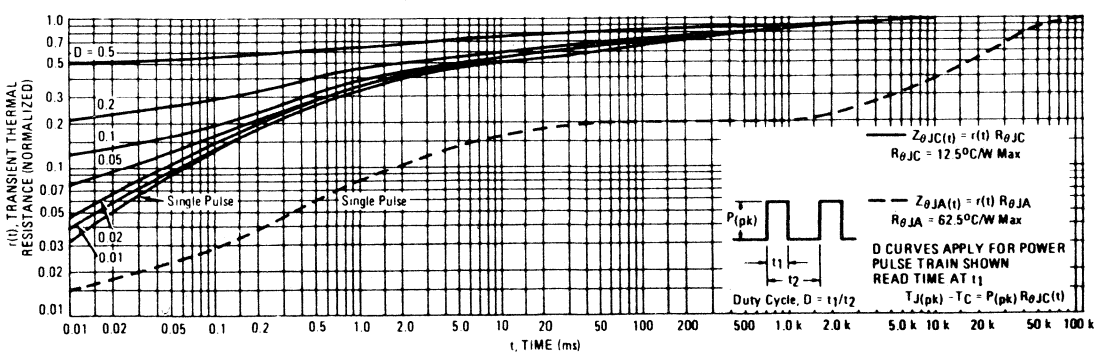


FIGURE 6 – THERMAL RESPONSE



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – CAPACITANCE

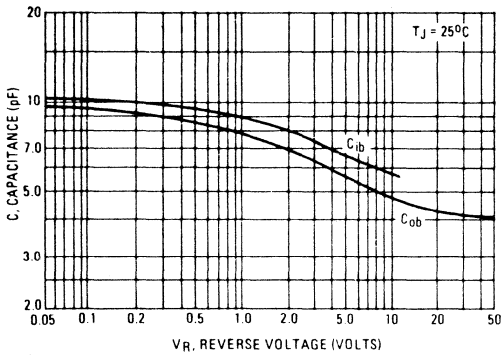
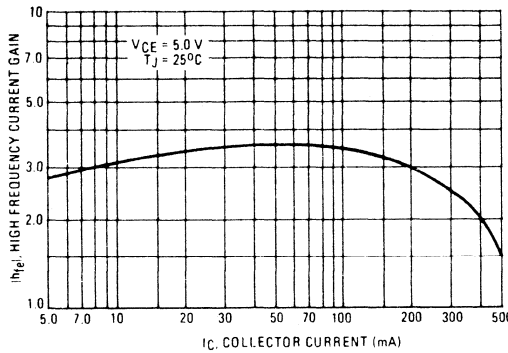


FIGURE 8 – HIGH-FREQUENCY CURRENT GAIN



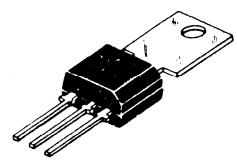
BD413
BD414

PNP SILICON DARLINGTON AMPLIFIER TRANSISTORS

. . . designed for amplifier and driver applications where high gain is an essential requirement, low power lamp and relay drivers and power drivers for high-current applications such as voltage regulators.

- High DC Current Gain –
  h_{FE} = 20,000 (Min) @ I_C = 200 mAdc – BD413
  = 15,000 (Min) @ I_C = 500 mAdc – BD414
- Collector-Emitter Breakdown Voltage –
  BV_{CES} = 40 Vdc (Min) @ I_C = 100 μAdc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.5 Vdc (Max) @ I_C = 1.0 Adc
- Duowatt Package –
  2 Watts Free Air Dissipation @ T_A = 25°C
- Complements to NPN BD411/412

PNP SILICON DARLINGTON AMPLIFIER TRANSISTORS



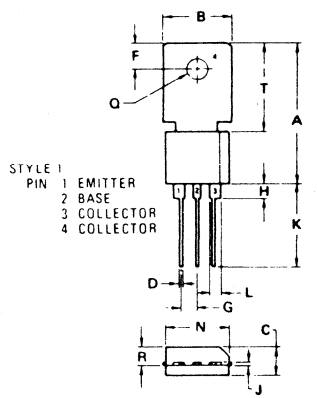
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Emitter Voltage	V_{CES}	40	Vdc
*Collector-Base Voltage	V_{CBO}	50	Vdc
*Emitter-Base Voltage	V_{EBO}	12	Vdc
*Collector Current – Continuous	I_C	2.0	Adc
*Base Current – Continuous	I_B	100	mAdc
*Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 16	Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80	Watts mW/°C
*Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C
*Solder Temperature, 1/16" from Case for 10 Seconds	–	260	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W

*Indicates JEDEC Registered Data.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

CASE 306-04

3

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

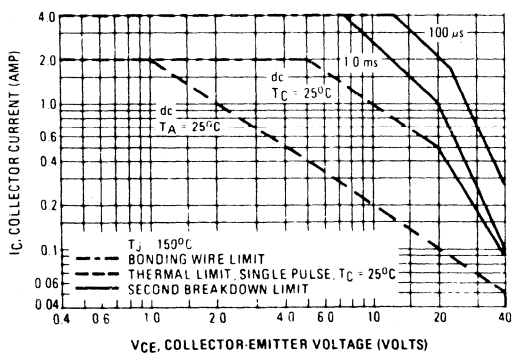
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 100 μAdc, V_{BE} = 0)		BV_{CES}	40	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)		BV_{CBO}	50	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)		BV_{EBO}	12	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)		I_{CBO}	–	100	nAdc
Emitter Cutoff Current (V_{EB} = 10 Vdc I_C = 0)		I_{EBO}	–	100	nAdc
ON CHARACTERISTICS(1)					
DC Current Gain		h_{FE}			–
(I_C = 200 mAdc, V_{CE} = 5.0 Vdc)	BD413		20,000	150,000	
	BD414		15,000	150,000	
(I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	BD413		15,000	–	
	BD414		10,000	–	
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	BD413		5,000	–	
	BD414		3,000	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 1.0 Adc, I_B = 2.0 mAdc)			–	1.5	
(I_C = 2.0 Adc, I_B = 4.0 mAdc)			–	2.0	
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 2.0 mAdc)		$V_{BE(sat)}$	–	2.0	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	–	2.0	Vdc
DYNAMIC CHARACTERISTICS					
High Frequency Current Gain (I_C = 200 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)		h_{fe}	0.5		–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{cb}	–	12	pF
Small-Signal Current Gain (I_C = 50 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	BD413	h_{fe}	20,000		
	BD414		15,000		

* Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

TYPICAL CHARACTERISTICS

FIGURE 1 – ACTIVE-REGION SAFE-OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A)

TYPICAL CHARACTERISTICS (continued)

FIGURE 2 – DC CURRENT GAIN

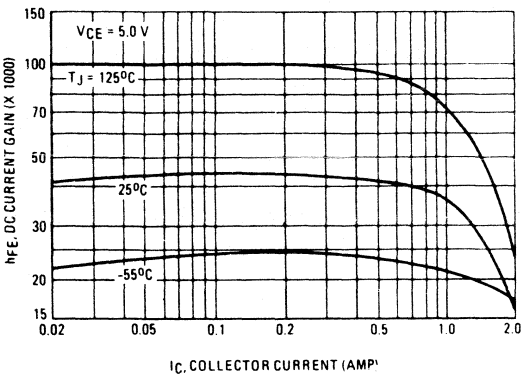


FIGURE 3 – "ON" VOLTAGES

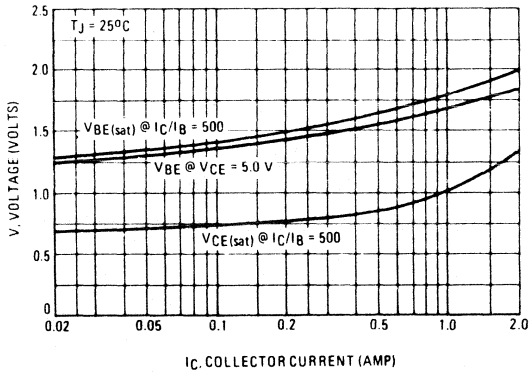


FIGURE 4 – COLLECTOR SATURATION REGION

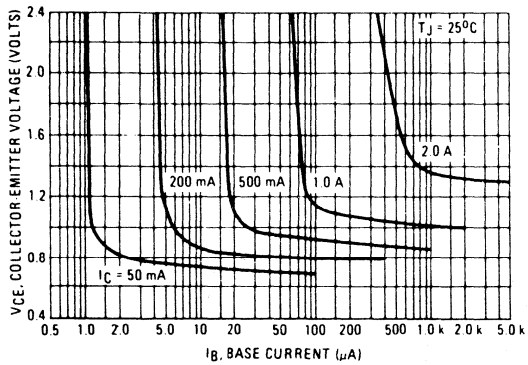


FIGURE 5 – TEMPERATURE COEFFICIENT

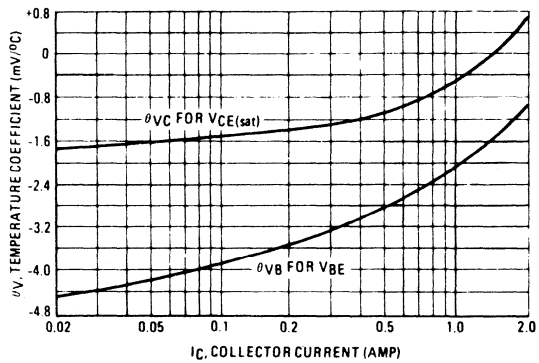
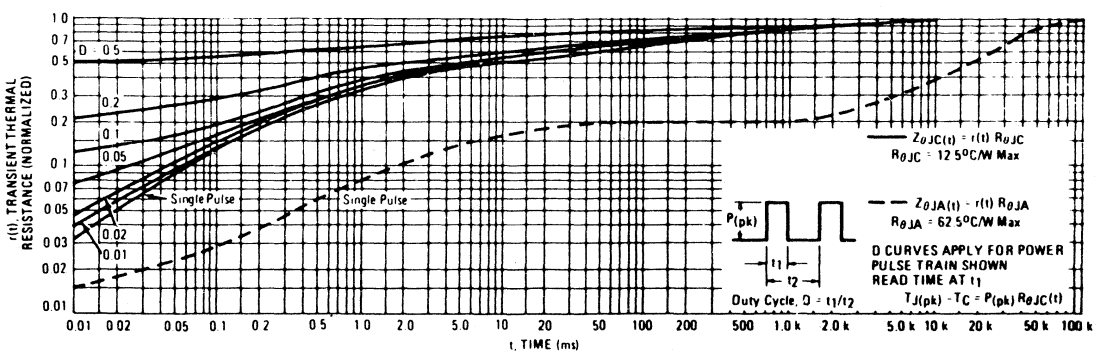


FIGURE 6 – THERMAL RESPONSE



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TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – CAPACITANCE

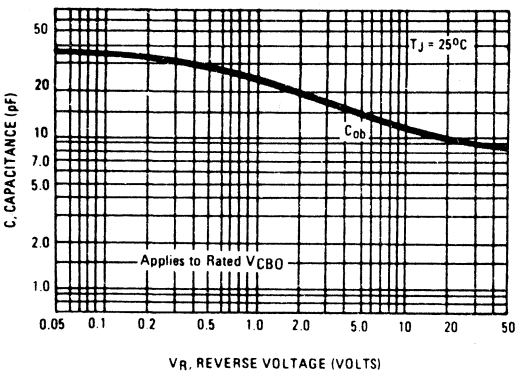
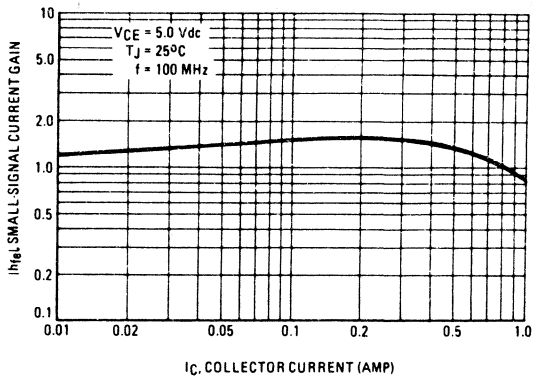


FIGURE 8 – HIGH-FREQUENCY CURRENT GAIN

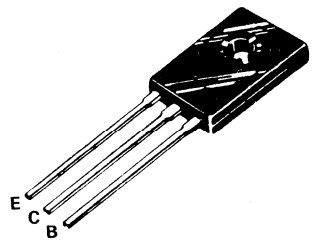


BD433, BD435, BD437, BD439, BD441

PLASTIC MEDIUM POWER SILICON
NPN TRANSISTOR

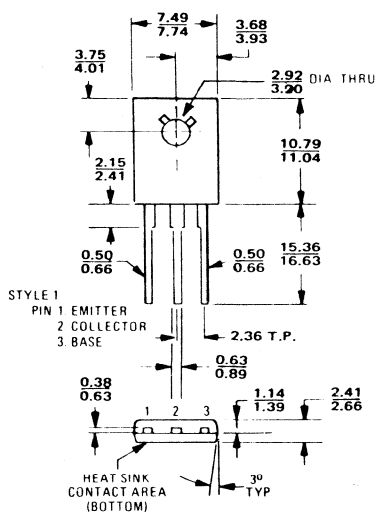
. . . for amplifier and switching applications Complementary types: BD434/436/438/440/442

4 AMPERE
POWER TRANSISTOR
NPN SILICON



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector Emitter Voltage	V_{CEO}	BD433 BD435 BD437 BD439 BD441	22 32 45 60 80	Vdc
Collector Base Voltage	V_{CBO}	BD433 BD435 BD437 BD439 BD441	22 32 45 60 80	Vdc
Emitter Base Voltage	V_{EBO}		5	Vdc
Collector current	I_C		4	Adc
Base Current	I_B		1	Adc
Total Device Dissipation $T_C = 25°C$ Derate above 25°C	P_D		 36 288	Watts mW/°C
Operating and Storage Junction Temperature range.	T_J, T_{stg}		−55 to +150	°C



When mounting the device, torque not to exceed 0.07 m-kg.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

All dimensions in millimeters

CASE 77-04

THERMAL CHARACTERISTICS

	Symbol	Max.	Unit
Thermal Resistance Junction to Case	θ_{JC}	3.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristics		Symbol	Min.	Typ.	Max.	Unit
Collector Emitter Breakdown Voltage (I_C = 100 mA, I_B = 0)	BD433	BV_{CEO}	22			Vdc
	BD435		32			
	BD437		45			
	BD439		60			
	BD441		80			
Collector Base Breakdown Voltage (I_C = 100 μA, I_B = 0)	BD433	BV_{CBO}	22			Vdc
	BD435		32			
	BD437		45			
	BD439		60			
	BD441		80			
Emitter Base Breakdown Voltage (I_E = 100 μA, I_C = 0)		BV_{EBO}	5			Vdc
Collector Cutoff Current						
(V_{CB} = 22 V, I_E = 0)	BD433				0.1	mAdc
(V_{CB} = 32 V, I_E = 0)	BD435				0.1	
(V_{CB} = 45 V, I_E = 0)	BD437				0.1	
(V_{CB} = 60 V, I_E = 0)	BD439				0.1	
(V_{CB} = 80 V, I_E = 0)	BD441				0.1	
Emitter Cutoff Current (V_{EB} = 5 V)		I_{EBO}			1	mAdc
DC Current Gain (I_C = 10 mA, V_{CE} = 5 V)	BD433	H_{FE}	40			
	BD435		40			
	BD437		30			
	BD439		20			
	BD441		15			
DC Current Gain (I_C = 500 mA, V_{CE} = 1 V)	BD433	H_{FE}	85			
	BD435		85			
	BD437		85			
	BD439		40			
	BD441		40			
DC Current Gain (I_C = 2 A, V_{CE} = 1 V)	BD433	H_{FE}	50			
	BD435		50			
	BD437		40			
	BD439		25			
	BD441		15			
Collector Saturation Voltage						
(I_C = 2 A, I_B = 0.2 A)	BD433	$V_{CE\ (sat)}$			0.5	Vdc
	BD435				0.5	
(I_C = 3 A, I_B = 0.3 A)	BD437				0.7	
	BD439				0.8	
	BD441				0.8	
Base – Emitter on voltage (I_C = 2 A, V_{CE} = 1 V)	**BD433/435/437**	$V_{BE(ON)}$			1.1	Vdc
	BD439/441				1.5	
Current Gain Bandwidth Product (V_{CE} = 1 V, I_C = 250 mA, f = 1 MHz)		f_T	3			MHz

FIGURE 1 – COLLECTOR SATURATION REGION

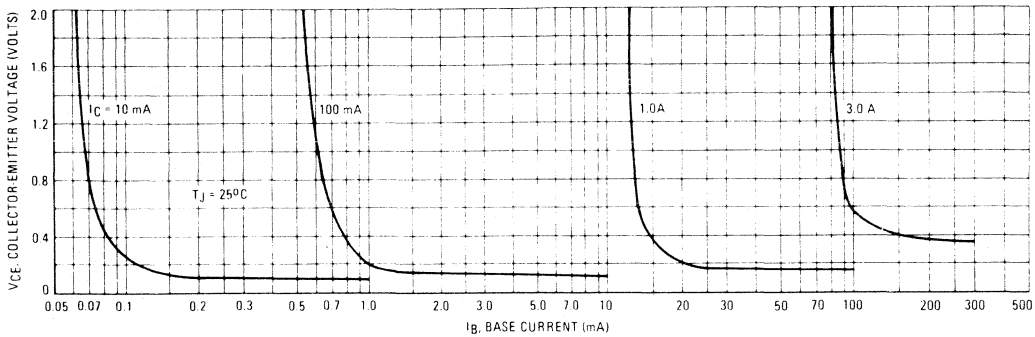


FIGURE 2 – CURRENT GAIN

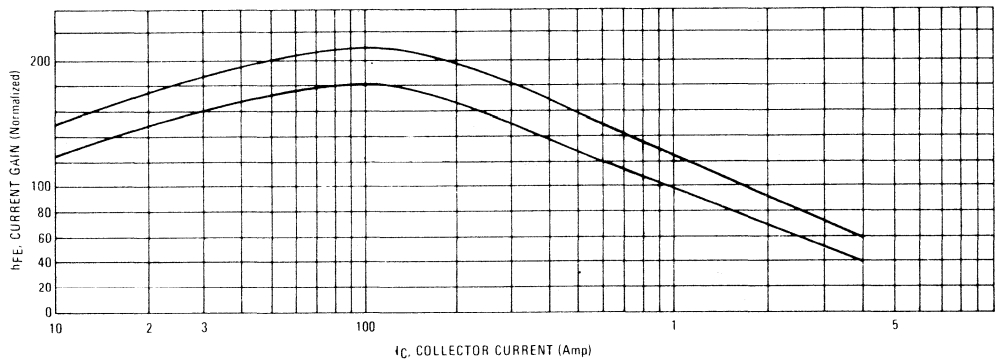


FIGURE 3 – "ON" VOLTAGE

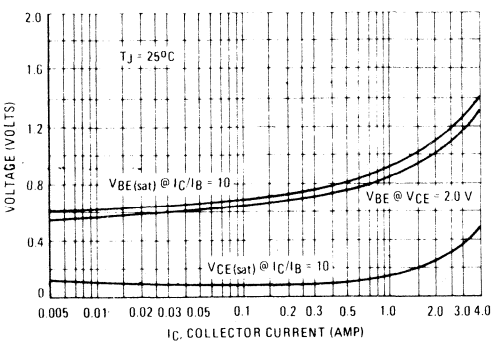
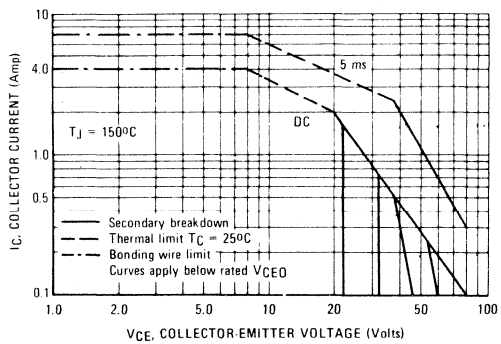


FIGURE 4 – ACTIVE REGION SAFE OPERATING AREA



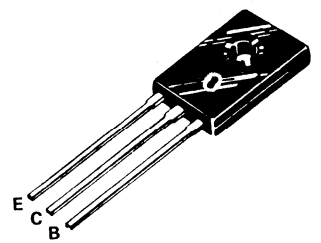
3

BD434, BD436, BD438, BD440, BD442

PLASTIC MEDIUM POWER SILICON
PNP TRANSISTOR

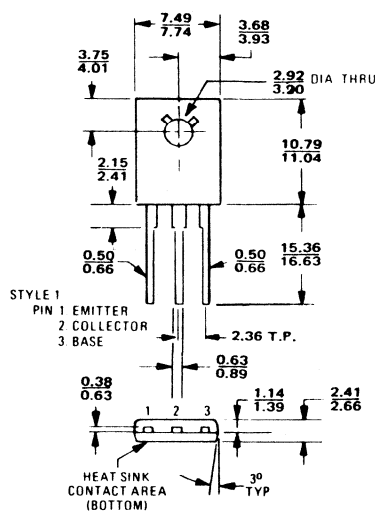
. . . for amplifier and switching applications Complementary types: BD433/435/437/439/441.

4 AMPERE
POWER TRANSISTOR
PNP SILICON



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector Emitter Voltage	V_{CEO}	BD434 BD436 BD438 BD440 BD442	22 32 45 60 80	Vdc
Collector Base Voltage	V_{CBO}	BD434 BD436 BD438 BD440 BD442	22 32 45 60 80	Vdc
Emitter Base Voltage	V_{EBO}		5	Vdc
Collector current	I_C		4	Adc
Base Current	I_B		1	Adc
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D		 36 288	Watts mW/°C
Operating and Storage Junction Temperature range.	T_J, T_{stg}		−55 to +150	°C



When mounting the device, torque not to exceed 0.07 m-kg

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

All dimensions in millimeters

CASE 77-04

THERMAL CHARACTERISTICS

	Symbol	Max.	Unit
Thermal Resistance Junction to Case	θJ_C	3.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristics		Symbol	Min.	Typ.	Max.	Unit
Collector Emitter Breakdown Voltage (I_C = 100 mA, I_B = 0)	BD434	BV_{CEO}	22			Vdc
	BD436		32			
	BD438		45			
	BD440		60			
	BD442		80			
Collector Base Breakdown Voltage (I_C = 100 μA, I_B = 0)	BD434	BV_{CBO}	22			Vdc
	BD436		32			
	BD438		45			
	BD440		60			
	BD442		80			
Emitter Base Breakdown Voltage (I_E = 100 μA, I_C = 0)		BV_{EBO}	5			Vdc
Collector Cutoff Current						
(V_{CB} = 22 V, I_E = 0)	BD434				0.1	mAdc
(V_{CB} = 32 V, I_E = 0)	BD436				0.1	
(V_{CB} = 45 V, I_E = 0)	BD438				0.1	
(V_{CB} = 60 V, I_E = 0)	BD440				0.1	
(V_{CB} = 80 V, I_E = 0)	BD442				0.1	
Emitter Cutoff Current (V_{EB} = 5 V)		I_{EBO}			1	mAdc
DC Current Gain (I_C = 10 mA, V_{CE} = 5 V)	BD434	H_{FE}	40			
	BD436		40			
	BD438		30			
	BD440		20			
	BD442		15			
DC Current Gain (I_C = 500 mA, V_{CE} = 1 V)	BD434	H_{FE}	85			
	BD436		85			
	BD438		85			
	BD440		40			
	BD442		40			
DC Current Gain (I_C = 2 A, V_{CE} = 1 V)	BD434	H_{FE}	50			
	BD436		50			
	BD438		40			
	BD440		25			
	BD442		15			
Collector Saturation Voltage (I_C = 2 A, I_B = 0.2 A)	BD434	$V_{CE\ (sat)}$			0.5	Vdc
	BD436				0.5	
(I_C = 3 A, I_B = 0.3 A)	BD438				0.7	
	BD440				0.8	
	BD442				0.8	
Base—Emitter on voltage (I_C = 2 A, V_{CE} = 1 V)	BD434/436/438	$V_{BE(ON)}$			1.1	Vdc
	BD440/442				1.5	
Current Gain Bandwidth Product (V_{CE} = 1 V, I_C = 250 mA, f = 1 MHz)		f_T	3			MHz

3

FIGURE 1 – COLLECTOR SATURATION REGION

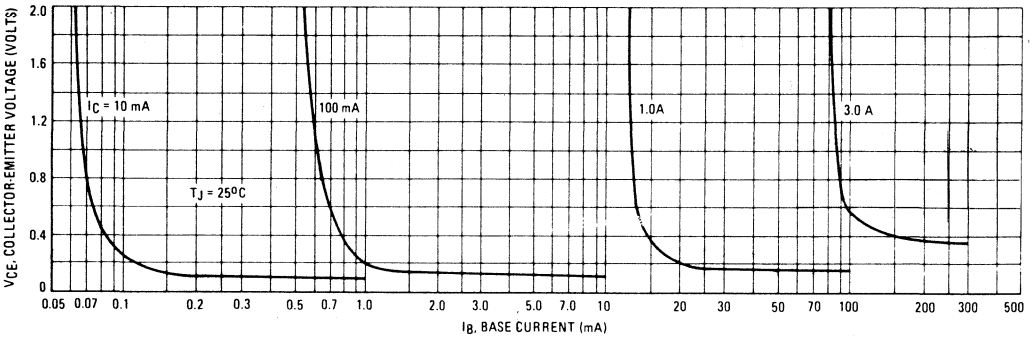


FIGURE 2 – CURRENT GAIN

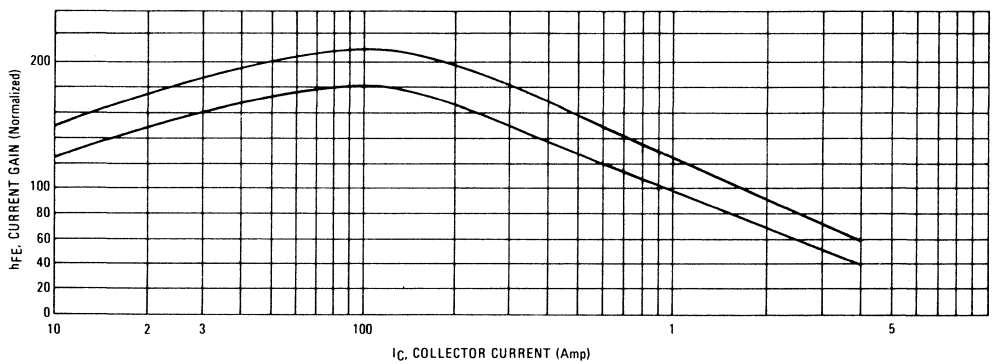


FIGURE 3 – "ON" VOLTAGE

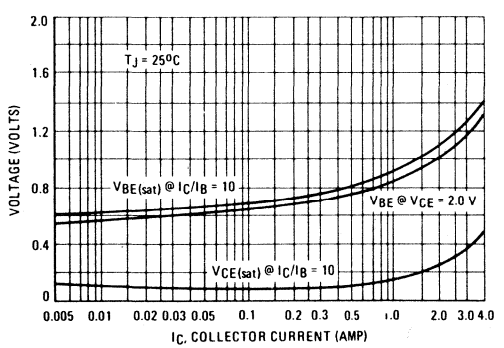
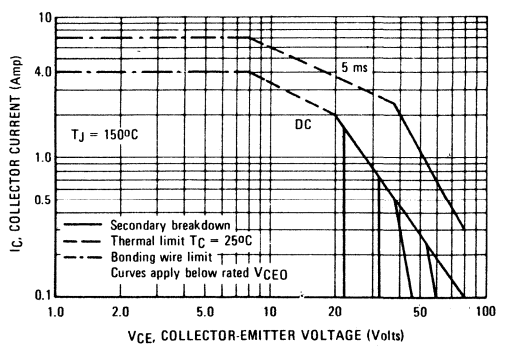


FIGURE 4 – ACTIVE REGION SAFE OPERATING AREA



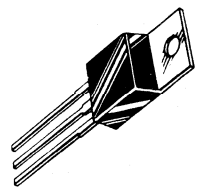
NPN BD533 BD535 BD537
PNP BD534 BD536 BD538

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in general purpose amplifier and switching applications.

- Collector-Emitter Saturation Voltage –
  V_{CE} = 0.8 Vdc (Max) @ I_C = 2.0 Adc
- Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 45 Vdc (Min) BD533, BD534
  = 60 Vdc (Min) BD535, BD536
  = 80 Vdc (Min) BD537, BD538
- High Current Gain – Bandwidth Product
  f_T = 3.0 MHz (Min) @ I_C = 250 mAdc
- Compact TO-220 AB Package
- TO-66 Leadform Also Available ordered with "–66" suffix

4 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
45, 60, 80 VOLTS
50 WATTS



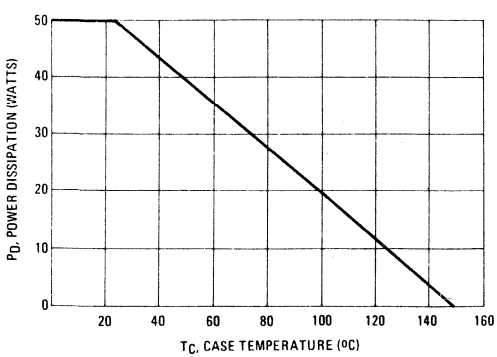
MAXIMUM RATINGS

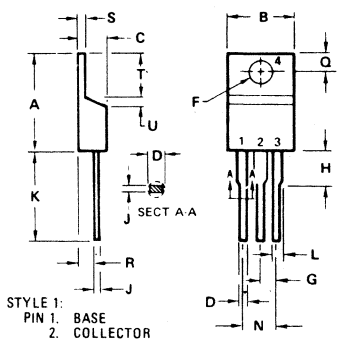
Rating	Symbol	BD533 BD534	BD535 BD536	BD537 BD538	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current - Continuous	I_C	4.0			Adc
Peak		8.0			
Base Current	I_B	1.0			Adc
Total Device Dissipation @ T_C = 25°C	P_D	50			Watts
Derate above 25°C		0.4			W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

3

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic		Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage[1]		$V_{CEO(sus)}$			Vdc
(I_C = 0.1 Adc, I_B = 0)	BD533, BD534		45		
	BD535, BD536		60		
	BD537, BD538		80		
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 45 Vdc, I_E = 0)	BD533, BD534			0.1	
(V_{CB} = 60 Vdc, I_E = 0)	BD535, BD536			0.1	
(V_{CB} = 80 Vdc, I_E = 0)	BD537, BD538			0.1	
Collector Cutoff Current		I_{CES}			μAdc
(V_{CE} = 45 Vdc, V_{EB} = 0)	BD533, BD534			100	
(V_{CE} = 60 Vdc, V_{EB} = 0)	BD535, BD536			100	
(V_{CE} = 80 Vdc, V_{EB} = 0)	BD537, BD538			100	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)				1.0	
ON CHARACTERISTICS[1]					
DC Current Gain		h_{FE}			
(I_C = 10 mAdc, V_{CE} = 5 Vdc)	BD533, BD534		20		
	BD535, BD536		20		
	BD537, BD538		15		
(I_C = 500 mAdc, V_{CE} = 2 Vdc)			40		
(I_C = 2 Adc, V_{CE} = 2 Vdc)	BD533, BD534		25		
	BD535, BD536		25		
	BD537, BD538		15		
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)				0.8	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)				1.5	
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product[2]		f_T			MHz
(I_C = 250 mAdc, V_{CE} = 1 Vdc, f_{test} = 1 MHz)			3.0		

[1] Pulse test = Pulse width ⩽300 μs, Duty Cycle ⩽2.0%.
[2] $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 – SWITCHING TIME EQUIVALENT CIRCUIT

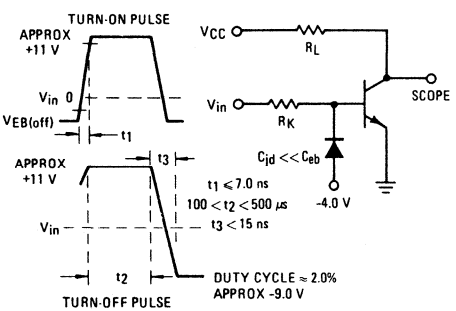


FIGURE 3 – TURN-ON TIME

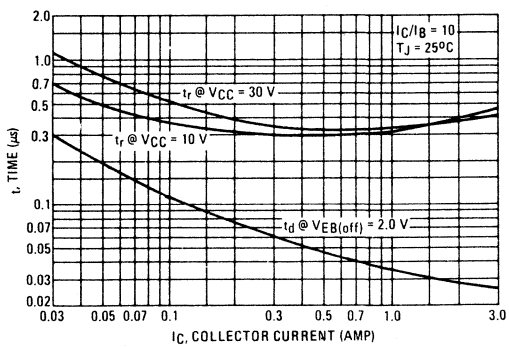


FIGURE 4 – THERMAL RESPONSE

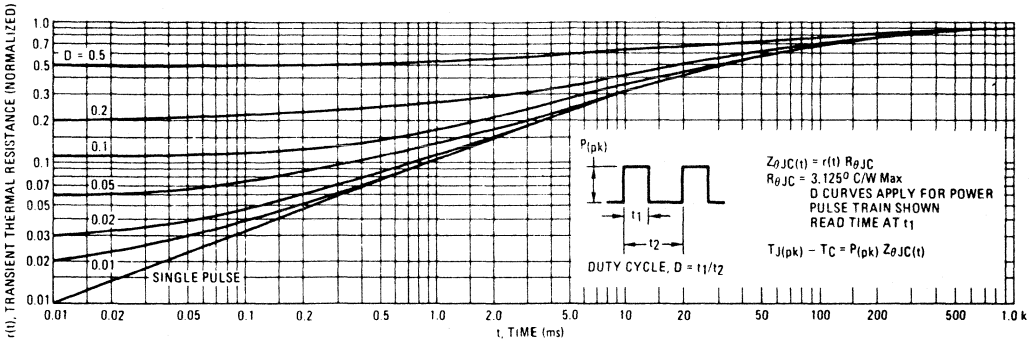
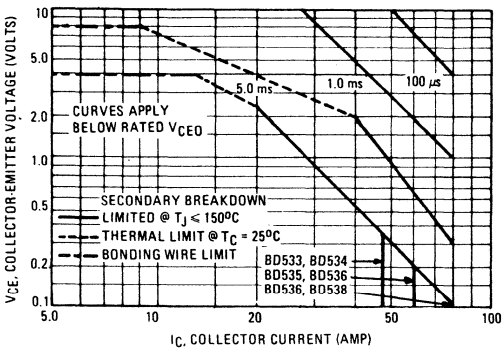


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

FIGURE 6 – TURN-OFF TIME

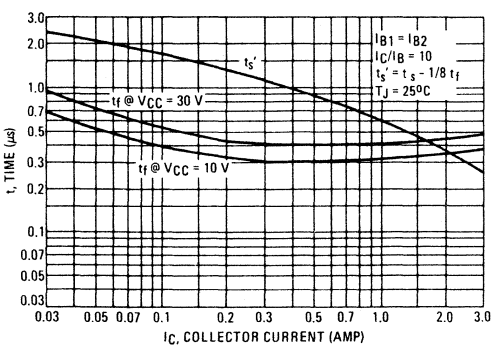


FIGURE 7 – CAPACITANCE

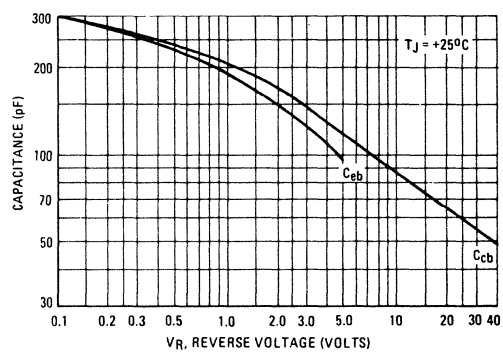


FIGURE 8 – DC CURRENT GAIN

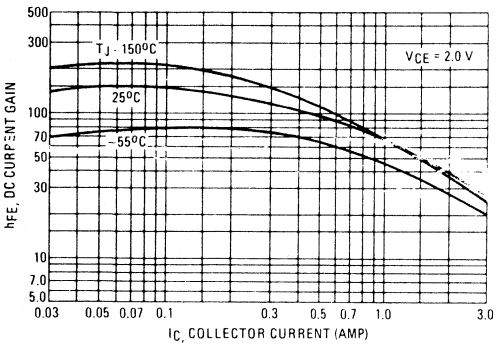


FIGURE 9 – COLLECTOR SATURATION REGION

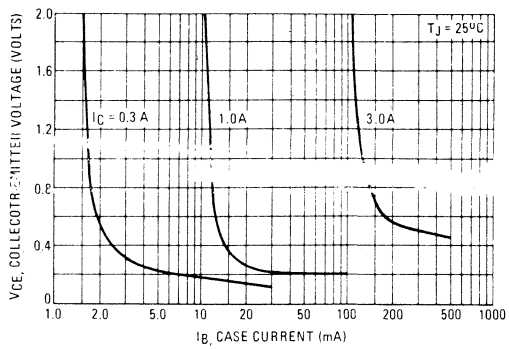


FIGURE 10 – "ON" VOLTAGES

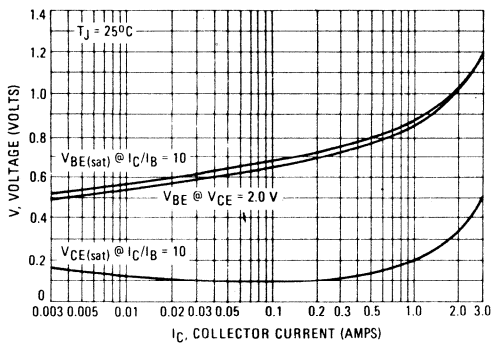


FIGURE 11 – TEMPERATURE COEFFICIENTS

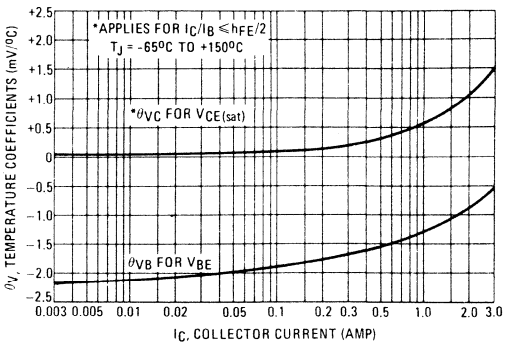


FIGURE 12 – COLLECTOR CUT-OFF REGION

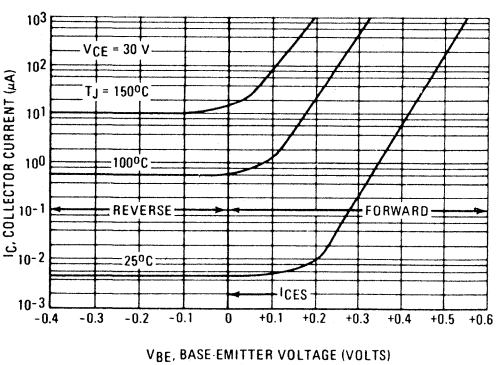
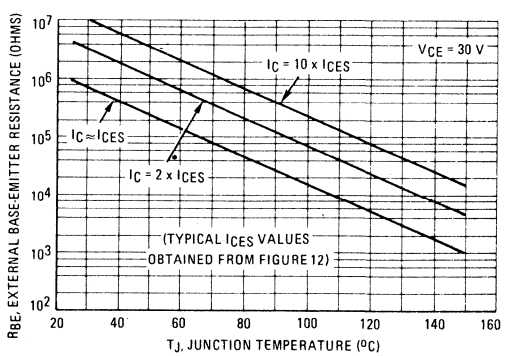


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



BD675, 675A
BD677, 677A
BD679, 679A
BD681

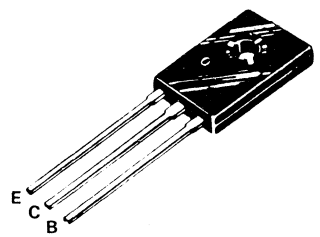
PLASTIC MEDIUM-POWER SILICON NPN DARLINGTONS

. . . for use as output devices in complementary general-purpose amplifier applications.

- High DC Current Gain – h_{FE} = 750 (Min) @ I_C = 1.5 and 2.0 Adc
- Monolithic Construction
- BD675, 675A, 677, 677A, 679, 679A, 681 are complementary with BD676, 676A, 678, 678A, 680, 680A, 682
- BD 677, 677A, 679, 679A are equivalent to MJE 800, 801, 802, 803

4.0 AMPERE
DARLINGTON
POWER TRANSISTORS
NPN SILICON

45, 60, 80, 100 VOLTS
40 WATTS



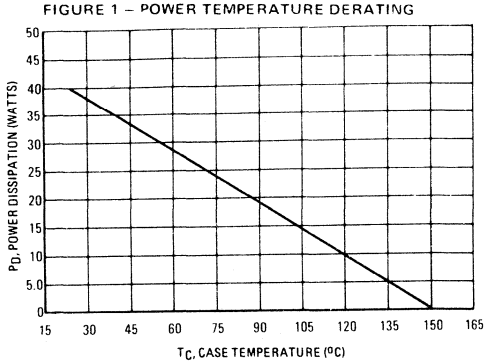
MAXIMUM RATINGS

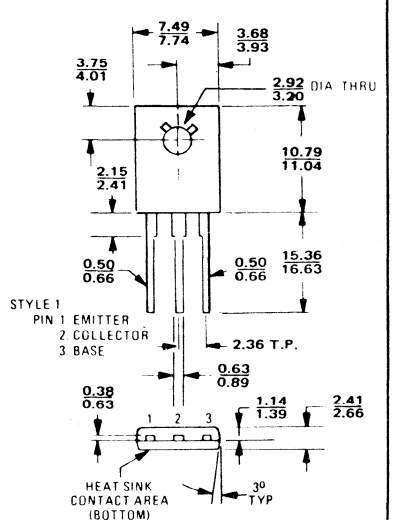
Rating	Symbol	BD675 BD675A	BD677 BD677A	BD679 BD679A	BD681	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current	I_C	4.0				Adc
Base Current	I_B	0.1				Adc
Total Device Dissipation @ T_C = 25 °C Derate above 25 °C	P_D	40 0.32				Watts W/°C
Operating and Storage Junction Temperating Range	T_J, T_{stg}	−55 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.13	°C/W

FIGURE 1 – POWER TEMPERATURE DERATING





When mounting the device, torque not to exceed 0.07 m-kg

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend

All dimensions in millimeters

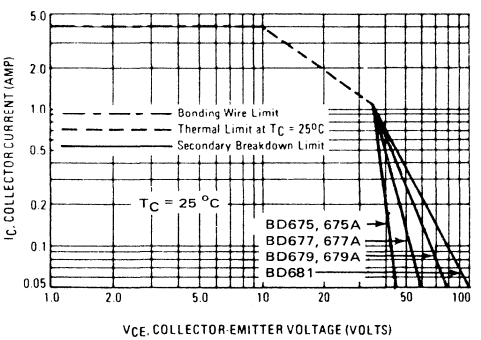
CASE 77-04

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 50 mAdc, I_B = 0)	BD675, 675A BD677, 677A BD679, 679A BD681	BV_{CEO}	45 60 80 100	– – – –	Vdc
Collector Cutoff Current (V_{CE} = Half Rated V_{CEO}, I_B = 0)		I_{CEO}	–	500	μAdc
Collector Cutoff Current (V_{CB} = Rated BV_{CEO}, I_E = 0) (V_{CB} = Rated BV_{CEO}, I_E = 0, T_C = 100°C)		I_{CBO}	– –	0.2 2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain(1) (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	BD675, 677, 679, 681 BD 675A, 677A, 679A	h_{FE}	750 750	– –	–
Collector-Emitter Saturation Voltage(1) (I_C = 1.5 Adc, I_B = 30 mAdc) (I_C = 2.0 Adc, I_B = 40 mAdc)	BD 677, 679 BD 675A, 677A, 679A	$V_{CE(sat)}$	– –	2.5 2.8	Vdc
Base-Emitter On Voltage(1) (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	BD 677, 679 BD 675A, 677A, 679A	$V_{BE(on)}$	– –	2.5 2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		h_{fe}	1.0	–	–

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

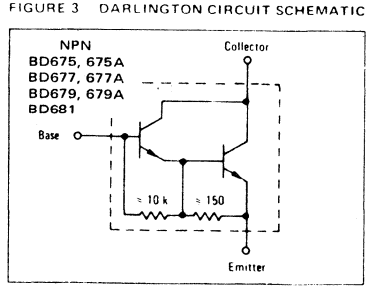
FIGURE 2 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown. (See AN-415)

FIGURE 3 DARLINGTON CIRCUIT SCHEMATIC



BD676, 676A
BD678, 678A
BD680, 680A
BD682

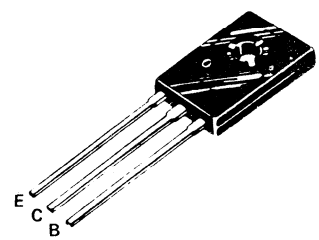
PLASTIC MEDIUM-POWER SILICON PNP DARLINGTONS

. . . for use as output devices in complementary general-purpose amplifier applications.

- High DC Current Gain – h_{FE} = 750 (Min) @ I_C = 1.5 and 2.0 Adc
- Monolithic Construction
- BD676, 676A, 678, 678A, 680, 680A, 682 are complementary with BD675, 675A, 677, 677A, 679, 679A, 681
- BD 678, 678A, 680, 680A are equivalent to MJE 700, 701, 702, 703

4.0 AMPERE
DARLINGTON POWER TRANSISTORS PNP SILICON

45, 60, 80, 100 VOLTS
40 WATTS



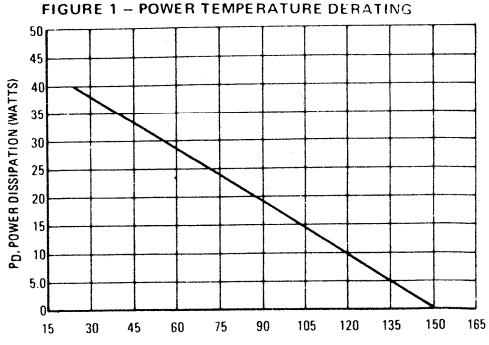
MAXIMUM RATING

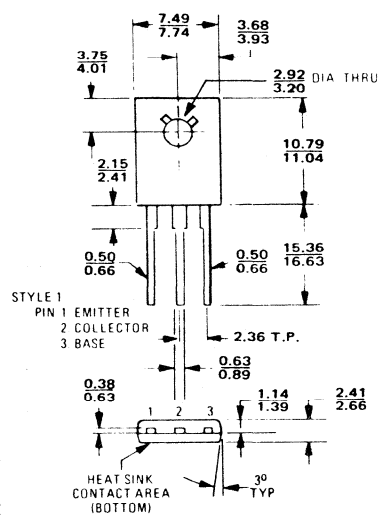
Rating	Symbol	BD676 BD676A	BD678 BD678A	BD680 BD680A	BD682	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current	I_C	4.0				Adc
Base Current	I_B	0.1				Adc
Total Device Dissipation @ T_C = 25 °C Derate above 25 °C	P_D	40 0.32				Watts W/°C
Operating and Storage Junction Temperating Range	T_J, T_{stg}	−55 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.13	°C/W

FIGURE 1 – POWER TEMPERATURE DERATING





When mounting the device, torque not to exceed 0.07 m-kg

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend

All dimensions in millimeters

CASE 77-04

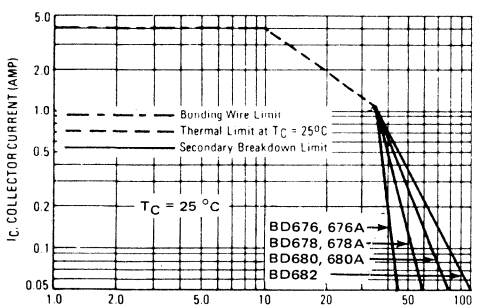
3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 50 mAdc, I_B = 0)	BD676, 676A BD678, 678A BD680, 680A BD682	BV_{CEO}	45 60 80 100	– – – –	Vdc
Collector Cutoff Current (V_{CE} = Half Rated V_{CEO}, I_B = 0)		I_{CEO}	–	500	μAdc
Collector Cutoff Current (V_{CB} = Rated BV_{CEO}, I_E = 0) (V_{CB} = Rated BV_{CEO}, I_E = 0, T_C = 100°C)		I_{CBO}	– –	0.2 2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain(1) (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	BD676, 678, 680, 682 BD 676A, 678A, 680A	h_{FE}	750 750	– –	–
Collector-Emitter Saturation Voltage(1) (I_C = 1.5 Adc, I_B = 30 mAdc) (I_C = 2.0 Adc, I_B = 40 mAdc)	BD 678, 680 BD 676A, 678A, 680A	$V_{CE(sat)}$		2.5 2.8	Vdc
Base-Emitter On Voltage(1) (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	BD 678, 680 BD 676A, 678A, 680A	$V_{BE(on)}$	– –	2.5 2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		h_{fe}	1.0	–	–

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

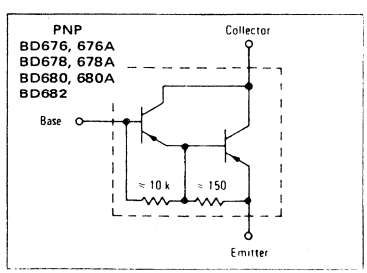
FIGURE 2 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown. (See AN-415)

FIGURE 3 – DARLINGTON CIRCUIT SCHEMATIC



NPN

BD 785 BD 787

PNP

BD 786 BD 788

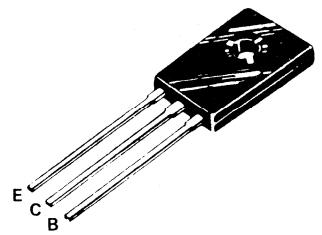
COMPLEMENTARY PLASTIC SILICON ANNULAR♦ POWER TRANSISTORS

. . . designed for low power audio amplifier and low current, high-speed switching applications.

- Low Collector-Emitter Sustaining Voltage –
  V_{CEO} (sus) 45 Vdc (Min) – BD785, BD786
  60 Vdc (Min) – BD787, BD788
- High Current-Gain – Bandwidth Product –
  f_T = 50 MHz (Min) @ I_C = 100 mAdc
- DC Current Gain Specified at 0.2, 1.0, 2.0 and 4.0 Adc
- Collector-Emitter Saturation Voltage Specified at 0.5, 1.0, 2.0 and 4.0 Adc

4 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON

45, 60 VOLTS
15 WATTS



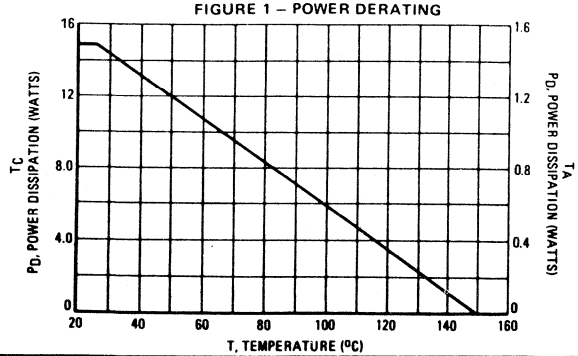
*MAXIMUM RATINGS

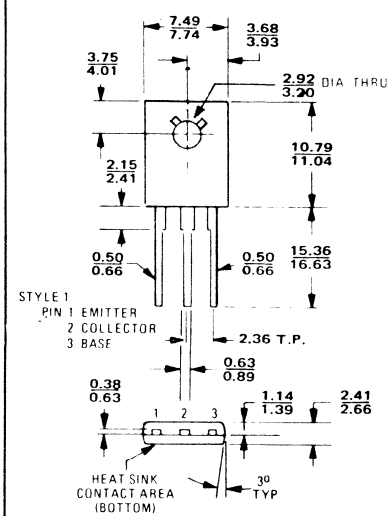
Rating	Symbol	BD785 BD786	BD787 BD788	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	Vdc
Collector-Base Voltage	V_{CBO}	60	80	Vdc
Emitter-Base Voltage	V_{EBO}	6.0		Vdc
Collector Current – Continuous – Peak	I_C	4.0 8.0		Adc Adc
Base Current	I_B	1.0		Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	15 0.12		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.34	°C/W

FIGURE 1 – POWER DERATING





When mounting the device, torque not to exceed 0.07 m-kg

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend

All dimensions in millimeters

CASE 77-04

3

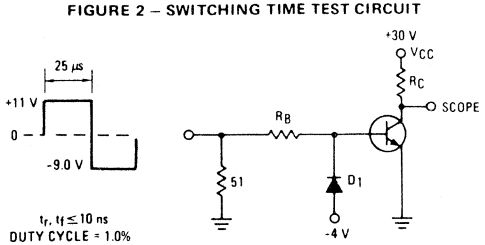
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 10 mAdc, I_B = 0)	BD785, BD786		45	–	
	BD787, BD788		60	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 20 Vdc, I_B = 0)	BD785, BD786		–	100	
(V_{CE} = 30 Vdc, I_B = 0)	BD787, BD788		–	100	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	BD785, BD786		–	1.0	μAdc
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	BD787, BD788		–	1.0	
(V_{CE} = 30 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	BD785, BD786		–	0.1	mAdc
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C	BD787, BD788		–	0.1	
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 200 mAdc, V_{CE} = 3.0 Vdc)			40	250	
(I_C = 1.0 Adc, V_{CE} = 3.0 Vdc)			25	–	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)			20	–	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			5.0	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)			–	0.4	
(I_C = 1.0 Adc, I_B = 100 mAdc)			–	0.6	
(I_C = 2.0 Adc, I_B = 200 mAdc)			–	0.8	
(I_C = 4.0 Adc, I_B = 800 mAdc)			–	2.5	
Base-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 200 mAdc)		$V_{BE(sat)}$	–	2.0	Vdc
Base-Emitter on Voltage (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)		f_T	50	–	MHz
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_C = 0)	BD785, BD787		–	50	
f = 0.1 MHz)	BD786, BD788		–	70	
Small-Signal Current Gain (I_C = 200 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	10	–	–

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg
MBD5300 USED ABOVE I_B ≈100 mA
MSD6100 USED BELOW I_B ≈100 mA

FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

FIGURE 3 – TURN-ON TIME

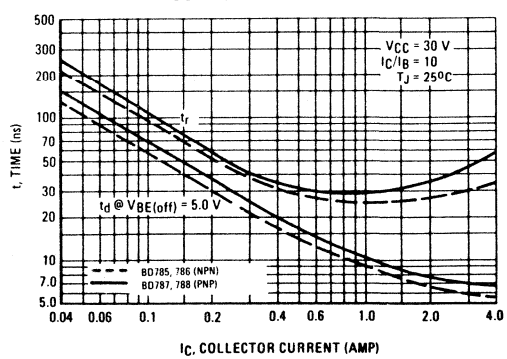


FIGURE 4 – THERMAL RESPONSE

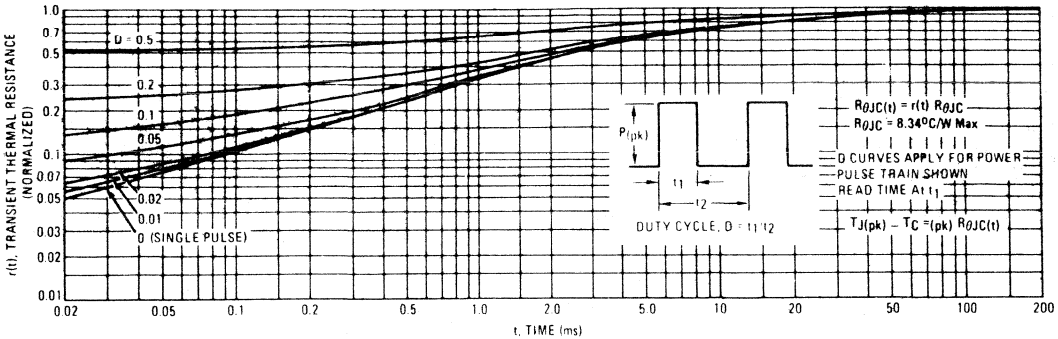
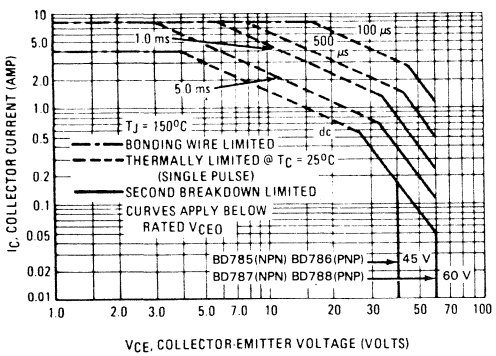


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A)

FIGURE 6 – TURN-OFF TIME

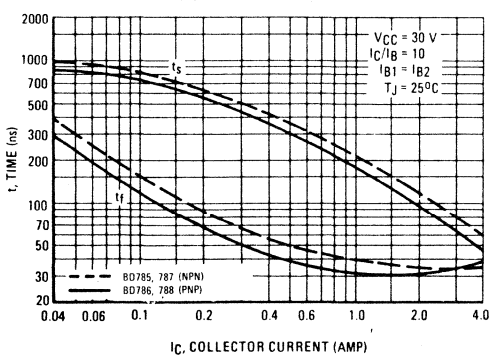
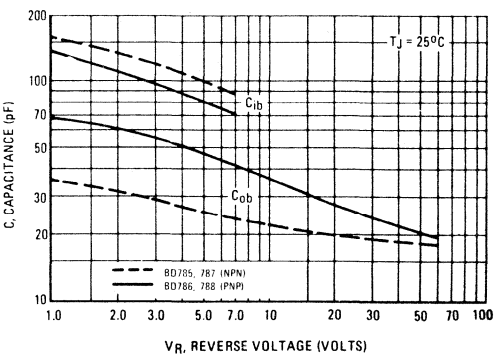


FIGURE 7 – CAPACITANCE

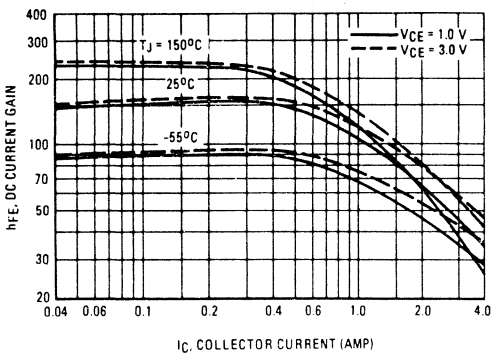


3

NPN
BD785, BD787

PNP
BD786, BD788

FIGURE 8 – DC CURRENT GAIN



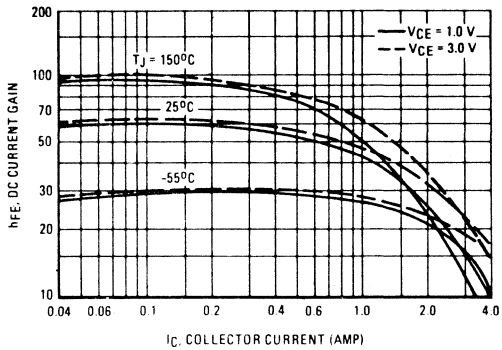
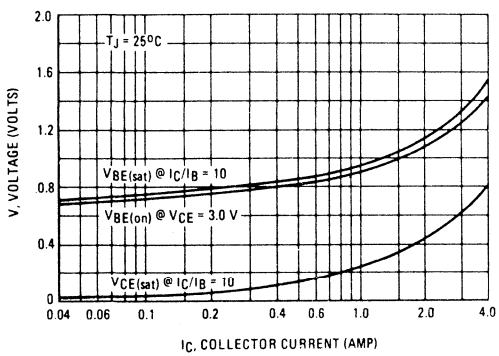


FIGURE 9 – "ON" VOLTAGES



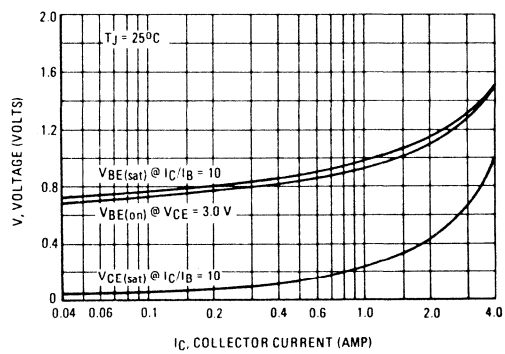
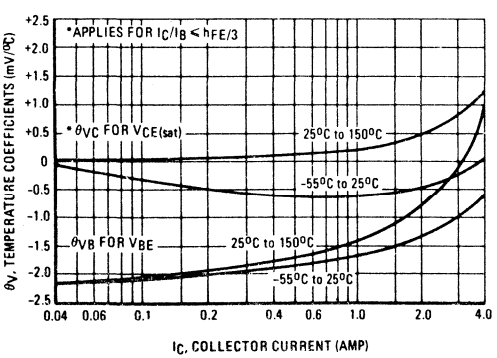
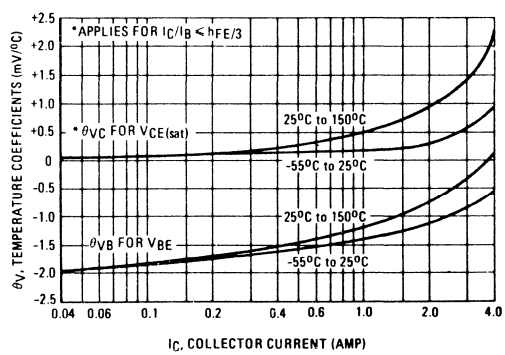


FIGURE 10 – TEMPERATURE COEFFICIENTS





NPN

BD 789 BD 791

PNP

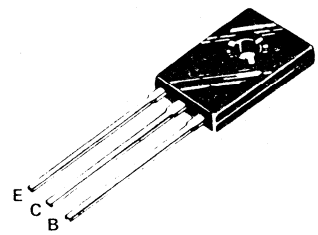
BD 790 BD 792

COMPLEMENTARY PLASTIC SILICON ANNULAR♦ POWER TRANSISTORS

. . . designed for low power audio amplifier and low-current, high speed switching applications.

- High Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 80 Vdc (Min) – BD789, BD790
  = 100 Vdc (Min) –BD791, BD792
- High DC Current Gain @ I_C = 200 mAdc
  h_{FE} = 40-250
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.5 Vdc (Max) @ I_C = 500 mAdc
- High Current Gain – Bandwidth Product –
  f_T = 40 MHz (Min) @ I_C = 100 mAdc)

4 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
80, 100 VOLTS
15 WATTS



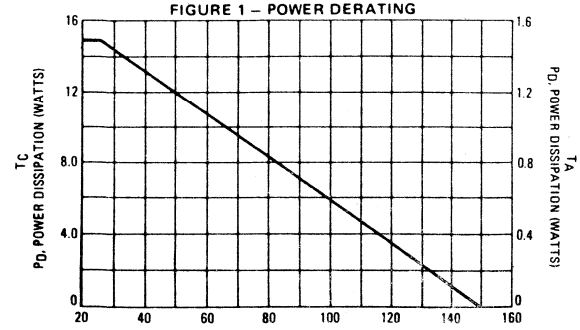
*MAXIMUM RATINGS

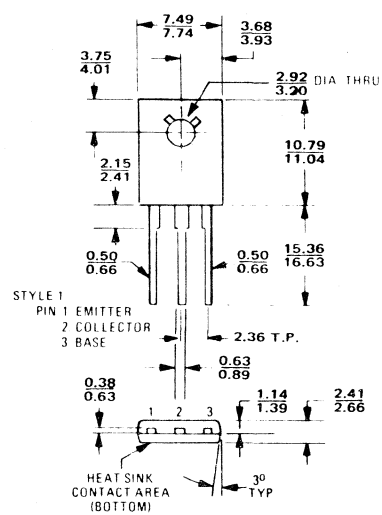
Rating	Symbol	BD789 BD790	BD791 BD792	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EBO}	6.0		Vdc
Collector Current – Continuous – Peak	I_C	4.0 8.0		Adc
Base Current	I_B	1.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12		Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.34	°C/W

FIGURE 1 – POWER DERATING





When mounting the device, torque not to exceed 0.07 m-kg

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend

All dimensions in millimeters

CASE 77-04

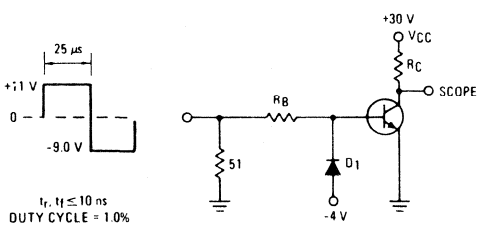
3

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 10 mAdc, I_B = 0)	BD789, BD790		80	–	
	BD791, BD792		100	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 40 Vdc, I_B = 0)	BD789, BD790		–	100	
(V_{CE} = 50 Vdc, I_B = 0)	BD791, BD792		–	100	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	BD789, BD790		–	1.0	μAdc
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	BD791, BD792		–	1.0	
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	BD789, BD790		–	0.1	mAdc
(V_{CE} = 50 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	BD791, BD792		–	0.1	
Emitter Cutoff Current		I_{EBO}	–	1.0	μAdc
(V_{EB} = 6.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 200 mAdc, V_{CE} = 3.0 Vdc)			40	250	
(I_C = 1.0 Adc, V_{CE} = 3.0 Vdc)			20	–	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)			10	–	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			5.0	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)			–	0.5	
(I_C = 1.0 Adc, I_B = 100 mAdc)			–	1.0	
(I_C = 2.0 Adc, I_B = 200 mAdc)			–	2.5	
(I_C = 4.0 Adc, I_B = 800 mAdc)			–	3.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$	–	1.8	Vdc
(I_C = 2.0 Adc, I_B = 200 mAdc)					
Base-Emitter On Voltage		$V_{BE(on)}$	–	1.5	Vdc
(I_C = 200 mAdc, V_{CE} = 3.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product		f_T	40	–	MHz
(I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)					
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_C = 0, f = 0.1 MHz	BD789, BD791		–	50	
	BD790, BD792		–	70	
Small-Signal Current Gain		h_{fe}	10	–	–
(I_C = 200 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)					

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE I_B ≈100 mA
MSD6100 USED BELOW I_B ≈100 mA

FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

FIGURE 3 – TURN-ON TIME

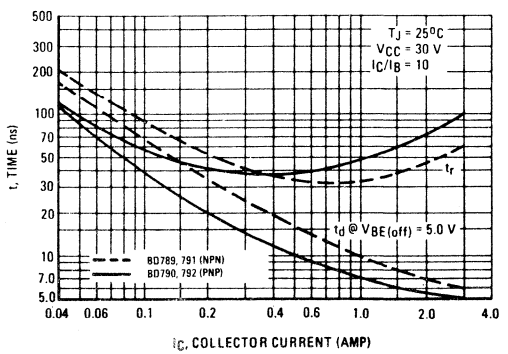


FIGURE 4 – THERMAL RESPONSE

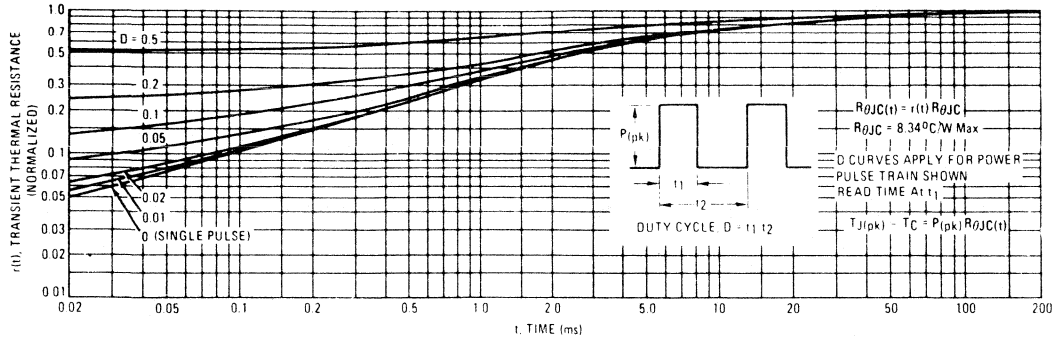
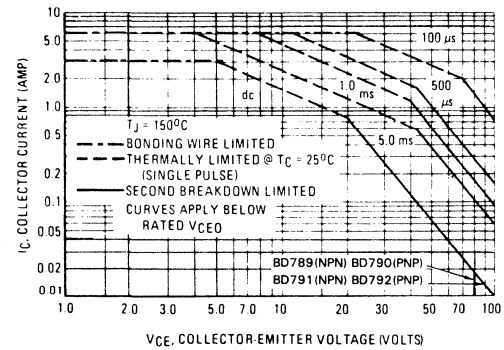


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A)

FIGURE 6 – TURN-OFF TIME

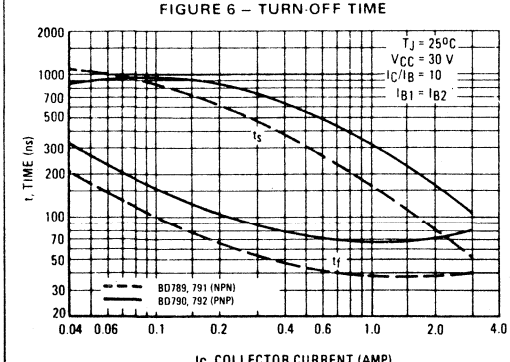
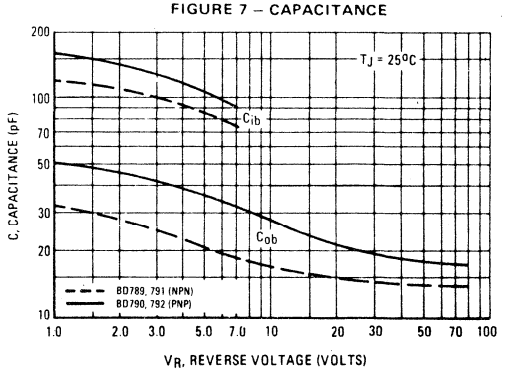


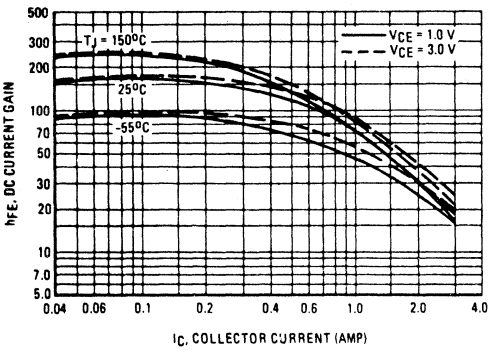
FIGURE 7 – CAPACITANCE



NPN
BD789, BD791

PNP
BD790, BD792

FIGURE 8 – DC CURRENT GAIN



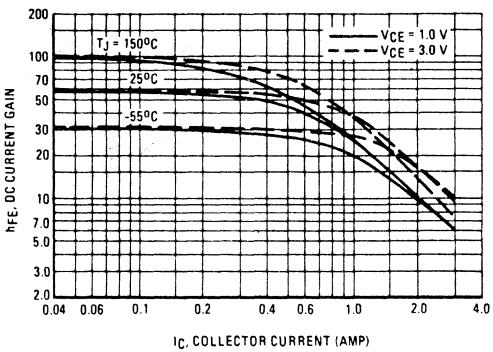
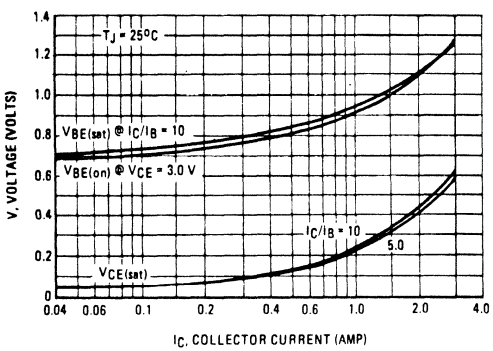


FIGURE 9 – "ON" VOLTAGES



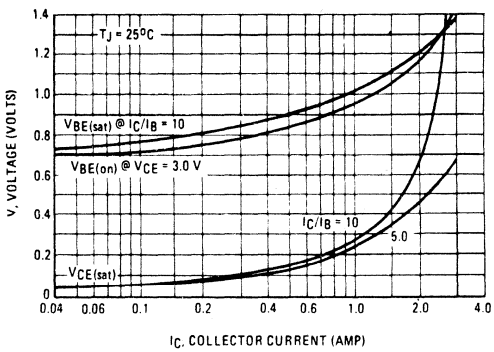
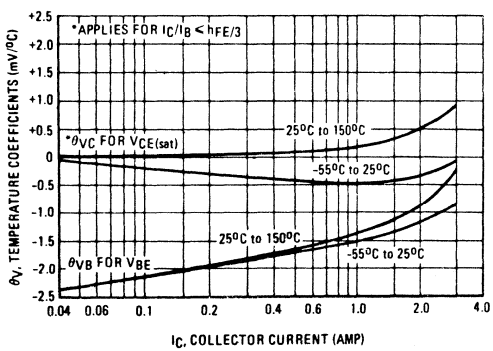
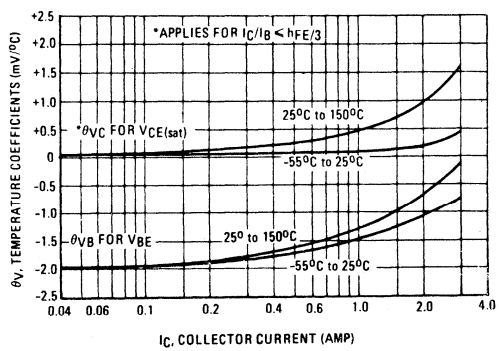


FIGURE 10 – TEMPERATURE COEFFICIENTS





BD795 • BD797
BD799 • BD801

PLASTIC HIGH POWER SILICON NPN TRANSISTOR

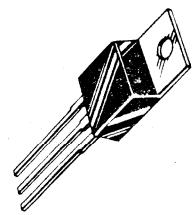
. . . designed for use up to 30 Watt audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 1.0 Adc
- BD 795, 797, 799, 801 are complementary with BD 796, 798, 800, 802

8 AMPERE POWER TRANSISTOR

NPN SILICON

45, 60, 80, 100 VOLTS
65 WATTS



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD795 BD797 BD799 BD801	45 60 80 100	Vdc
Collector-Base Voltage	V_{CBO}	BD795 BD797 BD799 BD801	45 60 80 100	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		8	Adc
Base Current	I_B		3	Adc
Total Device Dissipation T_C=25°C Derate avove 25°C	P_D		65 522	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		—55 to +150	°C

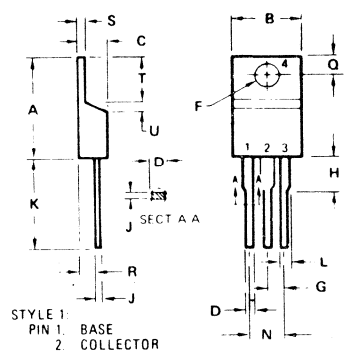
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		1.92	° C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0) (I_C = 0.05 Adc, I_B = 0)	BV_{CEO}*	BD795 BD797 BD799 BD801	45 60 80 100	— — — —	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	BD795 BD797 BD799 BD801	— — — —	0.1 0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 1 A, V_{CE} = 2 V) (I_C = 3 A, V_{CE} = 2 V)	h_{FE}*	BD 795/797 BD 799/801 BD 795/797 BD 799/801	40 30 25 15	— — — —	
Collector-Emitter Saturation Voltage* (I_C = 3 Adc, I_B = 0.3 Adc)	$V_{CE(sat)}$*		—	1.0	Vdc
Base-Emitter On Voltage* (I_C = 3 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.6	Vdc
Current-Gain-Bandwidth Product (I_C =0.25Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		3.0	—	MHz

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



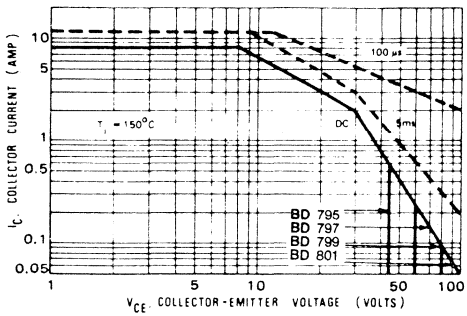
STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

3

FIGURE 1 – ACTIVE REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – COLLECTOR SATURATION REGION

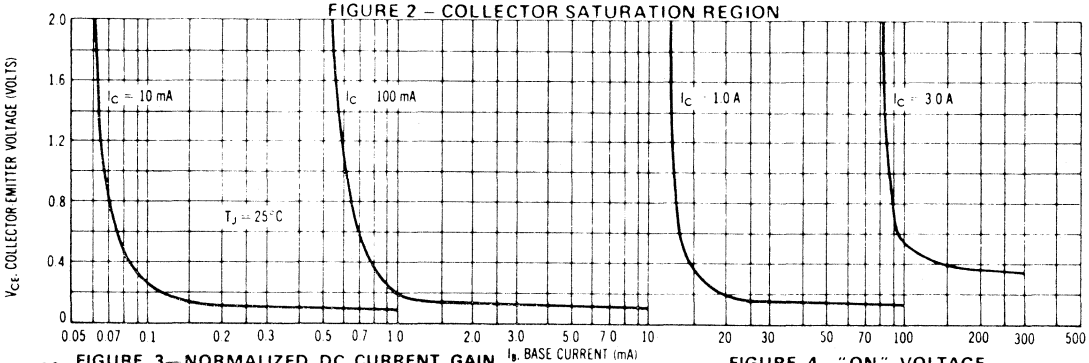


FIGURE 3– NORMALIZED DC CURRENT GAIN

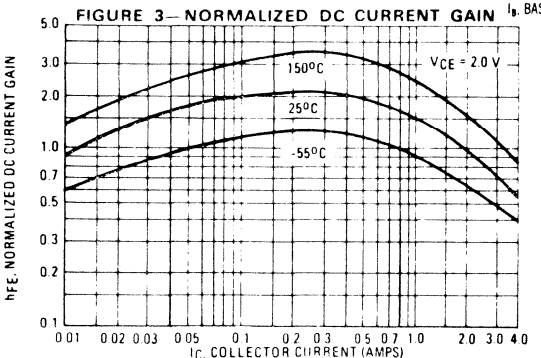


FIGURE 4 – "ON" VOLTAGE

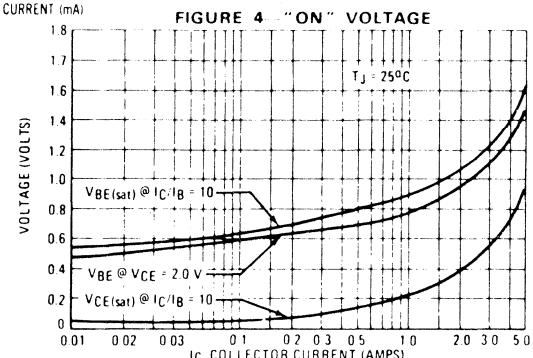
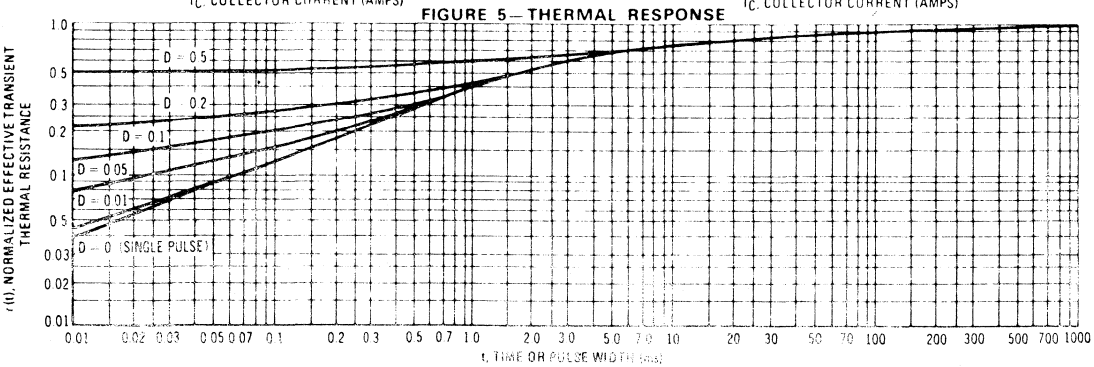


FIGURE 5– THERMAL RESPONSE



BD796 • BD798
BD800 • BD802

PLASTIC HIGH POWER
SILICON PNP TRANSISTOR

designed for use up to 30 Watt audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 1.0 Adc
- BD 796, 798, 800, 802 are complementary with BD 795, 797, 799, 801

8 AMPERE
POWER TRANSISTOR

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45, 60, 80, 100 VOLTS
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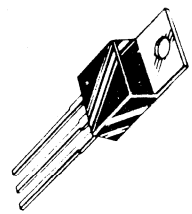


MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD796 BD798 BD800 BD802	45 60 80 100	Vdc
Collector-Base Voltage	V_{CBO}	BD796 BD798 BD800 BD802	45 60 80 100	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		8	Adc
Base Current	I_B		3	Adc
Total Device Dissipation T_C=25°C Derate avove 25°C	P_D		65 522	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		—55 to +150	°C

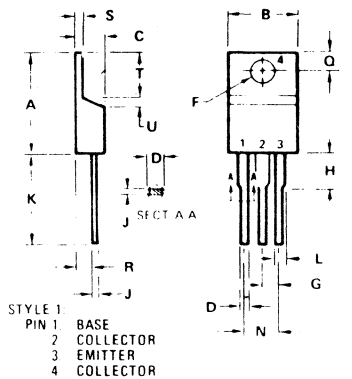
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		1.92	° C/W

ELECTRICAL CHARACTERISTICS (T_c = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0) (I_C = 0.05 Adc, I_B = 0)	BV_{CEO}*	BD796 BD798 BD800 BD802	45 60 80 100	— — — —	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	BD796 BD798 BD800 BD802	— — — —	0.1 0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 1 A, V_{CE} = 2 V) (I_C = 3 A, V_{CE} = 2 V)	h_{FE}*	BD 796/798 BD 800/802 BD 796/788 BD 800/802	40 30 25 15	— — — —	
Collector-Emitter Saturation Voltage* (I_C = 3 Adc, I_B = 0.3 Adc)	$V_{CE(sat)}$*		—	1.0	Vdc
Base-Emitter On Voltage* (I_C = 3 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.6	Vdc
Current-Gain-Bandwidth Product (I_C =0.25Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		3.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



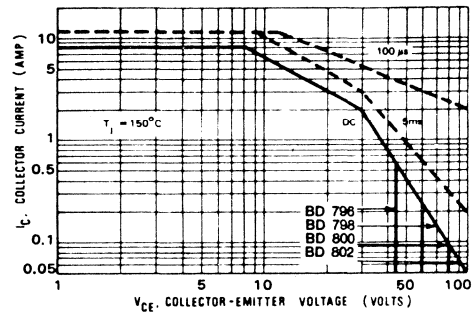
STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.036
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

3

FIGURE 1 – ACTIVE REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – COLLECTOR SATURATION REGION

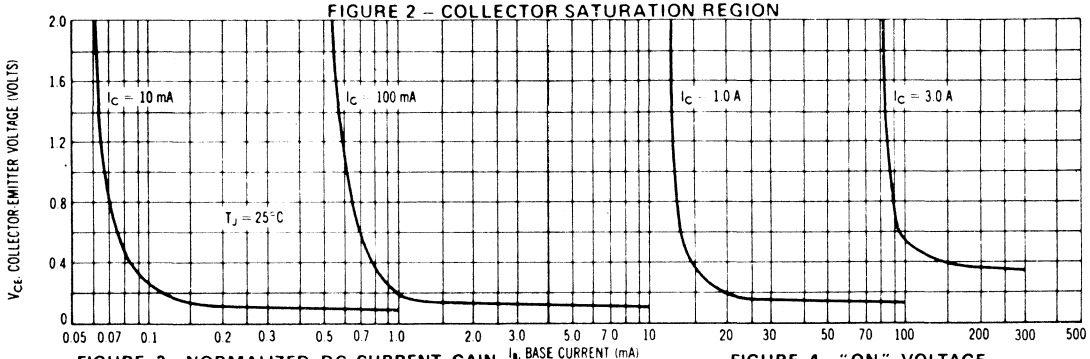


FIGURE 3 – NORMALIZED DC CURRENT GAIN

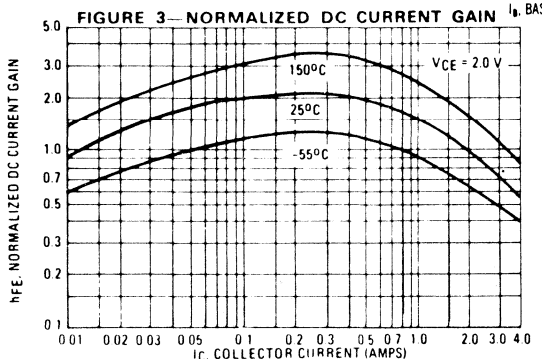


FIGURE 4 – "ON" VOLTAGE

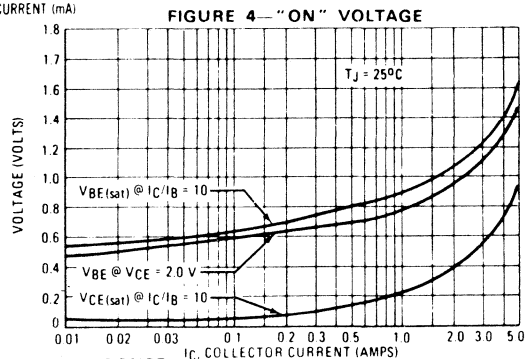
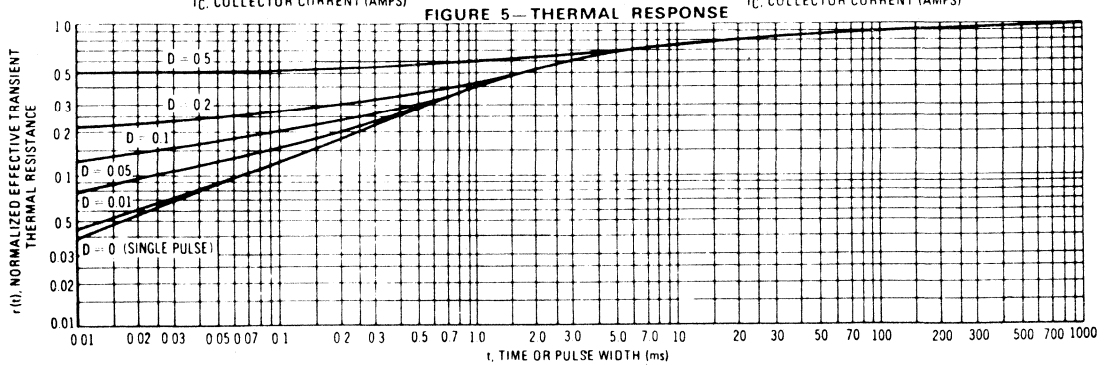


FIGURE 5 – THERMAL RESPONSE



BD805
BD807 • BD809

PLASTIC HIGH POWER
SILICON NPN TRANSISTOR

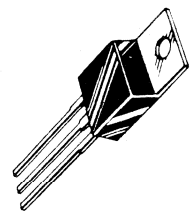
. . . designed for use in high power audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current—h_{FE} = 30 (Min) @ I_C = 2.0 Adc
- BD 805, 807, 809 are complementary with BD 806, 808, 810

10 AMPERE
POWER TRANSISTOR

NPN SILICON

45, 60, 80 VOLTS
90 WATTS



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD805 BD807 BD809	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD805 BD807 BD809	55 70 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		10.0	Adc
Base Current	I_B		6.0	Adc
Total Device Dissipation T_C=25°C Derate above 25°C	P_D		90 720	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−55 to +150	°C

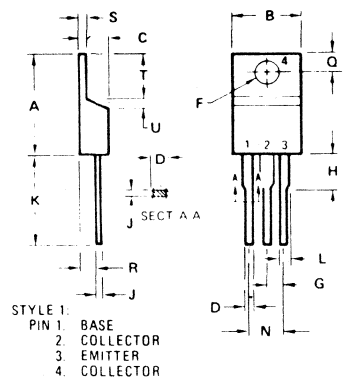
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		1.39	° C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.2 Adc, I_B = 0)	BV_{CEO}*	BD805 BD807 BD809	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 55 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	BD805 BD807 BD809	— — —	1.0 1.0 1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	2.0	mAdc
DC current Gain (I_C = 2A, V_{CE} = 2 V) (I_C = 4A, V_{CE} = 2 V)	h_{FE}*		30 15	— —	
Collector-Emitter Saturation Voltage* (I_C = 4 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$*		—	1.1	Vdc
Base-Emitter On Voltage* (I_C = 4 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.6	Vdc
Current-Gain-Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		1.5	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs Duty Cycle ≤ 2.0%



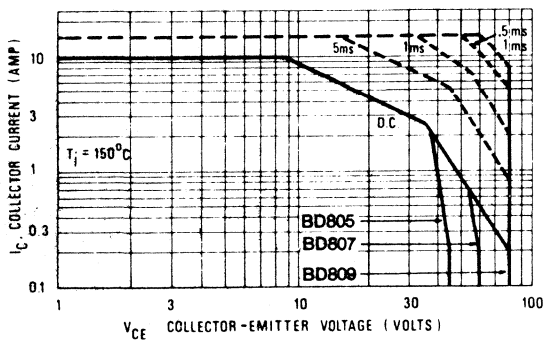
STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

3

FIGURE 1 – ACTIVE REGION DC SAFE OPERATING AREA



See Note 1

FIGURE 2 – POWER-TEMPERATURE DERATING CURVE

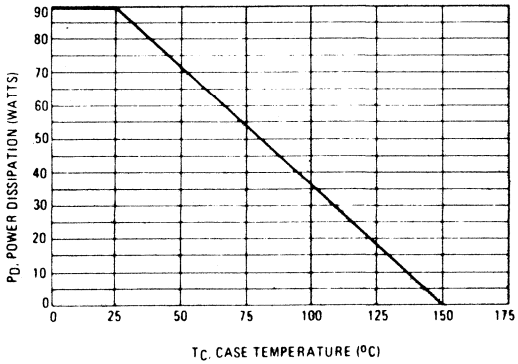


FIGURE 3 – "ON" VOLTAGES

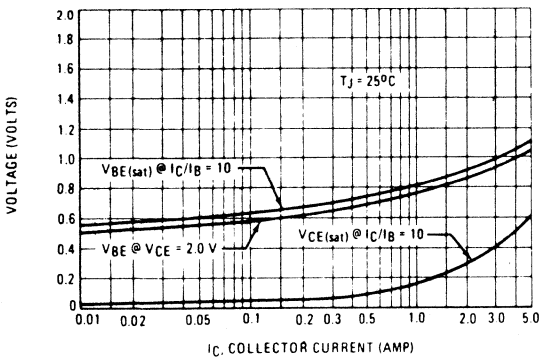


FIGURE 4 – CURRENT GAIN

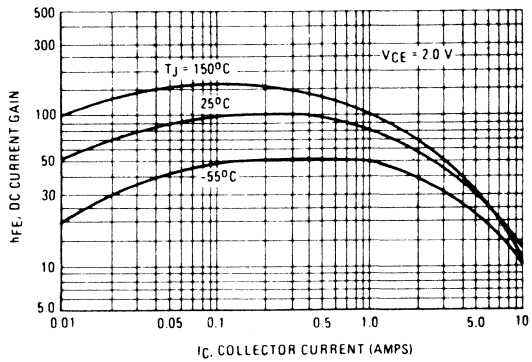
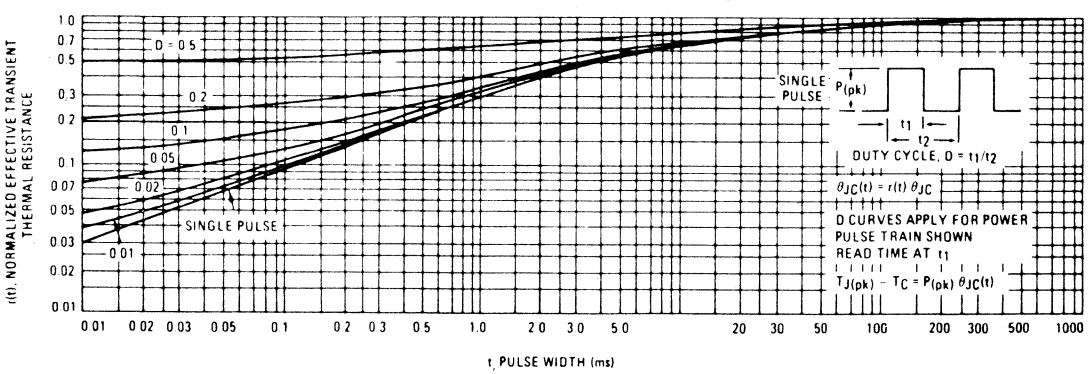


FIGURE 5 – THERMAL RESPONSE



Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ ≤150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

BD806
BD808 • BD810

PLASTIC HIGH POWER SILICON PNP TRANSISTOR

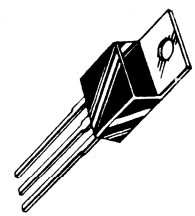
. . . designed for use in high power audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current—h_{FE} = 30 (Min) @ I_C = 2.0 Adc
- BD 806, 808, 810 are complementary with BD 805, 807, 809

10 AMPERE POWER TRANSISTOR

PNP SILICON

45, 60, 80 VOLTS 90 WATTS



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD806 BD808 BD810	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD806 BD808 BD810	55 70 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		10.0	Adc
Base Current	I_B		6.0	Adc
Total Device Dissipation T_C=25°C Derate above 25°C	P_D		90 720	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−55 to +150	°C

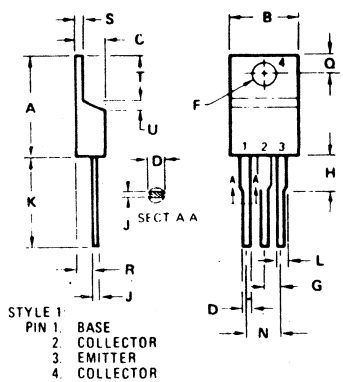
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		1.39	° C/W

ELECTRICAL CHARACTERISTICS (T_c = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.2 Adc, I_B = 0)	BV_{CEO}*	BD806 BD808 BD810	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 55 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	BD806 BD808 BD810	— — —	1.0 1.0 1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	2.0	mAdc
DC current Gain (I_C = 2A, V_{CE} = 2 V) (I_C = 4A, V_{CE} = 2 V)	h_{FE}*		30 15	— —	
Collector-Emitter Saturation Voltage* (I_C = 4 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$*		—	1.1	Vdc
Base-Emitter On Voltage* (I_C = 4 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.6	Vdc
Current-Gain-Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		1.5	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



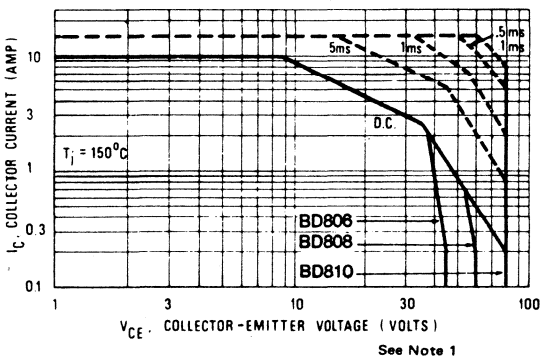
STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

3

FIGURE 1 – ACTIVE REGION DC SAFE OPERATING AREA



See Note 1

FIGURE 2 — POWER-TEMPERATURE DERATING CURVE

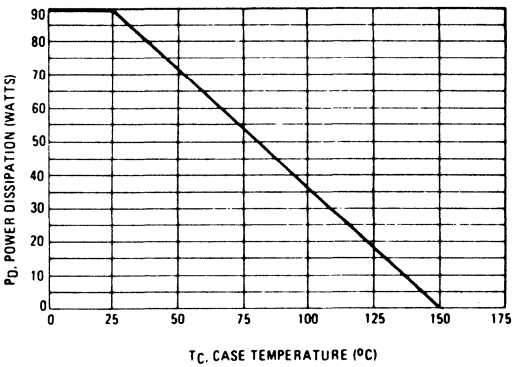


FIGURE 3 — "ON" VOLTAGES

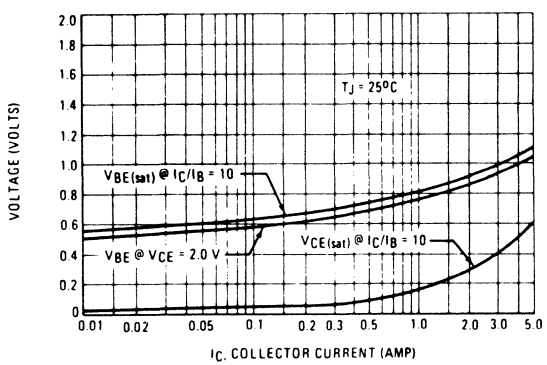


FIGURE 4 – CURRENT GAIN

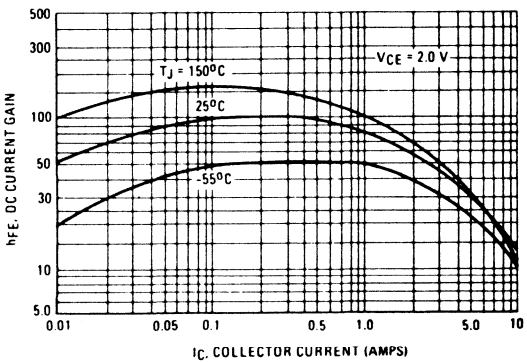
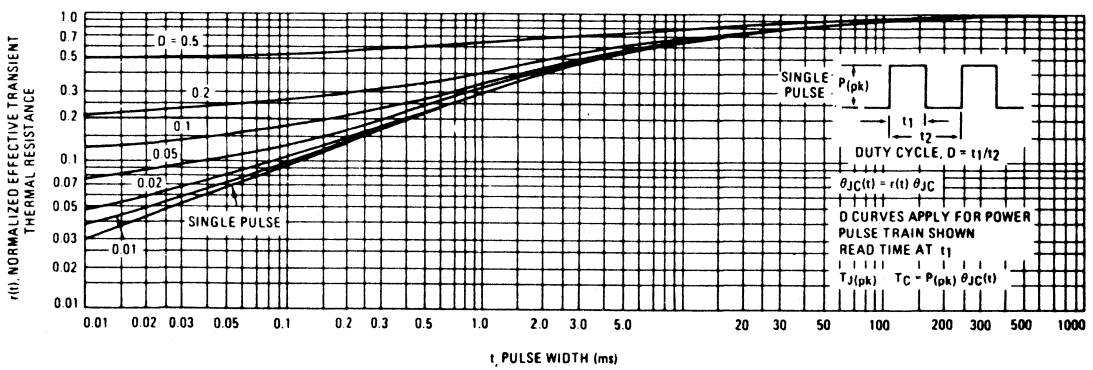


FIGURE 5 — THERMAL RESPONSE



Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

BD895, BD895A
BD897, BD897A
BD899, BD899A
BD901

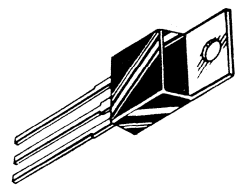
PLASTIC POWER SILICON NPN DARLINGTONS

. . . for use as output devices in complementary general-purpose amplifier applications.

- High DC Current Gain – h_{FE} = 750 (Min) @ I_C = 3.0 and 4.0 Adc
- Monolithic Construction
- BD895, 895A, 897, 897A, 899, 899A, 901 are complementary with BD896, 896A, 898, 898A, 900, 900A, 902.
- Electrical equivalents to BD695A, 697, 697A, 699, 699A, 701.

DARLINGTON 8 AMPERE NPN SILICON POWER TRANSISTORS

45-60-80-100 VOLTS
70 WATTS



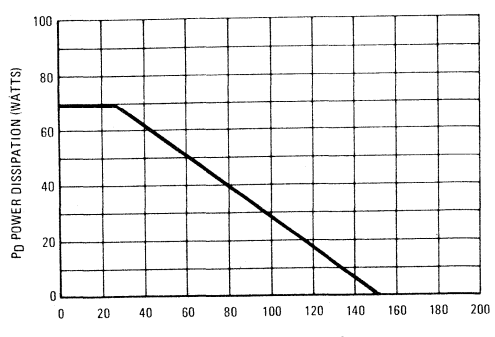
MAXIMUM RATINGS

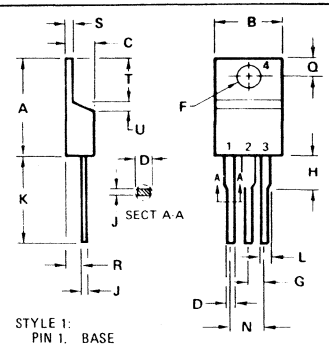
Rating	Symbol	BD895 BD895A	BD897 BD897A	BD899 BD899A	BD901	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current	I_C	8.0				Adc
Base Current	I_B	0.1				Adc
Total Device Dissipation @ T_C = 25 °C	P_D	70				Watts
Derate above 25 °C		0.56				W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.79	°C/W

FIGURE 1 – POWER TEMPERATURE DERATING CURVE





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

3

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic		Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage[1] (I_C = 100 mAdc, I_B = 0)	BD895, 895A	BV_{CEO}	45	–	Vdc
	BD897, 897A		60	–	
	BD899, 899A		80	–	
	BD901		100	–	
Collector Cutoff Current (V_{CE} = Half Rated V_{CEO}, I_B = 0)		I_{CEO}	–	500	μAdc
Collector Cutoff Current (V_{CB} = Rated BV_{CEO}, I_E = 0)		I_{CBO}	–	0.2	mAdc
(V_{CB} = Rated BV_{CEO}, I_E = 0, T_C = 100 °C)			–	2.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain[1]		h_{FE}			–
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)	BD895, 897, 899, 901		750	–	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	BD895A, 897A, 899A		750	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 12 mAdc)	BD895, 897, 899, 901		–	2.5	
(I_C = 4.0 Adc, I_B = 16 mAdc)	BD895A, 897A, 899A		–	2.8	
Base-Emitter On Voltage[1]		$V_{BE(on)}$			Vdc
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)	BD895, 897, 899, 901		–	2.5	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	BD895A, 897A, 899A		–	2.5	
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		h_{fe}	1.0	–	–

[1] Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown (see AN-415).

FIGURE 2 – DC SAFE OPERATING AREA

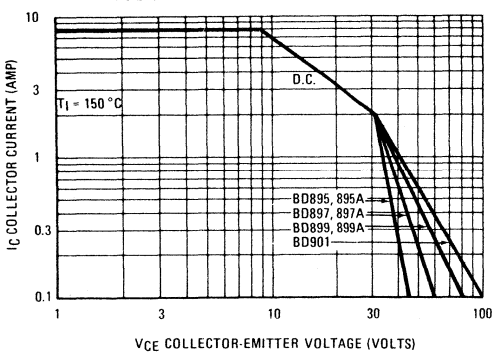
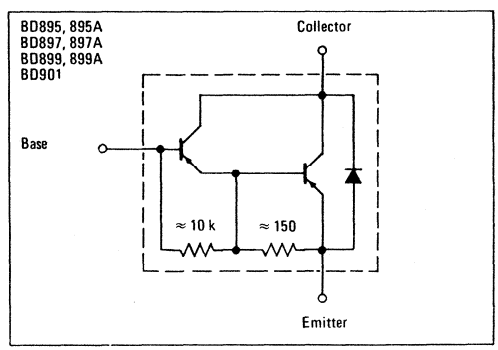


FIGURE 3 – DARLINGTON CIRCUIT SCHEMATIC



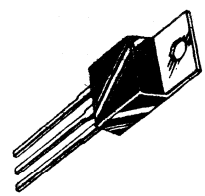
BD896, 896A • BD898, 898A
BD900, 900A • BD902

PLASTIC MEDIUM-POWER PNP TRANSISTORS

. . . for use as output devices in complementary general-purpose amplifier applications.

- High DC Current Gain – h_{FE} = 750 (Min) @ I_C = 3.0 and 4.0 Adc
- Monolithic Construction
- **BD896A, 898, 898A, 900, 900A, 902 are complementary with BD895A, 897, 897A, 899, 899A, 901**
- **Electrical equivalents to BD696A, 698, 698A, 700, 700A, 702**

DARLINGTON
8 AMPERE
SILICON
POWER TRANSISTORS
45-60-80-100 VOLTS
70 WATTS



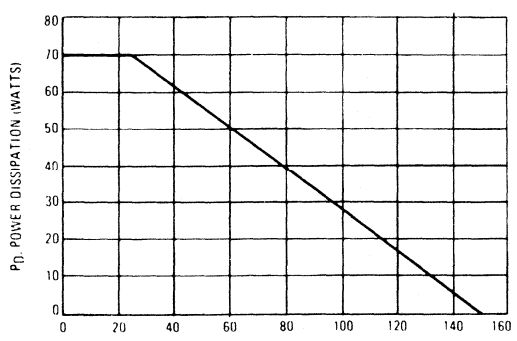
MAXIMUM RATINGS

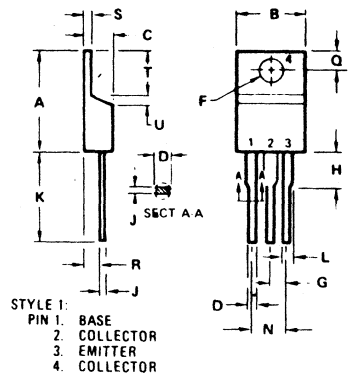
Rating	Symbol	BD696 BD696A	BD898 BD898A	BD900 BD900A	BD902	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current	I_C	8.0				Adc
Base Current	I_B	0.1				Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	70 0.56				Watts W/°C
Operating and Storage Junction Temperating Range	T_J, T_{stg}	-55 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.79	°C/W

FIGURE 1 – POWER TEMPERATURE DERATING CURVE





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

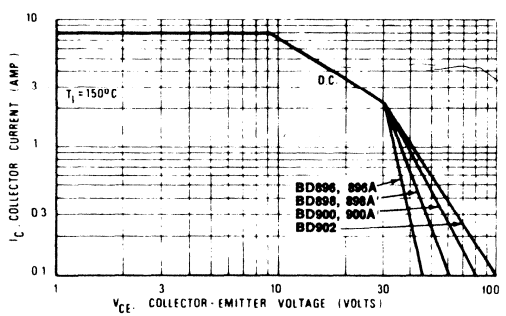
3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage[1] (I_C = 100 mAdc, I_B = 0)	BD896, 896A BD898, 898A BD900, 900A BD902	BV_{CEO}	45 60 80 100	– – – –	Vdc
Collector Cutoff Current (V_{CE} = Half Rated V_{CEO}, I_B = 0)		I_{CEO}	–	500	μAdc
Collector Cutoff Current (V_{CB} = Rated BV_{CEO}, I_E = 0) (V_{CB} = Rated BV_{CEO}, I_E = 0, T_C = 100°C)		I_{CBO}	– –	0.2 2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain[1] (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	BD896, 898, 900, 902 BD896A, 898A, 900A	h_{FE}	750 750	– –	–
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 12 mAdc) (I_C = 4.0 Adc, I_B = 16 mAdc)	BD896, 898, 900, 902 BD896A, 898A, 900A	$V_{CE(sat)}$	– –	2.5 2.8	Vdc
Base-Emitter On Voltage[1] (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	BD896, 898, 900, 902 BD896A, 898A, 900A	$V_{BE(on)}$	– –	2.5 2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		h_{fe}	1.0	–	–

[1]Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

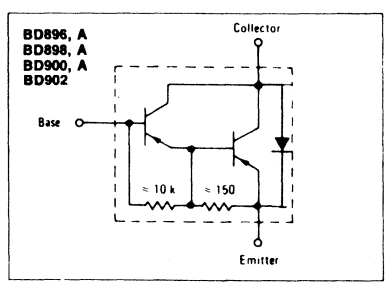
FIGURE 2 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown. (See AN-415)

FIGURE 3 – DARLINGTON CIRCUIT SCHEMATIC



NPN **PNP**

BDV 65 BDV 64
BDV 65A BDV 64A
BDV 65B BDV 64B

COMPLEMENTARY SILICON PLASTIC POWER DARLINGTONS

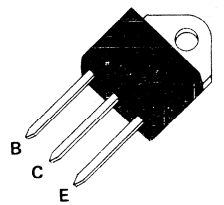
. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain
  HFE = 1000 (min.) @ 5 Adc
- Monolithic Construction with Built-in
  Base Emitter Shunt Resistors

DARLINGTONS
10 AMPERES

COMPLEMENTARY SILICON POWER TRANSISTORS

60-80-100 VOLTS
125 WATTS



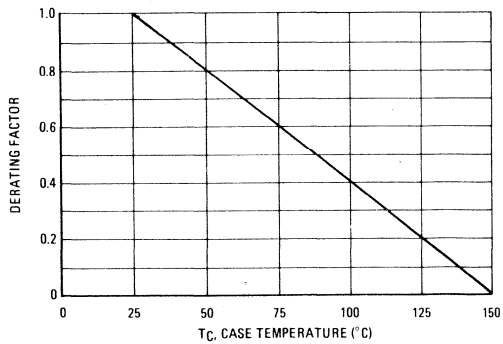
MAXIMUM RATINGS

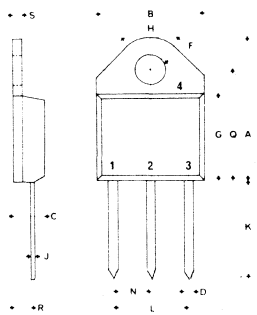
Rating	Symbol	BDV 65 BDV 64	BDV 65A BDV 64A	BDV 65B BDV 64B	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5			Vdc
Collector Current - Continuous - Peak	I_C	10 20			Adc
Base Current	I_B	0.5			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1	°C/W

FIGURE 1 – POWER DERATING





PIN 1 Base
PIN 2 Collector
PIN 3 Emitter
CASE (4) Collector

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.30	21.10	0.800	0.830
B	15.50	15.90	0.610	0.626
C	4.20	5.00	0.165	0.197
D	1.00	1.60	0.040	0.063
F	4.00	4.20	0.157	0.165
G	12.30	12.70	0.484	0.500
H	90 typ.		90 typ.	
J	0.45	0.70	0.018	0.028
K	12.7	15.5	0.500	0.610
L	10.65	11.15	0.420	0.440
N	5.20	5.70	0.205	0.225
Q	15.90	16.50	0.626	0.650
R	2.40	3.20	0.094	0.126
S	1.35	1.65	0.053	0.065

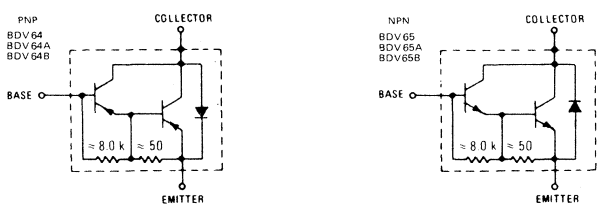
CASE 340

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

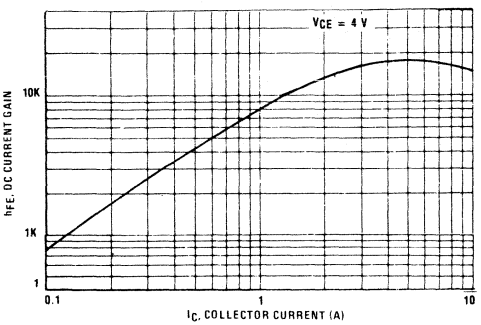
Characteristic		Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 30 mAdc, I_B = 0)	BDV65, BDV64		60	–	
	BDV65A, BDV64A		80	–	
	BDV65B, BDV64B		100	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	BDV65, BDV64		–	1	
(V_{CE} = 40 Vdc, I_B = 0)	BDV65A, BDV64A		–	1	
(V_{CE} = 50 Vdc, I_B = 0)	BDV65B, BDV64B		–	1	
Collector Cutoff Current		I_{CBO}			mA
(V_{CB} = 60 Vdc, I_E = 0)	BDV65, BDV64		–	0.4	
(V_{CB} = 80 Vdc, I_E = 0)	BDV65A, BDV64A		–	0.4	
(V_{CB} = 100 Vdc, I_E = 0)	BDV65B, BDV64B		–	0.4	
Collector Cutoff Current		I_{CBO}			mA
(V_{CB} = 30 Vdc, I_E = 0, T_C = 150°C)	BDV65, BDV64		–	2	
(V_{CB} = 40 Vdc, I_E = 0, T_C = 150°C)	BDV65A, BDV64A		–	2	
(V_{CB} = 50 Vdc, I_E = 0, T_C = 150°C)	BDV65B, BDV64B		–	2	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 5 Vdc, I_C = 0)				5	
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 5 Adc, V_{CE} = 4 Vdc)			1000	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 5 Adc, I_B = 0.02 Adc)			–	2	
Base-Emitter Saturation Voltage		$V_{BE(on)}$			Vdc
(I_C = 5 Adc, I_B = V_{CE} = 4 Vdc)			–	2.5	

FIGURE 1 – DARLINGTON CIRCUIT SCHEMATIC



NPN

FIGURE 2 – DC CURRENT GAIN



PNP

FIGURE 3 – DC CURRENT GAIN

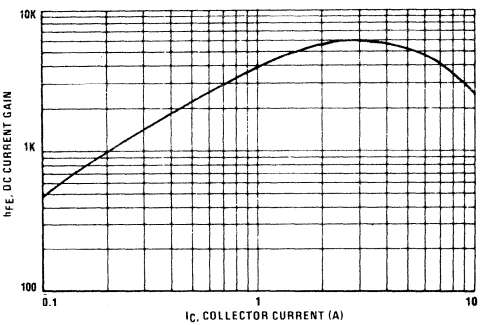


FIGURE 4 – "ON" VOLTAGES

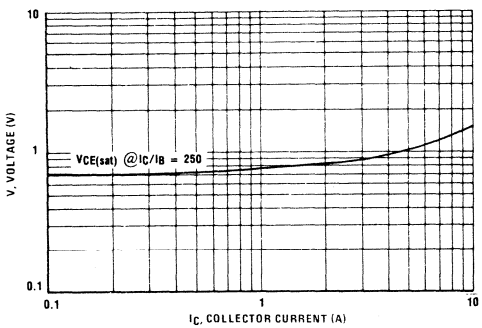


FIGURE 5 – "ON" VOLTAGES

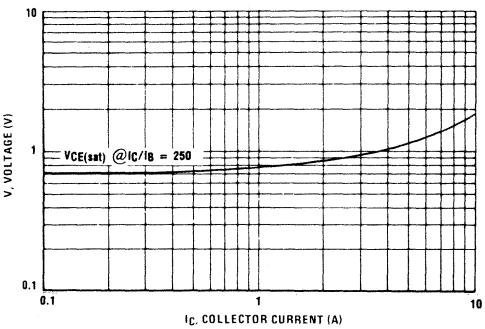
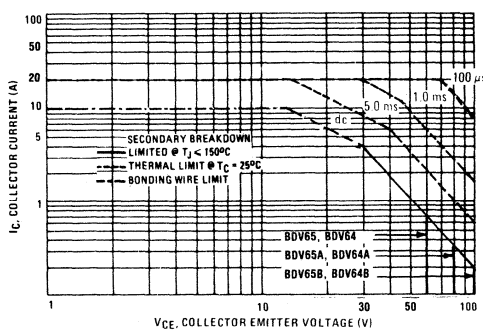


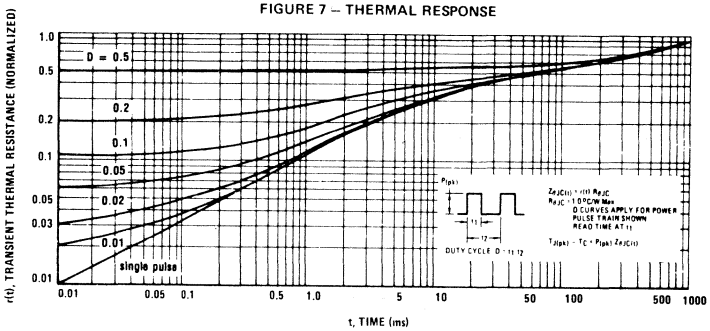
FIGURE 6 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 6 is based on $T_{J(pk)}$ 150°C, T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in figure 7. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN 415A)

FIGURE 7 – THERMAL RESPONSE



NPN PNP

BDW39 BDW44
BDW40 BDW45
BDW41 BDW46
BDW42 BDW47

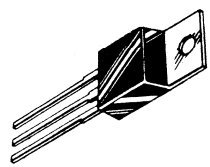
DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general purpose and low speed switching applications.

- High DC Current Gain – h_{FE} = 2500 (typ.) @ I_C = 5.0 Adc.
- Collector Emitter Sustaining Voltage @ 30 mAdc:
  $V_{CEO(sus)}$ = 45 Vdc (min.) – BDW39/BDW44
  60 Vdc (min.) – BDW40/BDW45
  80 Vdc (min.) – BDW41/BDW46
  100 Vdc (min.) – BDW42/BDW47
- Low Collector Emitter Saturation Voltage:
  $V_{CE(sat)}$ = 2.0 Vdc (max.) @ I_C = 5.0 Adc
  3.0 Vdc (max.) @ I_C = 10.0 Adc
- Monolithic Construction with Built-In Base Emitter Shunt resistors
- TO-220AB Compact Package
- TO-66 Lead form also available ordered with "-66" suffix.

DARLINGTON 15 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS 45-60-80-100 VOLTS 85 WATTS



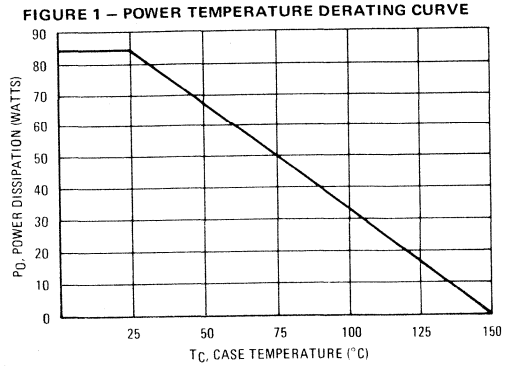
MAXIMUM RATINGS

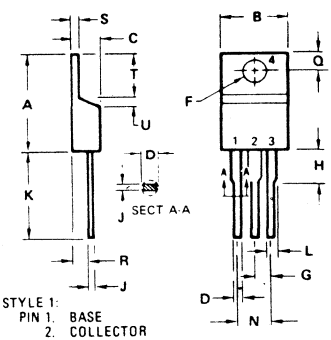
Rating	Symbol	BDW39 BDW44	BDW40 BDW45	BDW41 BDW46	BDW42 BDW47	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current - Continuous	I_C	15				Adc
Base Current	I_B	0.5				Adc
Total Device Dissipation @ T_C = 25 °C Derate above 25 °C	P_D	85 0.68				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.47	°C/W

FIGURE 1 – POWER TEMPERATURE DERATING CURVE





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

3

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic		Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage[1]		$V_{CEO(sus)}$			Vdc
(I_C = 30 mAdc, I_B 0)	BDW39/BDW44		45		
	BDW40/BDW45		60		
	BDW41/BDW46		80		
	BDW42/BDW47		100		
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 22.5 Vdc, I_B = 0)	BDW39/BDW44			2	
(V_{CE} = 30 Vdc, I_B = 0)	BDW40/BDW45			2	
(V_{CE} = 40 Vdc, I_B = 0)	BDW41/BDW46			2	
(V_{CE} = 50 Vdc, I_B = 0)	BDW42/BDW47			2	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 45 Vdc, I_E = 0)	BDW39/BDW44			1	
(V_{CB} = 60 Vdc, I_E = 0)	BDW40/BDW45			1	
(V_{CB} = 80 Vdc, I_E = 0)	BDW41/BDW46			1	
(V_{CB} = 100 Vdc, I_E = 0)	BDW42/BDW47			1	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)				2	
ON CHARACTERISTICS[1]					
DC Current Gain		h_{FE}			–
(I_C = 5 Adc, V_{CE} = 4.0 Vdc)			1000		
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)			250		
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 5 Adc, I_B = 10 mAdc)				2	
(I_C = 10 Adc, I_B = 50 mAdc)				3	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 10 Adc, V_{CE} = 4 Vdc)				3	
SECOND BREAKDOWN[2]					
Second Breakdown Collector-Current With Base Forward Biased		$I_{S/b}$			Adc
BDW39/BDW40/BDW41/BDW42	V_{CE} = 28.4 Vdc		3		
	V_{CE} = 40 Vdc		1.2		
BDW44/BDW45/BDW46/BDW47	V_{CE} = 22.5 Vdc		3.8		
	V_{CE} = 36 Vdc		1.2		
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product[3]		f_T			MHz
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)			4.0		
Output Capacitance		C_{ob}			pF
V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	BDW39/40/41/42			200	
	BDW44/45/46/47			300	
Small Signal Current Gain		h_{fe}			–
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 KHz)			300		

[1] Pulse test: Pulse width = 300 μs, Duty cycle = 2.0%.
[2] Pulse test non repetitive pulse width: 250 ms.
[3] $f_T = |h_{fe}| \cdot f$ test.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

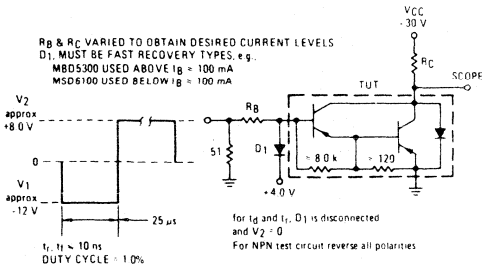


FIGURE 3 – SWITCHING TIMES

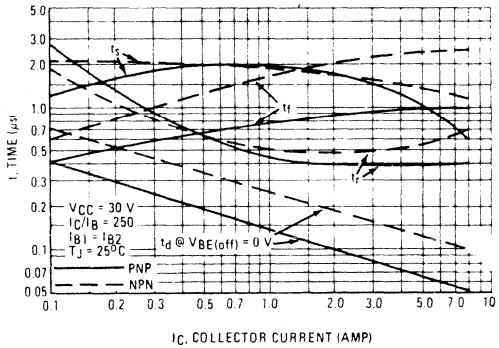
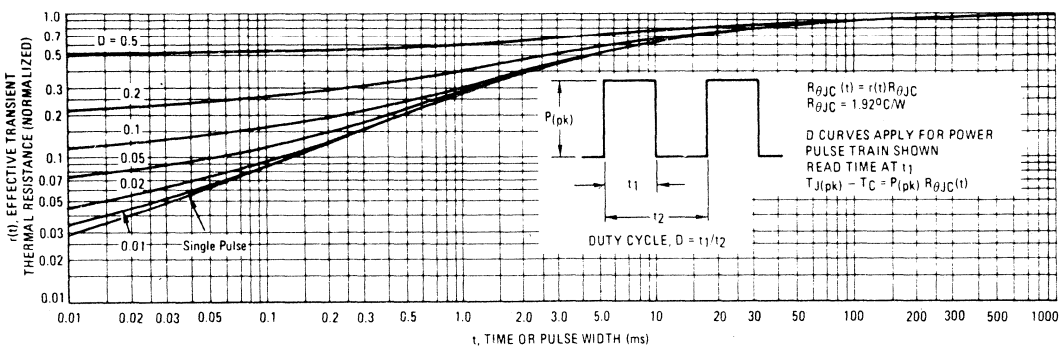


FIGURE 4 – THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 5 – BDW39 THRU BDW42

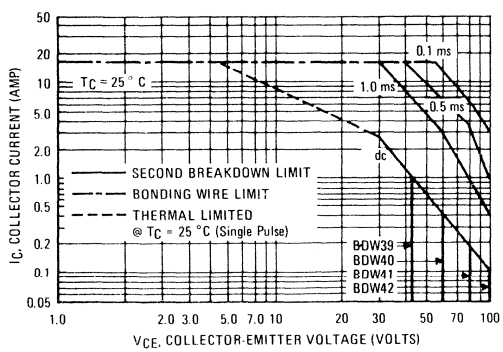
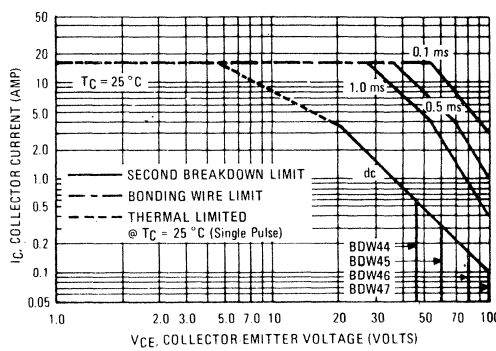


FIGURE 6 – BDW44 THRU GDW47



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Fig. 5 and 6 is based on $T_{J(pk)}$ = 200 °C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200$ °C. $T_{J(pk)}$ may be calculated from the data in Fig. 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See an-415).

FIGURE 7 – SMALL-SIGNAL CURRENT GAIN

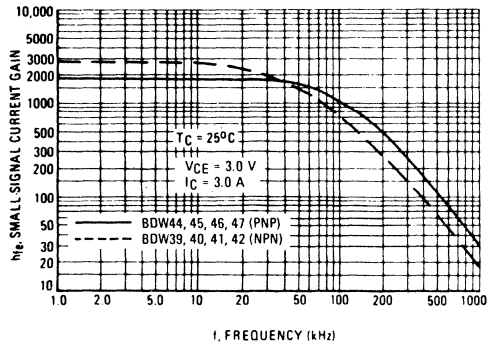
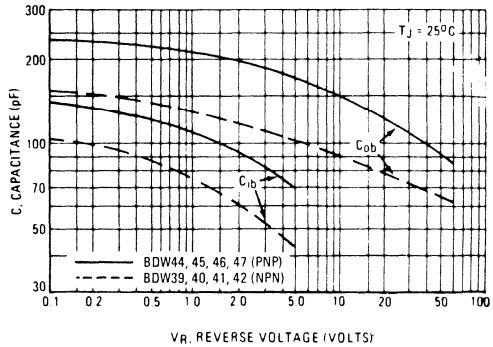


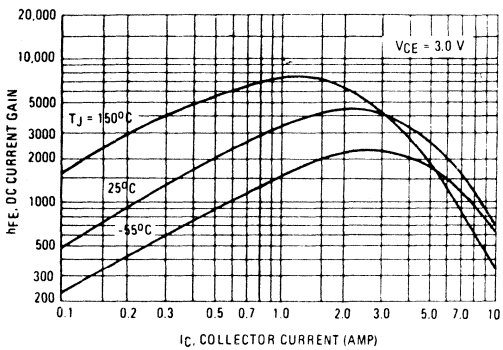
FIGURE 8 – CAPACITANCE



BDW39, 40, 41, 42 (NPN)

BDW44, 45, 46, 47 (PNP)

FIGURE 9 – DC CURRENT GAIN



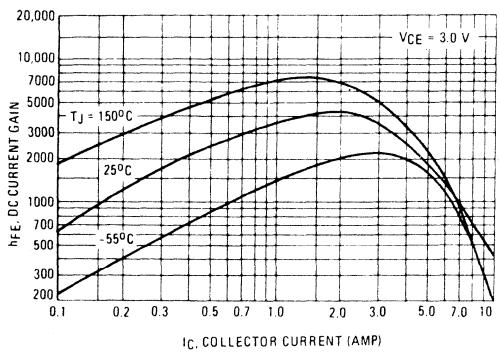
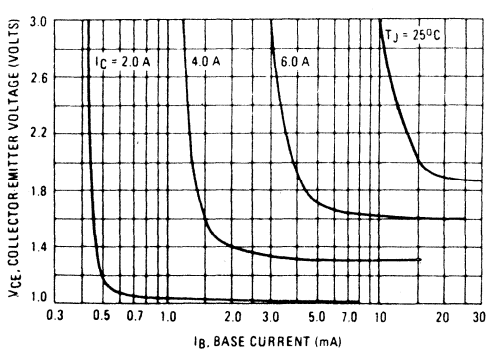
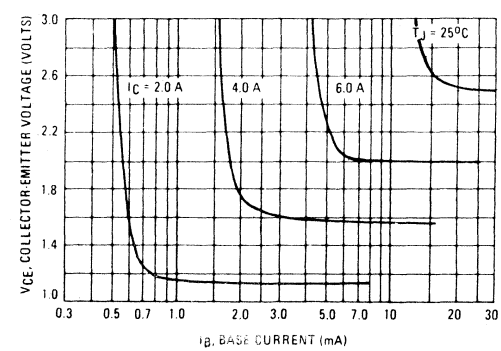


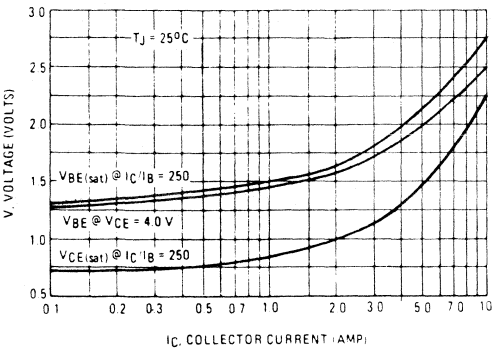
FIGURE 10 – COLLECTOR SATURATION REGION





BDW39, 40, 41, 42 (NPN) **BDW44, 45, 46, 47 (PNP)**

FIGURE 11 – "ON" VOLTAGES



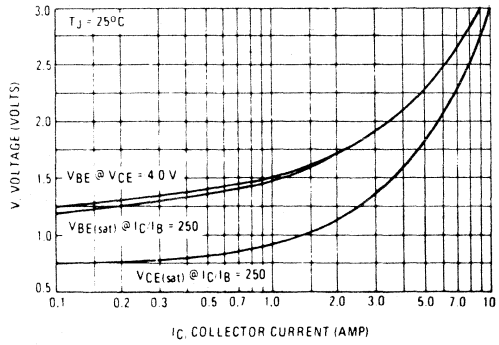
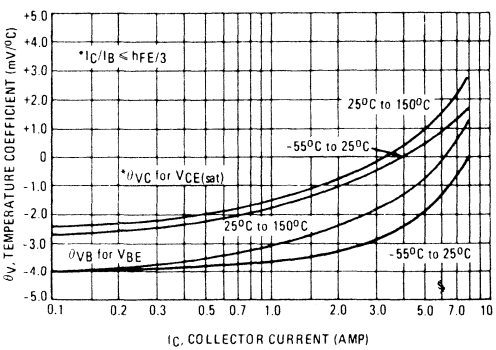


FIGURE 12 – TEMPERATURE COEFFICIENTS



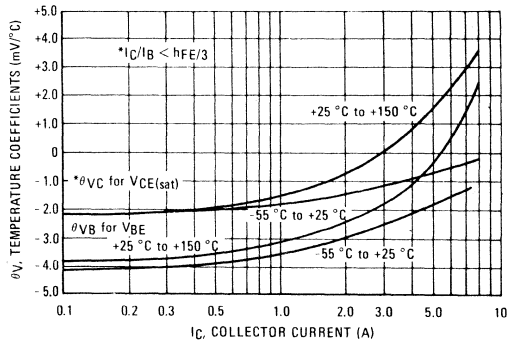
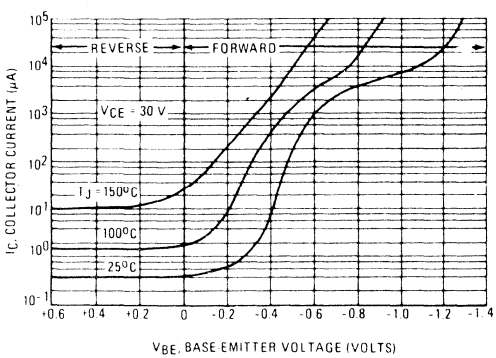
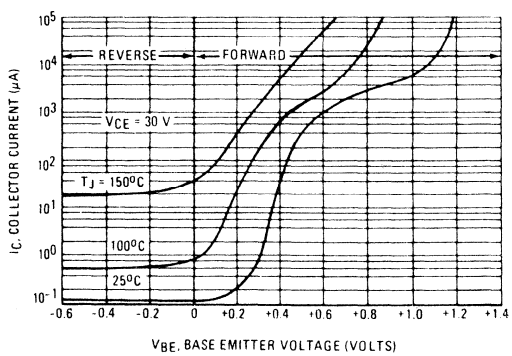


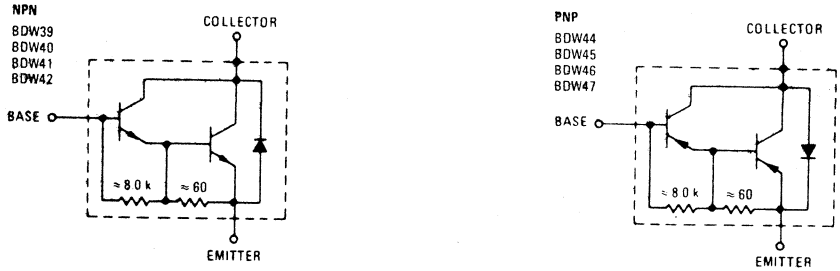
FIGURE 13 – COLLECTOR CUT-OFF REGION





3

FIGURE 14 – DARLINGTON SCHEMATIC



NPN PNP

BDX33 BDX34
BDX33A BDX34A
BDX33B BDX34B
BDX33C BDX34C

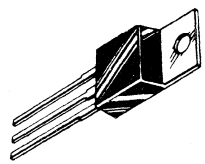
DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general purpose and low speed switching applications.

- High DC Current Gain – h_{FE} = 2500 (typ.) at I_C = 4.0 Adc
- Collector Emitter sustaining Voltage at 100 mAdc
  $V_{CEO(sus)}$ – 45 Vdc (min.) – BDX33, 34
  60 Vdc (min.) – BDX33A, 34A
  80 Vdc (min.) – BDX33B, 34B
  100 Vdc (min.) – BDX33C, 34C
- Low Collector Emitter Saturation Voltage
  $V_{CE(sat)}$ = 2.5 Vdc (max.) at I_C = 4.0 Adc – BDX33, 33A/34, 34A
  2.5 Vdc (max.) at I_C = 3.0 Adc – BDX33B, 33C/34B, 34C
- Monolithic Construction with Built-In Base Emitter Shunt resistors
- TO-220AB Compact Package
- TO-66 Lead form also available ordered with "-66" suffix.

DARLINGTON 10 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS
45-60-80-100 VOLTS
70 Watts



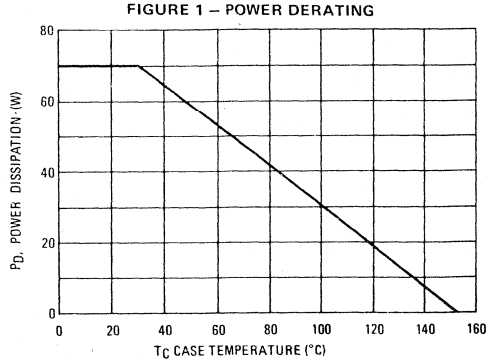
MAXIMUM RATINGS

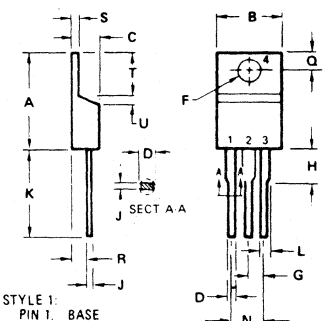
Rating	Symbol	BDX33 BDX34	BDX33A BDX34A	BDX33B BDX34B	BDX33C BDX34C	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current - Continuous Peak	I_C	10 15				Adc
Base Current	I_B	0.25				Adc
Total Device Dissipation @ T_C = 25 °C Derate above 25 °C	P_D	70 0.56				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.78	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

3

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic		Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage[1] (I_C = 100 mAdc, I_B = 0)	BDX33/BDX34	$V_{CEO(sus)}$	45		Vdc
	BDX33A/BDX34A		60		
	BDX33B/BDX34B		80		
	BDX33C/BDX34C		100		
Collector-Emitter Sustaining Voltage[1] (I_C = 100 mAdc, I_B = 0, R_{BE} = 100)	BDX33/BDX34	$V_{CER(sus)}$	45		Vdc
	BDX33A/BDX34A		60		
	BDX33B/BDX34B		80		
	BDX33C/BDX34C		100		
Collector-Emitter Sustaining Voltage[1] (I_C = 100 mAdc, I_B = 0, V_{BE} = 1.5 Vdc)	BDX33/BDX34	$V_{CEX(sus)}$	45		Vdc
	BDX33A/BDX34A		60		
	BDX33B/BDX34B		80		
	BDX33C/BDX34C		100		
Collector Cutoff Current (V_{CE} = ½ rated V_{CEO}, I_B = 0)	T_C = 25 °C	I_{CEO}		0.5	mAdc
	T_C = 100 °C			10	
Collector Cutoff Current (V_{CB} = rated V_{CBO}, I_E = 0)	T_C = 25 °C	I_{CBO}		1	mAdc
	T_C = 100 °C			5	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}		10	mAdc
ON CHARACTERISTICS					
DC Current Gain[1] (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	BDX33, 33A/34, 34A	h_{FE}	750		–
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)	BDX33B, 33C/34B, 34C		750		
Collector-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 8 mAdc)	BDX33, 33A/34, 34A	$V_{CE(sat)}$		2.5	Vdc
(I_C = 3.0 Adc, I_B = 6 mAdc)	BDX33B, 33C/34B, 34C			2.5	
Base-Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 3 V)	BDX33, 33A/34, 34A	$V_{BE(on)}$		2.5	Vdc
(I_C = 3.0 Adc, V_{CE} = 3 Vdc)	BDX33B, 33C/34B, 34C			2.5	
Diode Forward Voltage (I_C = 8 Adc)		V_F		4	Vdc
SECOND BREAKDOWN[2]					
Second Breakdown Collector Current With Base Forward Biased (V_{CE} = 25 Vdc)	BDX33 Series	$I_{S/b}$	2.8		Adc
(V_{CE} = 20 Vdc)	BDX34 Series		3.5		
(V_{CE} = 36 Vdc)	BDX33 Series		1.0		
(V_{CE} = 33 Vdc)	BDX34 Series		1.0		
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (T_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f = 1 MHz)		h_{FE}	1000		–
Current Gain-Bandwidth product (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f = 1.0 MHz)		f_T	3		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	BDX33 Series	C_{ob}		200	pF
	BDX34 Series			300	

[1] Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%
[2] Pulse Test non repetitive: Pulse Width = 0.25 s.

FIGURE 2 – THERMAL RESPONSE

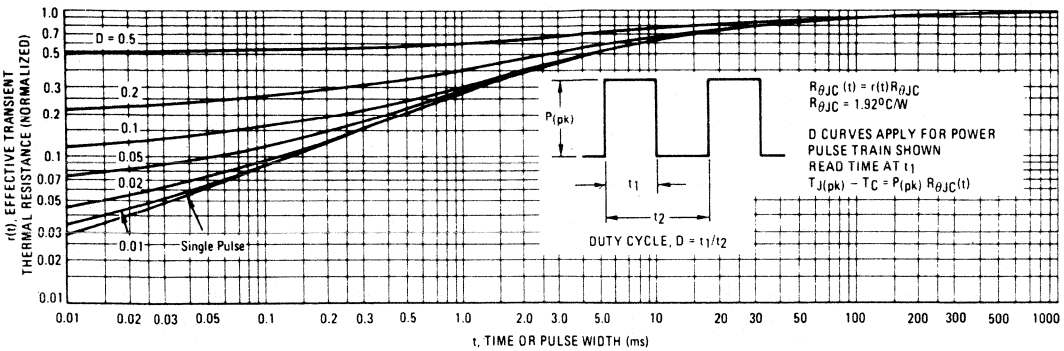
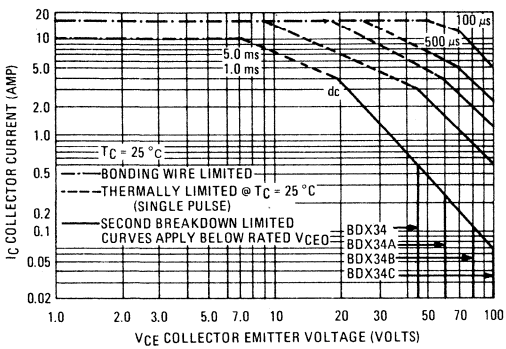
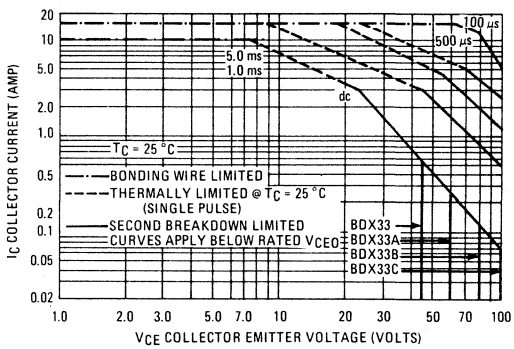


FIGURE 3 – ACTIVE-REGION SAFE OPERATING AREA





There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Fig. 3 is based on $T_{J(pk)} = 150\,^{\circ}C$;

T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ 150 °C $T_{J(pk)}$ may be calculated from the data in Fig. . At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown (see AN-415A).

FIGURE 4 – SMALL-SIGNAL CURRENT GAIN

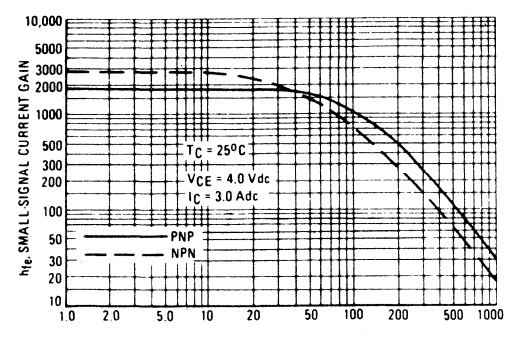
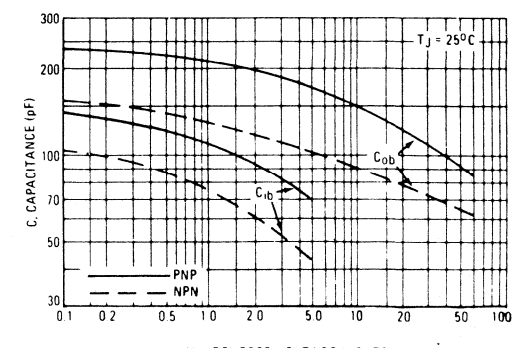


FIGURE 5 – CAPACITANCE

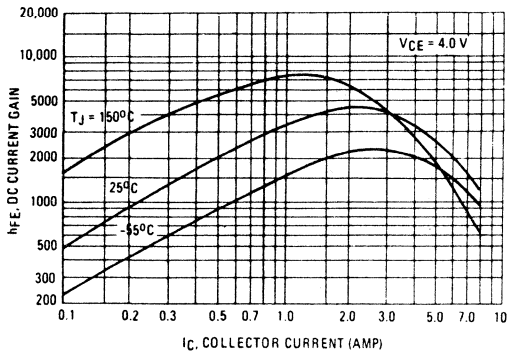


3

NPN
BDX33, 33A, 33B, 33C

PNP
BDX34, 34A, 34B, 34C

FIGURE 6 – DC CURRENT GAIN



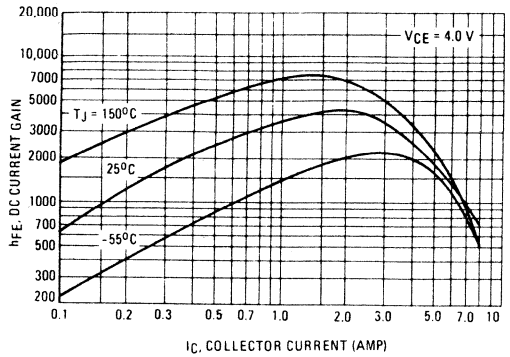
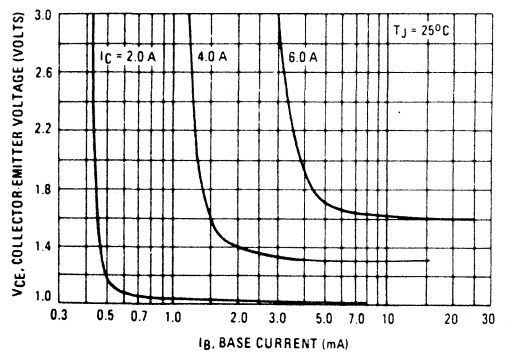


FIGURE 7 – COLLECTOR SATURATION REGION



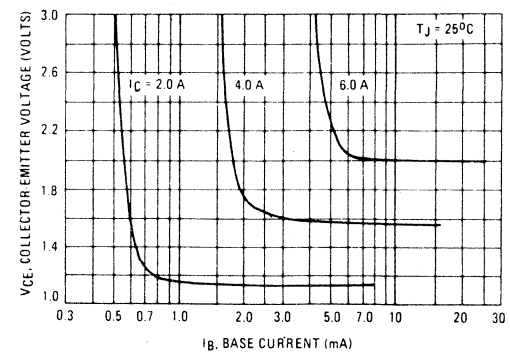
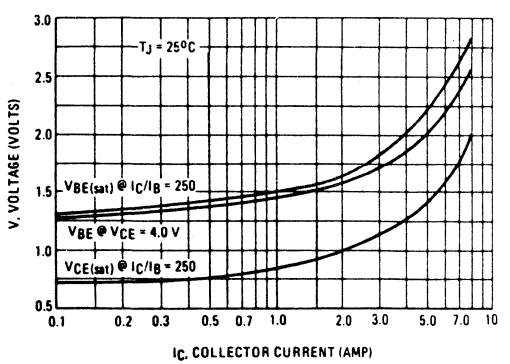
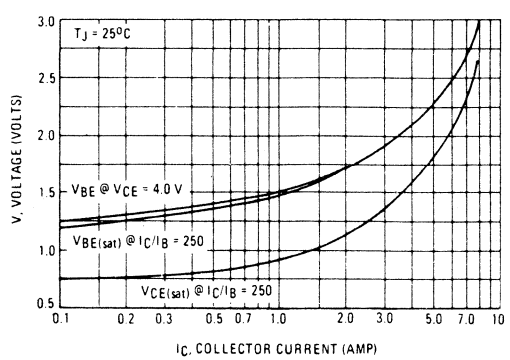


FIGURE 8 – "ON" VOLTAGES





BDX53, 53A, 53B, 53C (NPN)
BDX54, 54A, 54B, 54C (PNP)

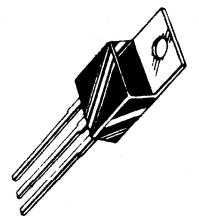
PLASTIC MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain –
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage – @ 100 mAdc
  $V_{CEO(sus)}$ = 45 Vdc (Min) — BDX53, 54
  = 60 Vdc (Min) — BDX53A, 54A
  = 80 Vdc (Min) — BDX53B, 54B
  = 100 Vdc (Min) — BDX53C, 54C
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc
  = 4.0 Vdc (Max) @ I_C = 5.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package

DARLINGTON 8 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

60-80-100 VOLTS
65 WATTS



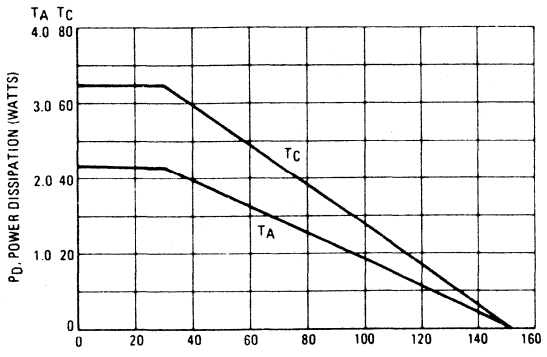
***MAXIMUM RATINGS**

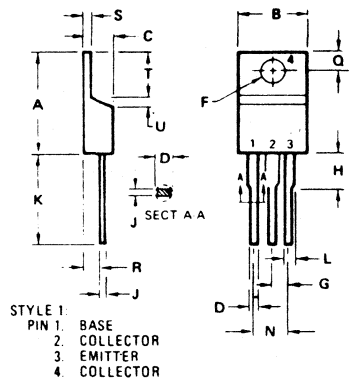
Rating	Symbol	BDX53 BDX54	BDX53A BDX54A	BDX53B BDX54B	BDX53C BDX54C	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current — Continuous	I_C	8				Adc
Peak		12				
Base Current	I_B	0.2				Adc
Total Device Dissipation @ T_C = 25°C	P_D	60				Watts
Derate above 25°C		0.48				W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150				°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.08	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	BDX53, BDX54	$V_{CEO(sus)}$	45		Vdc
	BDX53A, BDX54A		60	–	
	BDX53B, BDX54B		80	–	
	BDX53C, BDX54C		100	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 22 Vdc, I_B = 0)	BDX53, BDX54			0.5	
(V_{CE} = 30 Vdc, I_B = 0)	BDX53A, BDX54A		–	0.5	
(V_{CE} = 40 Vdc, I_B = 0)	BDX53B, BDX54B		–	0.5	
(V_{CE} = 50 Vdc, I_B = 0)	BDX53C, BDX54C		–	0.5	
Collector Cutoff Current		I_{CBO}		0.2	mAdc
(V_{CB} = 45 Vdc, I_E = 0)	BDX53, BDX54		–	0.2	
(V_{CB} = 60 Vdc, I_E = 0)	BDX53A, BDX54A		–	0.2	
(V_{CB} = 80 Vdc, I_E = 0)	BDX53B, BDX54B		–	0.2	
(V_{CB} = 100 Vdc, I_E = 0)	BDX53C, BDX54C		–	0.2	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)			750	–	
				–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 12 mAdc)			–	2.0	
			–	4.0	
Base-Emitter Saturation Voltage (I_C = 3.0 Adc, I_C = 12 mA)		$V_{BE(sat)}$	–	2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	–	–
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	BDX53, 53A, 53B, 53C		–	300	
	BDX54, 54A, 54B, 54C		–	200	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

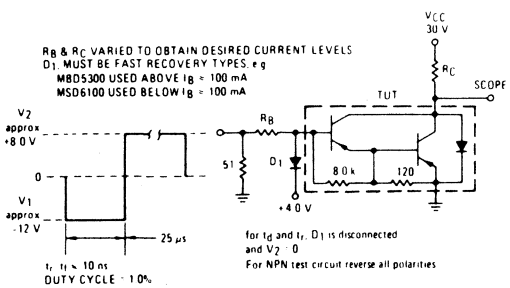


FIGURE 3 – SWITCHING TIMES

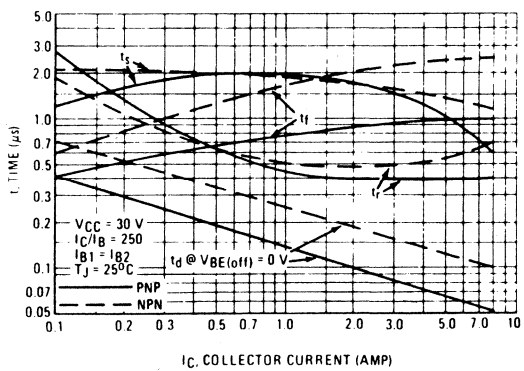


FIGURE 4 – THERMAL RESPONSE

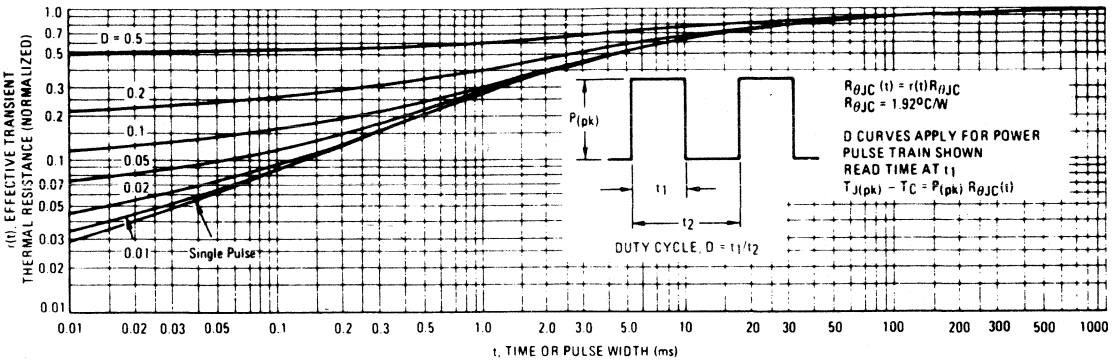
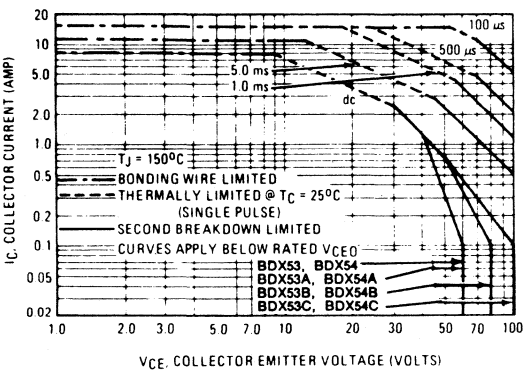


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown (see AN-415A).

FIGURE 6 – SMALL-SIGNAL CURRENT GAIN

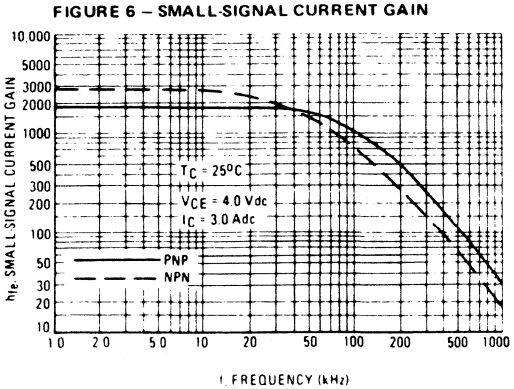
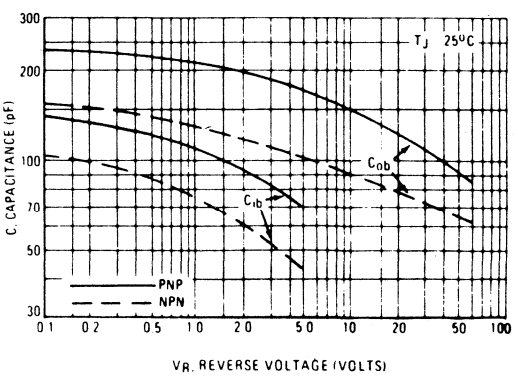


FIGURE 7 – CAPACITANCE



3

NPN

BDX53, BDX53A, BDX53B, BDX53C

PNP

BDX54, BDX54A, BDX54B, BDX54C

FIGURE 8 – DC CURRENT GAIN

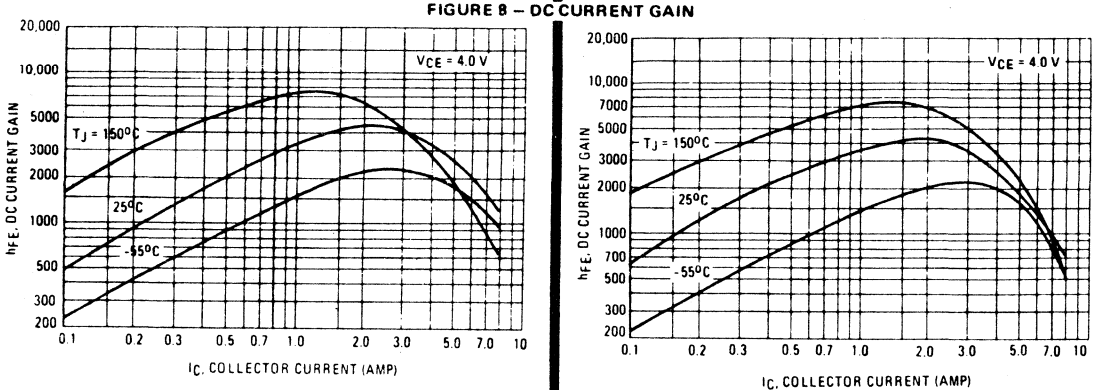


FIGURE 9 – COLLECTOR SATURATION REGION

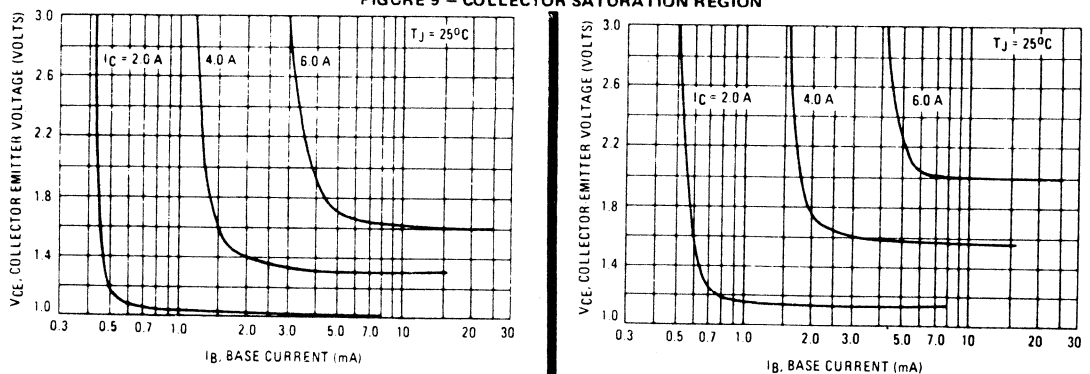
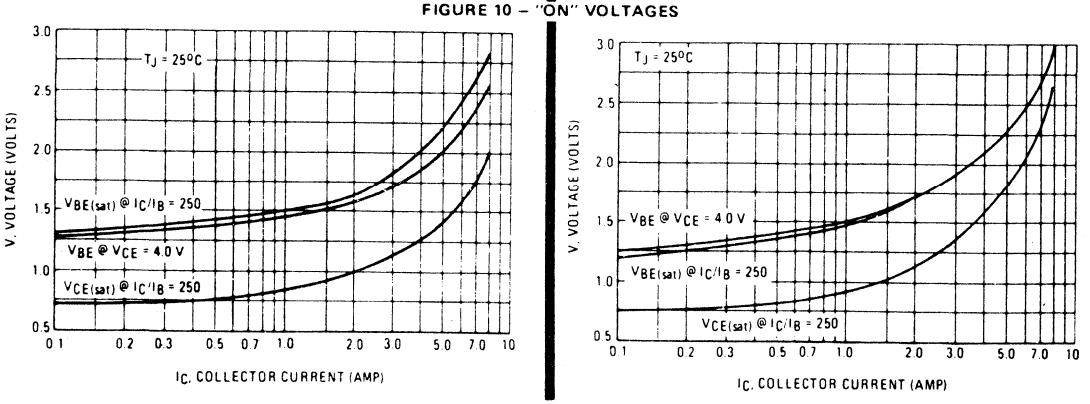


FIGURE 10 – "ON" VOLTAGES



NPN

BDX53, BDX53A, BDX53B, BDX53C

PNP

BDX54, BDX54A, BDX54B, BDX54C

FIGURE 11 – TEMPERATURE COEFFICIENTS

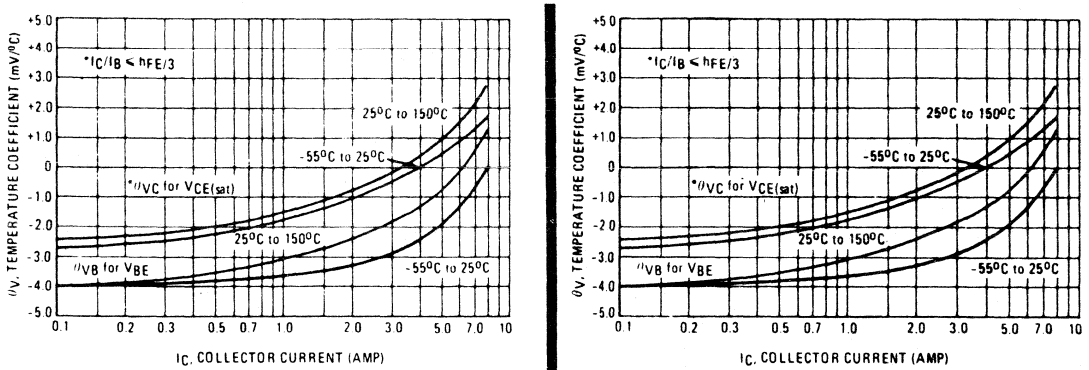


FIGURE 12 – COLLECTOR CUT-OFF REGION

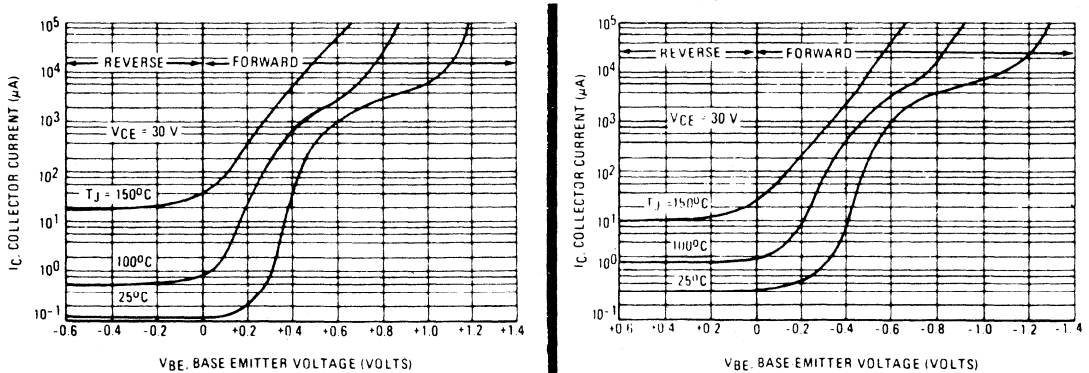
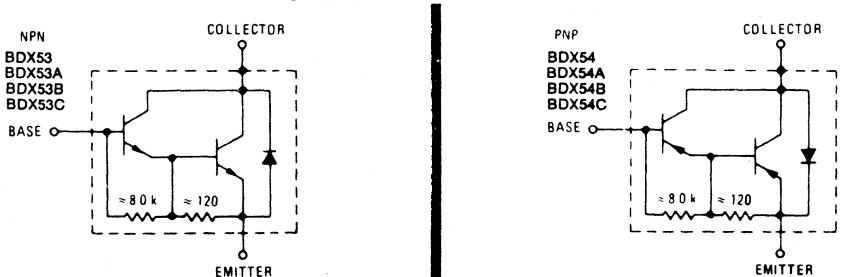


FIGURE 13 – DARLINGTON SCHEMATIC



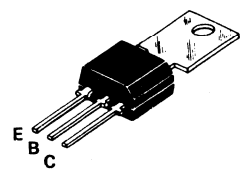
BF466
BF467
BF468

NPN SILICON ANNULAR ♦
HIGH VOLTAGE AMPLIFER TRANSISTORS

. . . designed for horizontal driver applications in television receivers.

- High Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 250 Vdc (min) @ I_C = 1.0 mAdc — BF468
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.5 Vdc (max) @ I_C = 200 mAdc
- Duowatt Package —
  2 Watts Free Air Dissipation @ T_A = 25 °C

NPN SILICON
AMPLIFIER TRANSISTORS

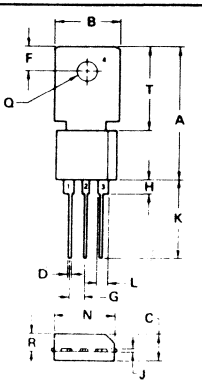


MAXIMUM RATINGS

Rating	Symbol	BF466	BF467	BF468	Unit
Collector-Emitter Voltage	V_{CEO}	150	200	250	Vdc
Collector-Base Voltage	V_{CBO}	150	200	250	Vdc
Emitter-Base Voltage	V_{EBO}	5			Vdc
Collector Current — Continuous Peak	I_C	1 2			Adc
Base Current	I_B	300			mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 16			Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80			Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150			°C
Solder Temperature, 1/16" from Case for 10 Seconds	–	260			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W



STYLE 1
PIN 1 EMITTER
2 BASE
3 COLLECTOR
4 COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

CASE 306-04

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BF466	BV_{CEO}	150	–	Vdc
	BF467		200	–	
	BF468		250	–	
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BF466	BV_{CBO}	150	–	Vdc
	BF467		200	–	
	BF468		250	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	5	–	Vdc
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 100, Vdc, I_E = 0)	BF466		–	0.1	
(V_{CB} = 150, Vdc, I_E = 0)	BF467		–	0.1	
(V_{CB} = 200, Vdc, I_E = 0)	BF468		–	0.1	
Emitter Cutoff Current (V_{BE} = 4 Vdc, I_C = 0)		I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 10 mA, V_{CE} = 10 Vdc)			40	–	
(I_C = 100 mA, V_{CE} = 10 Vdc)			40		
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 200 mAdc, I_B = 20 mAdc)			–	1.5	
Base-Emitter On Voltage (I_C = 200 mA, V_{CE} = 1 Vdc)		$V_{BE(on)}$		1	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 50 mA, V_{CE} = 20 Vdc, f = 20 MHz)		f_T	100		MHz
Collector output capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	12	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 0.1 MHz)		C_{ib}	–	110	pF

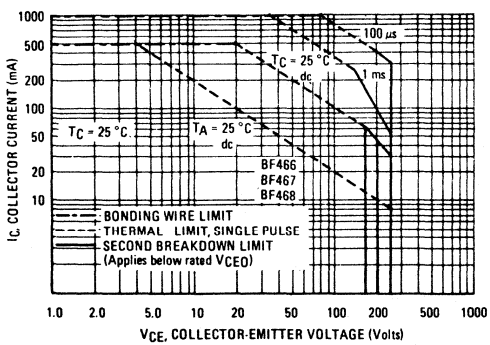


FIGURE 1 – ACTIVE-REGION SAFE-OPERATING AREA

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

3

TYPICAL CHARACTERISTICS

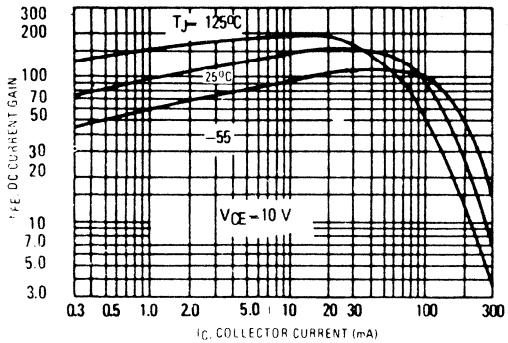


FIGURE 2 – DC CURRENT GAIN

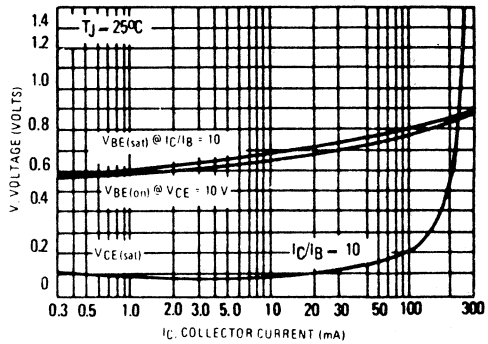


FIGURE 3 – "ON" VOLTAGES

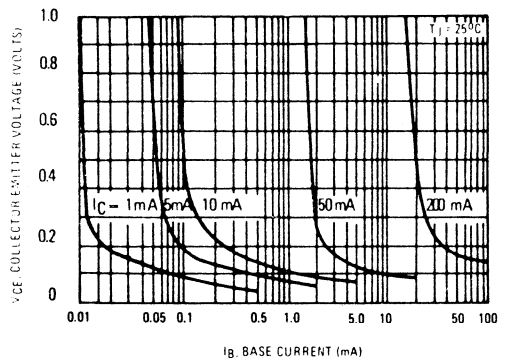


FIGURE 4 – COLLECTOR SATURATION REGION

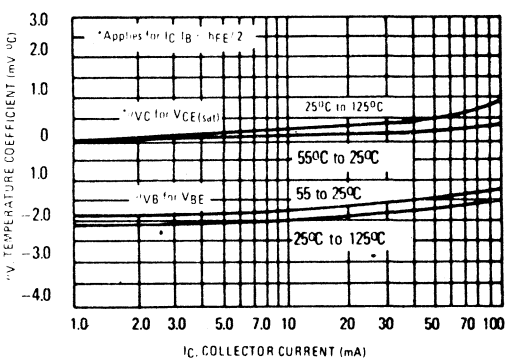


FIGURE 5 – TEMPERATURE COEFFICIENTS

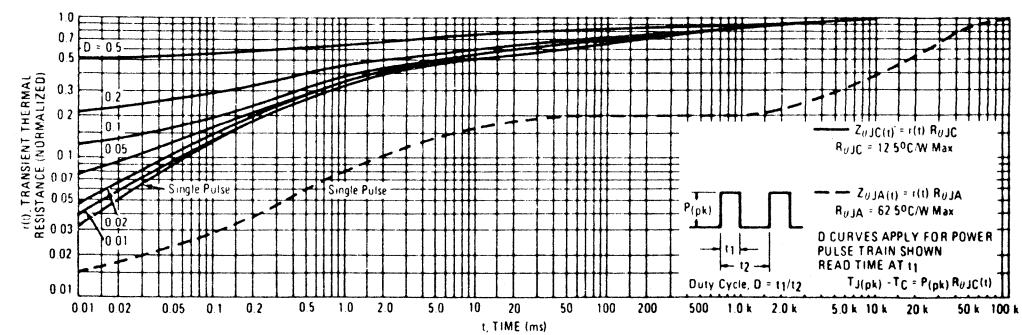


FIGURE 6 – THERMAL RESPONSE

TYPICAL CHARACTERISTICS (continued)

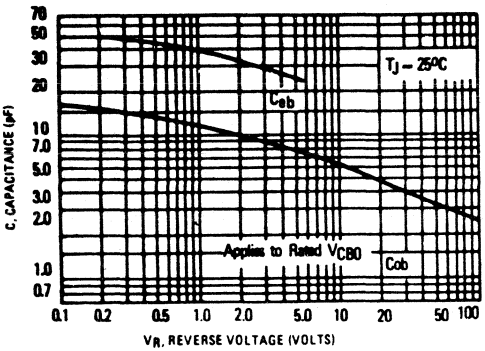


FIGURE 7 – CAPACITANCE

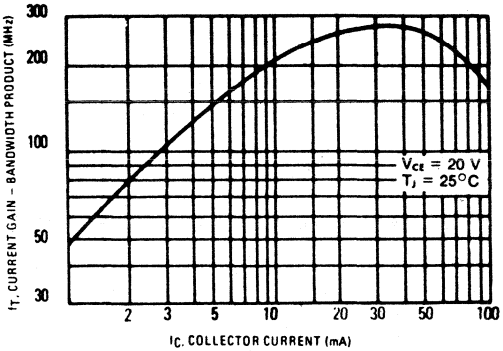


FIGURE 8 – CURRENT-GAIN – BANDWIDTH PRODUCT

3

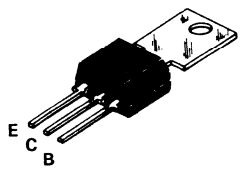
BF757
BF758
BF759

NPN SILICON ANNULAR HIGH VOLTAGE AMPLIFER TRANSISTORS

. . . designed for high-voltage TV video and chroma output circuits, high-voltage linear amplifiers, and high-voltage transistor regulators.

- High Collector-Emitter Breakdown Voltage –
  BV_{CEO} = 350 Vdc (Min) @ I_C = 1.0 mAdc – BF759
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.6 Vdc (Max) @ I_C = 30 mAdc
- Low Collector-Base Capacitance –
  C_{re} = 3.0 pF (Max) @ V_{CB} = 20 Vdc
- Duowatt Package –
  2 Watts Free Air Dissipation @ T_A = 25°C
- Complements to NPN BF760/BF761/BF762

NPN SILICON AMPLIFIER TRANSISTORS

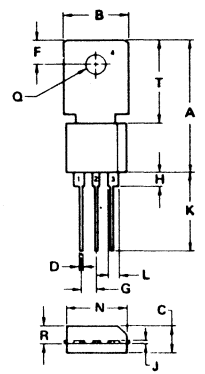


MAXIMUM RATINGS

Rating	Symbol	BF757	BF758	BF759	Unit
*Collector-Emitter Voltage	V_{CEO}	250	300	350	Vdc
*Collector-Base Voltage	V_{CBO}	250	300	350	Vdc
*Emitter-Base Voltage	V_{EBO}	← 6.0 →			Vdc
*Collector Current – Continuous Peak	I_C	← 0.5 → ← 0.7 →			Adc
*Base Current	I_B	← 250 →			mAdc
*Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	← 2.0 → ← 16 →			Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 10 → ← 80 →			Watts mW/°C
*Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -55 to +150 →			°C
*Solder Temperature, 1/16" from Case for 10 Seconds	–	← 260 →			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W



STYLE 2
PIN 1. EMITTER
2. COLLECTOR
3. BASE
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

CASE 306-04

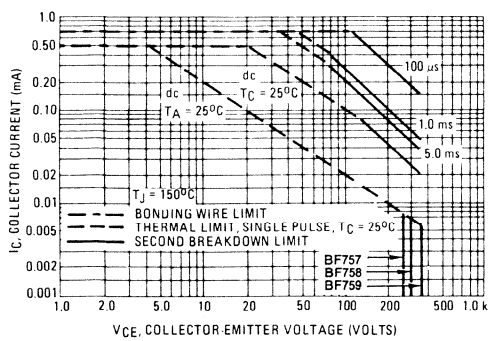
***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BF757	BV_{CEO}	250	–	Vdc
	BF758		300	–	
	BF759		350	–	
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BF757	BV_{CBO}	250	–	Vdc
	BF758		300	–	
	BF759		350	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	6.0	–	Vdc
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 150 Vdc, I_E = 0)	BF757		–	0.2	
(V_{CB} = 200 Vdc, I_E = 0)	BF758		–	0.2	
(V_{CB} = 250 Vdc, I_E = 0)	BF759		–	0.2	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS(1)					
DC Current Gain		h_{FE}			–
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)			25	–	
(I_C = 30 mAdc, V_{CE} = 10 Vdc)			40	180	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 30 mAdc, I_B = 3.0 mAdc)			–	0.6	
(I_C = 50 mAdc, I_B = 5 mAdc)			–	1.5	
Base-Emitter On Voltage (I_C = 30 mAdc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 20 MHz)		f_T	45	200	MHz
Common Emitter Reverse Transfer Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)		Cre	–	3.0	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

3

TYPICAL CHARACTERISTICS



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

FIGURE 1 – ACTIVE-REGION SAFE-OPERATING AREA

TYPICAL CHARACTERISTICS (continued)

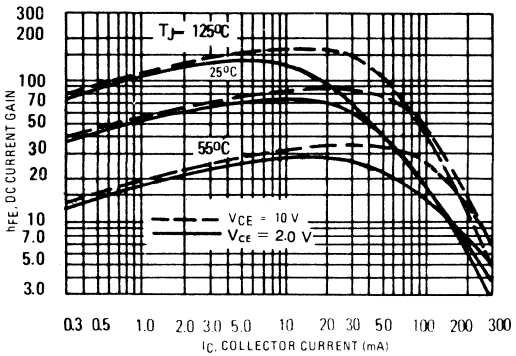


FIGURE 2 – DC CURRENT GAIN

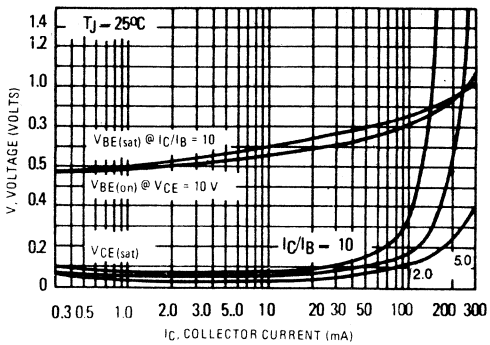


FIGURE 3 – "ON" VOLTAGES

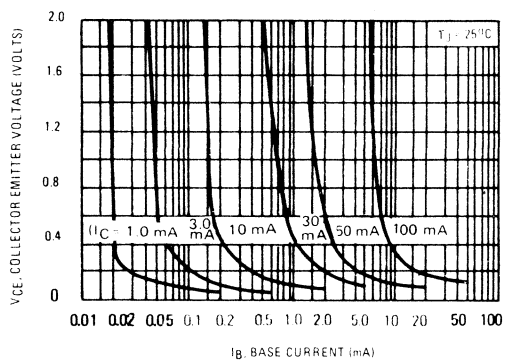


FIGURE 4 – COLLECTOR SATURATION REGION

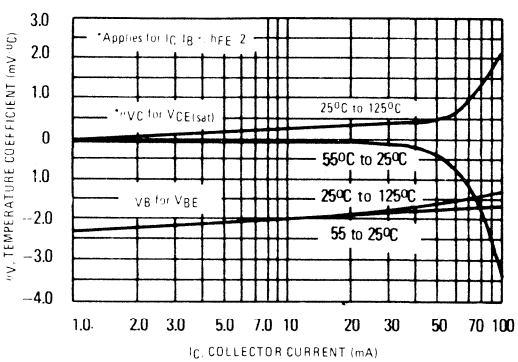


FIGURE 5 – TEMPERATURE COEFFICIENTS

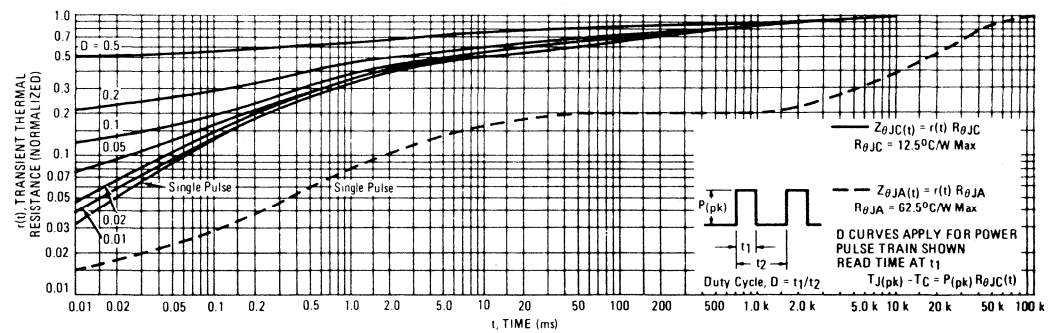


FIGURE 6 – THERMAL RESPONSE

TYPICAL CHARACTERISTICS (continued)

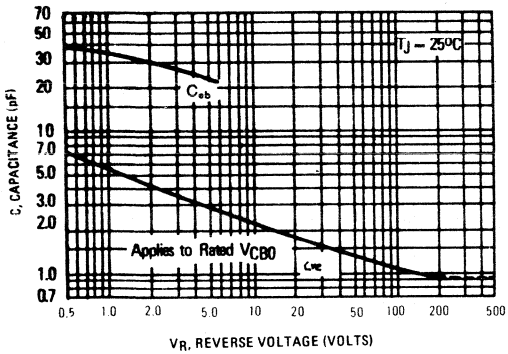


FIGURE 7 – CAPACITANCE

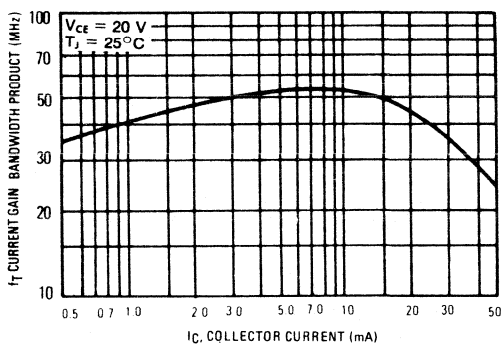


FIGURE 8 – CURRENT-GAIN – BANDWIDTH PRODUCT

3

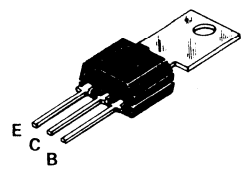
BF760
BF761
BF762

PNP SILICON ANNULAR◆ HIGH VOLTAGE AMPLIFIER TRANSISTORS

designed for high-voltage TV video and chroma output circuits, high-voltage linear amplifiers, and high-voltage transistor regulators.

- High Collector-Emitter Breakdown Voltage –
  BV_{CEO} = 350 Vdc (Min) @ I_C = 1.0 mAdc – BF762
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.75V (Max) @ I_C = 30 mAdc
- Low Collector-Base Capacitance –
  C_{re} = 3.0 pF (Max) @ V_{CB} = 60 Vdc
- Duowatt Package –
  2 Watts Free Air Dissipation @ T_A = 25°C
- Complementary to NPN BF757/BF758/BF759

PNP SILICON AMPLIFIER TRANSISTORS

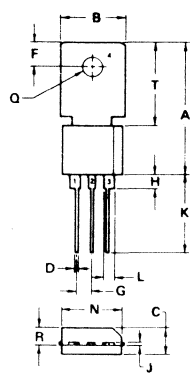


MAXIMUM RATINGS

Rating	Symbol	BF760	BF761	BF762	Unit
*Collector-Emitter Voltage	V_{CEO}	250	300	350	Vdc
*Collector-Base Voltage	V_{CBO}	250	300	350	Vdc
*Emitter-Base Voltage	V_{EBO}	5			Vdc
*Collector Current – Continuous Peak	I_C	0.5 0.7			Adc
*Base Current	I_B	250			mAdc
*Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 16			Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80			Watts mW/°C
*Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150			°C
*Solder Temperature, 1/16" from Case for 10 Seconds	–	260			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W



STYLE 2
PIN 1. EMITTER
2. COLLECTOR
3. BASE
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

CASE 306-04

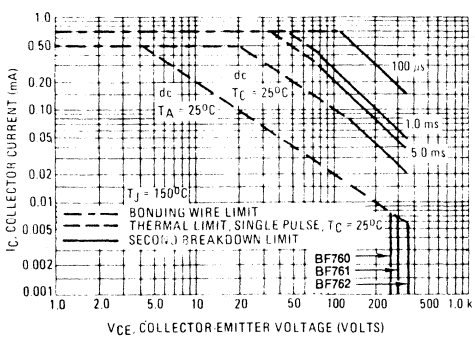
***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BF760	BV_{CEO}	250	–	Vdc
	BF761		300	–	
	BF762		350	–	
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BF760	BV_{CBO}	250	–	Vdc
	BF761		300	–	
	BF762		350	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	5	–	Vdc
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 150 Vdc, I_E = 0)	BF760		–	0.2	
(V_{CB} = 200 Vdc, I_E = 0)	BF761		–	0.2	
(V_{CB} = 250 Vdc, I_E = 0)	BF762		–	0.2	
Emitter Cutoff Current (V_{BE} = 3 Vdc, I_C = 0)		I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS(1)					
DC Current Gain		h_{FE}			–
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)			25	–	
(I_C = 30 mAdc, V_{CE} = 10 Vdc)			40	180	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 30 mAdc, I_B = 3.0 mAdc)			–	0.75	
			–		
Base-Emitter On Voltage (I_C = 30 mAdc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	–	0.85	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 20 MHz)		f_T	45	200	MHz
Common Emitter Reverse Transfer Capacitance (V_{CB} = 60 Vdc, I_E = 0, f = 1.0 MHz)		Cre	–	3	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

3

TYPICAL CHARACTERISTICS



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

FIGURE 1 – ACTIVE-REGION SAFE-OPERATING AREA

TYPICAL CHARACTERISTICS (continued)

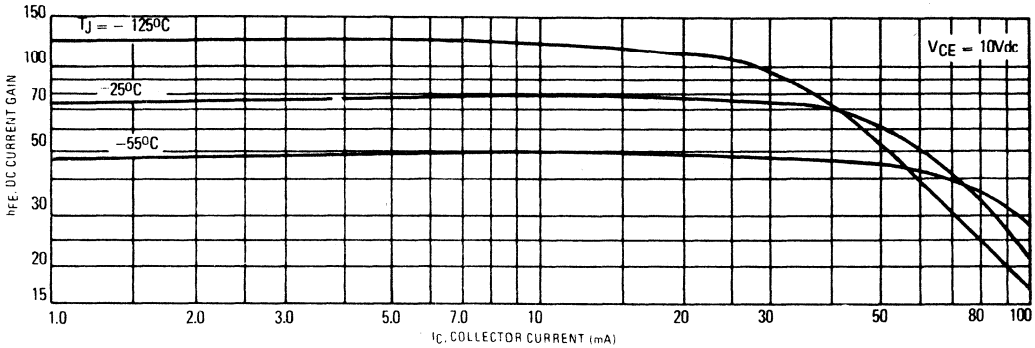


FIGURE 2 – DC CURRENT GAIN

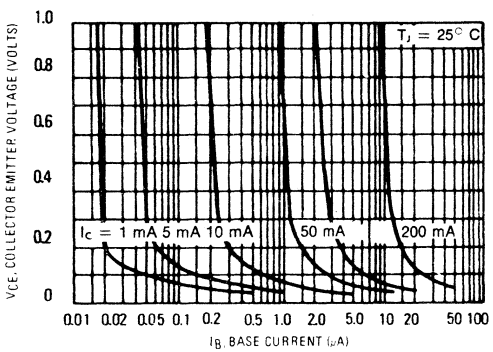


FIGURE 3 – COLLECTOR SATURATION REGION

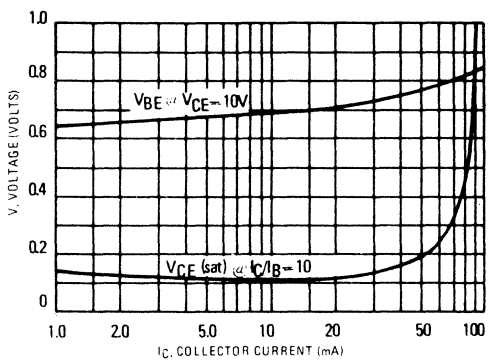


FIGURE 4 – "ON" VOLTAGES

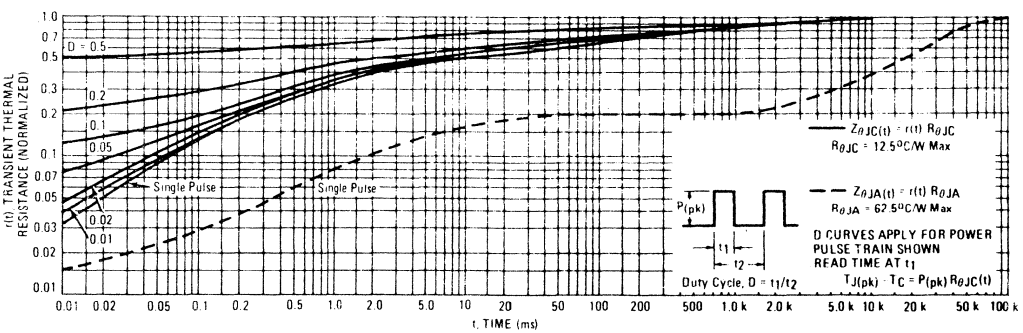


FIGURE 5 – THERMAL RESPONSE

TYPICAL CHARACTERISTICS (continued)

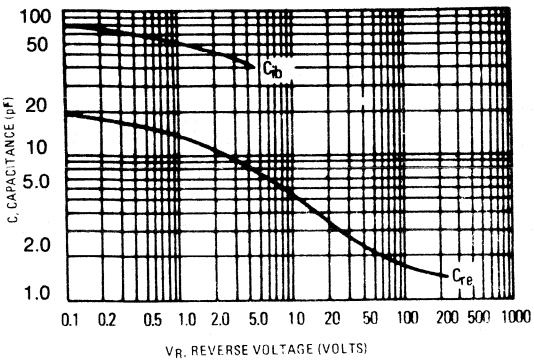


FIGURE 6 – CAPACITANCE

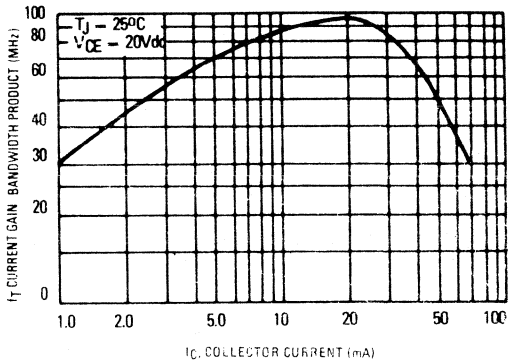


FIGURE 7 – CURRENT-GAIN – BANDWIDTH PRODUCT

3

BU205

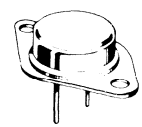
HORIZONTAL DEFLECTION SILICON TRANSISTORS

. . . designed for use in color televisions receivers.

- Collector-Emitter Voltage V_{CES} 1500 Volts
- Collector Current I_C = 2.5 A
- Fall time @ I_C = 4.5 Adc, I_B = 1.8 A
  T_f = 0.75 μs (Typ) – T_f = 1.0 μs (Max)

2.5 AMPERES
NPN SILICON
POWER TRANSISTOR
TRIPLE DIFFUSED

1500 VOLTS
36 WATTS



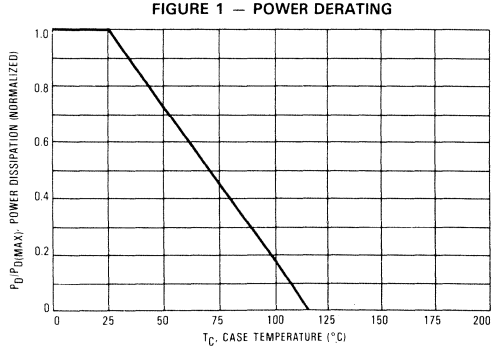
MAXIMUM RATINGS

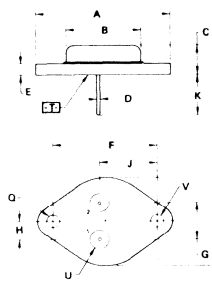
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	700	Vdc
Collector-Base Voltage	V_{CBO}	1500	Vdc
Emitter-Base Voltage	V_{EBO}	5	Vdc
Collector-Emitter Voltage (V_{BE} = −1.5 V)	V_{CEX}	1500	Vdc
Collector-Emitter Voltage (R_{BE} = 100Ω)	V_{CER}		Vdc
Collector Current – Continuous – Peak (pw ≦ 10 ms)	I_C I_{CM}	2.5 3.0	Adc Apk
Base-Current continuous	I_B	2.5	Adc
Total Power Dissipation @ T_C = 25°C	P_D	56	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +115	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R\theta_{JC}$	2.5	°C/W

FIGURE 1 — POWER DERATING





NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. T IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q
   ⌖ ⌀13 (0.005) Ⓜ T V Ⓜ
   FOR LEADS
   ⌖ ⌀13 (0.005) Ⓜ T V Ⓜ Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 (TO-3)

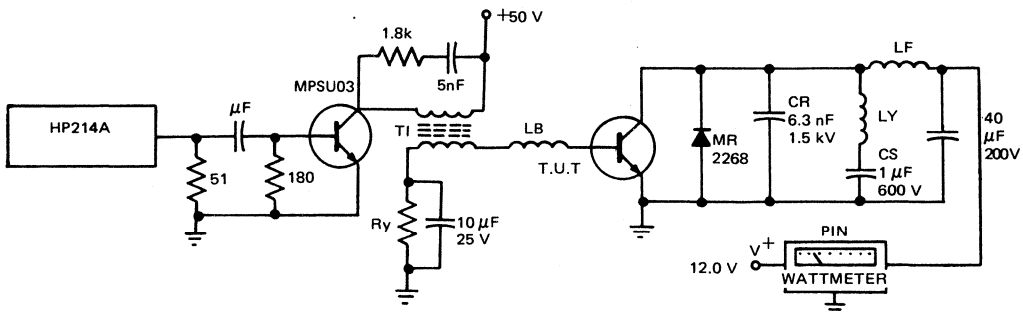
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Voltage (I_C = 100 mA, L = 25 mH)	$V_{CEO(sus)}$	700	–	–	Vdc
Collector Cutoff Current (V_{CE} = 1500 Vdc, V_{BE} = 0)	I_{CES}			1.0	mAdc
Emitter-Base Voltage (I_C = 0, I_E = 10 mA)	V_{EBO}	5.0	7		Vdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}			10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2 A, V_{CE} = 5 V)	H_{FE}	2			–
Collector-Emitter Saturation Voltage (I_C = 2 Adc, I_B = 1.0 Adc)	$V_{CE(sat)}$			5.0	Vdc
Base Emitter Saturation Voltage (I_C = 2 Adc, I_B = 1.0 Adc)	$V_{BE(sat)}$			1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased (t = 1.0 s, V_{CE} = 100 Vdc)	$I_{S/b}$	200			mAdc
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	f_T		7.5		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}		65		pF
SWITCHING CHARACTERISTICS					
Fall Time (I_C = 2 Adc, I_{B1} = 1 Adc, L_B = 25 μH)	t_f		0.75	1.0	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

3

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



BASE CIRCUIT VALUES

	RB	LB
SWITCH-TEST	2.5	12
OPTIMUM	7	15

LY = 5.5 mH
LF = 2 mH
LB = 25 μH
RB = 7 Ω

FLASHOVER PERFORMANCE

The BU205 is guaranteed to the following additional maximum ratings

	BU205	
I_C PEAK	5 A	20 pulses maximum of Pulse Width ≤ 50 μS. Duty cycle ≤ 50%.
Followed by		
V_{CES} PEAK.	1650 V	

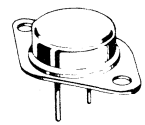
BU208, 208A
BU209, 209A

HORIZONTAL DEFLECTION TRANSISTORS

. . . designed for use in televisions.

- Collector-Emitter Voltages V_{CES} 1500/1700 Volts
- Fast Switching – 400 ns Typical Fall Time
- Low $V_{CE(sat)}$ 0.3 Vdc Typical at 4.5 Adc/2.25 Adc (BU208A)
- Low thermal Resistance 1 °C/W increased reliability
- Glass passivated (patented photoglass). Triple diffused Mesa Technology for long term stability.

6 AND 7 AMPERES
NPN SILICON
POWER TRANSISTORS
1500 to 1700 VOLTS



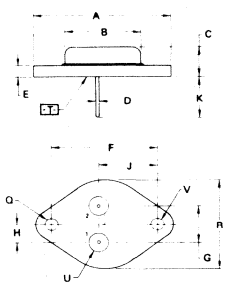
MAXIMUM RATINGS

Rating	Symbol	BU208 BU208A	BU209 BU209A	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	700	800	Vdc
Collector-Emitter Voltage	V_{CES}	1500	1700	Vdc
Emitter-Base Voltage	V_{EB}	5	5	Vdc
Collector Current – Continuous – Peak	 I_C I_{CM}	 7 (5) 15 (7.5)	 6 (4) 12 (6)	Vdc
Base Current – Continuous – Peak (Negative)	 I_B I_{BM}	 4 3.5		Adc
Total Power Dissipation at T_C = 95°C Derate above 95°C	P_D	 20 (12.5) 1 (0.625)		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +115		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R\theta_{JC}$	1.0 (1.6)	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	275	°C

NOTE: 1. Pulsed 5 ms, Duty Cycle ≦ 10%.
2. See page 3 for Additional Ratings on A Type.
3. Figures in ( ) are Standard Ratings Motorola Guarantees are Superior.



NOTES
1. DIMENSIONS Q AND V ARE DATUMS
2. T IS SEATING PLANE AND DATUM
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q
   ⌖ ⌀13 (0.005) M T V M
   FOR LEADS
   ⌖ ⌀13 (0.005) M T V M Q M
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 (TO-3)

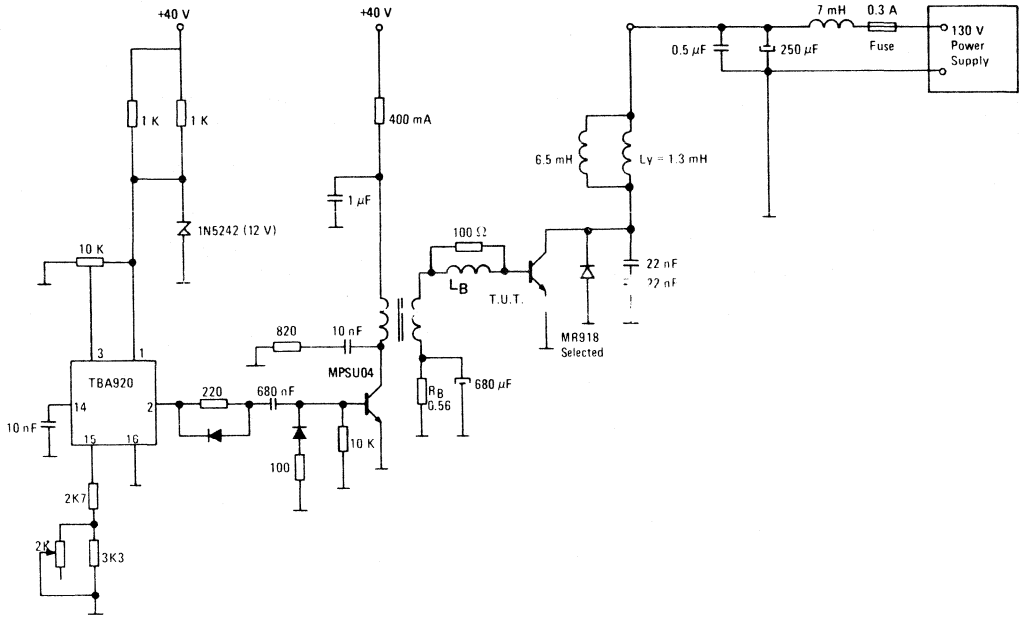
3

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristics		Symbol	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, L = 25 mH)	BU208/BU208A BU209/BU209A	$V_{CEO(sus)}$	 700 800			Vdc
Collector Cutoff Current[1] (V_{CE} = rated V_{CES}, V_{BE} = 0)	ALL TYPES	I_{CES}			1.0	mAdc
Emitter Base Voltage[1] (I_C = 0, I_E = 10 mAdc) (I_C = 0, I_E = 100 mAdc)		V_{EBO}	5	 7		Vdc
ON CHARACTERISTICS[1]						
DC Current Gain		h_{FE}				
(I_C = 4.5 Adc, V_{CE} = 5 Vdc) (I_C = 3 Adc, V_{CE} = 5 Vdc)	BU208/BU208A BU209/BU209A		2.25 2.25			
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 4.5 Adc, I_B = 2 Adc) (I_C = 4.5 Adc, I_B = 2 Adc) (I_C = 3 Adc, I_B = 1.3 Adc)	BU208 BU208A BU209/BU209A				5 1 5	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 4.5 Adc, I_B = 2 Adc) (I_C = 3 Adc, I_B = 1.3 Adc)	BU208/BU208A BU209/BU209A				1.5 1.5	
DYNAMIC CHARACTERISTICS						
Current-Gain Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 5 Vdc, f_{test} = 1 MHz)		f_T		4		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0), f_{test} = 1 MHz)		C_{ob}		125		pF
SWITCHING CHARACTERISTICS						
Storage Time (see test circuit fig. 1) (I_C = 4.5 Adc, I_{B1} = 1.8 Adc, L_B = 10 μH)		t_s		8		μS
Fall time (see test circuit fig. 1) (I_C = 4.5 Adc, I_{B1} = 1.8 Adc, L_B = 10 μH)		t_f		0.4		μS

[1] Pulse test: PW = 300 μS; Duty cycle ≤ 2%.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT

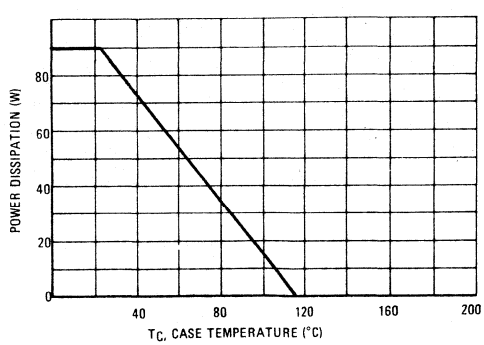


FLASHOVER PERFORMANCE

The BU207A, BU208A, and BU209A are guaranteed to the following additional maximum ratings

	BU208A	BU209A	
I_C PEAK	10A	8A	20 pulses maximum of Pulse Width ⩽ 50 μS. Duty cycle ⩽ 50%.
Followed by			
V_{CES} PEAK	1650V	1850V	

FIGURE 2 – POWER DERATING



BASE DRIVE
The Key to Performance

By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM}. Worst-case component variations and maximum high voltage loading must also be taken into account.

If the base of the output transistor is driven by a very low impedance source, the turn-off base current will reverse very quickly as shown in Fig. 3. This results in rapid, but only partial collector turn-off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Fig. 4, thus allowing axcess carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right L_B is usually done empirically since the equivalent circuit is complex, and since there are several important variables (I_{CM}, I_{B1}, and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B, at the desired conditions, for several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values of L_B. This shows the parameter that really matters, dissipation, whether caused by switching or by saturation. For very low L_B a very narrow optimum is obtained. This occurs when $I_{B1} \cdot h_{FE} \cong I_{CM}$, and therefore would be acceptable only for the "typical" device with constant I_{CM}. As L_B is increased, the curves become broader and flatter above the $I_{B1} \cdot h_{FE} = I_{CM}$ point as the turn off "tails" are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor initiation of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE}, essentially moves the curves to the left, or right according to the relation $I_{B1} \cdot h_{FE}$ = constant. It then becomes obvious that, for a specified I_{CM}, an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1}. The only remaining decision is to pick I_{B1} high enough to accomodate the lowest h_{FE} part specified. Neither L_B nor I_{B1} are absolutely critical. Due to the high gain of Motorola devices it is suggested that in general a low value of I_{B1} be used to obtain optimum efficiency— eg. for BU208A with $I_{CM} = 4.5$ A use $I_{B1} \approx 1.5$ A, at $I_{CM} = 4$ A use $I_{B1} \approx 1.2$ A. These values are lower than for most competition devices but practical tests have showed comparable efficiency for Motorola devices even at the higher level of I_{B1}.

An L_B of 10 uH to 12 uH should give satisfactory operation of BU208A with I_{CM} of 4 to 4.5 A and I_{B1} between 1.2 and 2 A.

TEST CIRCUIT WAVEFORMS

FIGURE 3

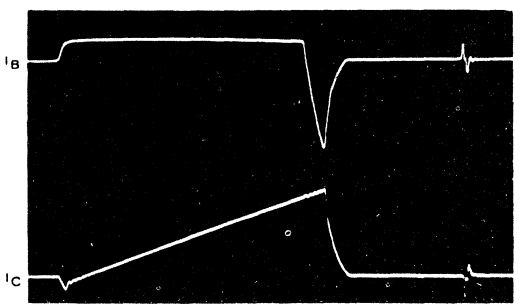
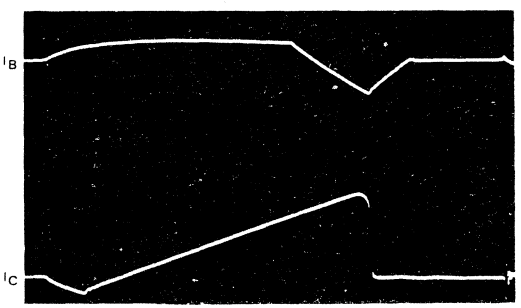


FIGURE 4



TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance. Once the required transistor operating current is determined, fixed circuit values may be selected.

FIGURE 5 – DC CURRENT GAIN

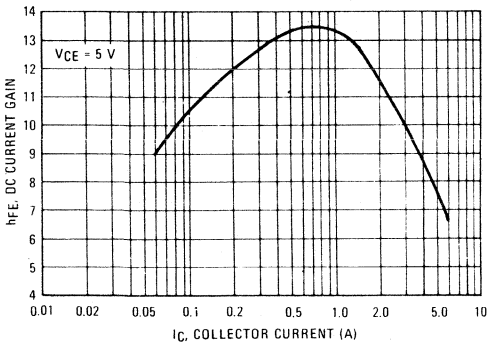


FIGURE 6 – COLLECTOR-EMITTER SATURATION VOLTAGE

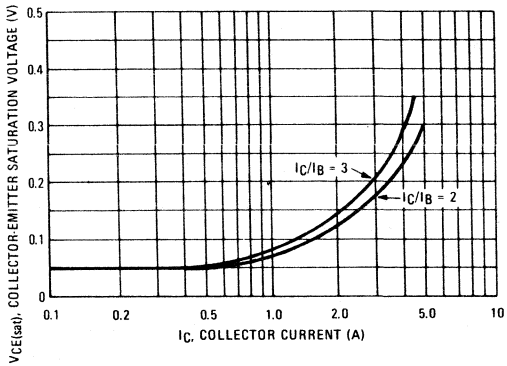


FIGURE 7 – BASE EMITTER SATURATION VOLTAGE

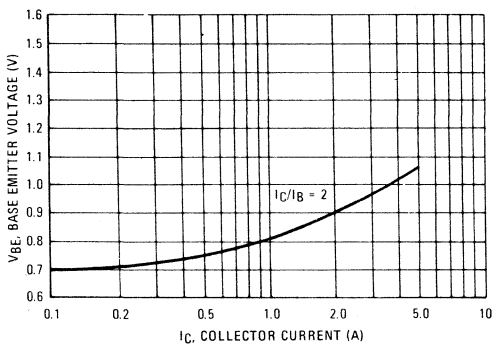


FIGURE 8 – COLLECTOR SATURATION REGION

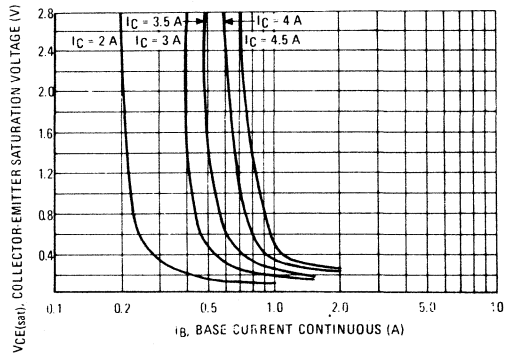
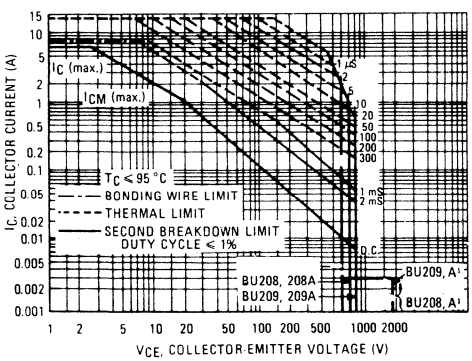


FIGURE 9 – MAXIMUM FORWARD BIAS SAFE OPERATING AREA



[1] Pulse width ≤ 20 μs. Duty cycle ≤ 0.25. R_{BE} ≤ 100 Ohms.

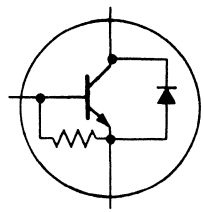
3

BU 208D

NPN SILICON HORIZONTAL DEFLECTION TRANSISTOR WITH INTEGRATED DAMPER DIODE

. . . specifically designed for use in large screen color deflection circuits

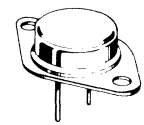
- V_{CES} = 1500 V;
  $V_{CEO(sus)}$ = 700 V (min.)
- Low saturation:
  $V_{CE(sat)}$ = 1 V (max.) @ Ic = 4.5 Adc



5 AMPERES

NPN SILICON POWER TRANSISTOR

1500 VOLTS
60 WATTS



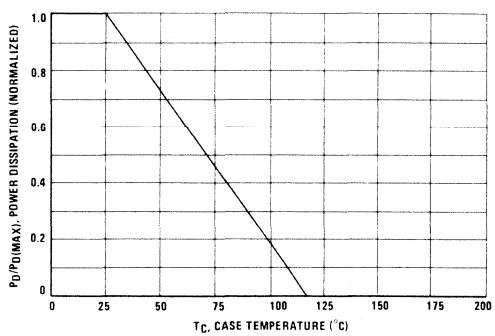
MAXIMUM RATINGS

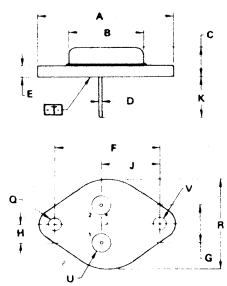
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	700	Vdc
Collector-Emitter Voltage (R_{BE} = 0)	V_{CES}	1500	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Collector-Current – Continuous – Peak	I_C I_{CM}	5 7.5	Adc
Base Current – Peak	I_B	3.5	Adc
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	60 0.666	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 115	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.5	°C/W

FIGURE 1 – POWER DERATING





NOTES:
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2. T IS SEATING PLANE AND DATUM
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q
   ⌖ ⌀ 13 (0.005) M T V M
   FOR LEADS:
   ⌖ ⌀ 13 (0.005) M T V M Q M
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0, L = 25 mH, Vclamp = 800 V)	$V_{CEO(sus)}$	700		Vdc
Collector Cutoff Current (V_{CES} = 1500 Vdc, R_{BE} = 0)	I_{CES}		1.0	mAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}		300	mAdc
ON CHARACTERISTICS				
Diode Forward Voltage (I_F = 4 A)	V_F		2.0	Vdc
Collector-Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 2.0 Adc)	$V_{CE(sat)}$		1.0	Vdc
Base-Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 2.0 Adc)	$V_{BE(sat)}$		1.5	Vdc

3

SWITCHING CHARACTERISTICS (Resistive Load)

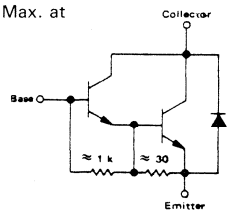
Fall Time	I_C (end) = 4.5 Adc, V_{CC} = Vdc, I_B (end) = 1.8 A, L_C = 0.9 mH, L_B = 10 μH	t_f	–	0.6 (typ)	μs

BU323
BU323A

NPN SILICON POWER DARLINGTON TRANSISTOR

The BU323, BU323A are monolithic darlington transistors designed for automotive ignition, switching regulator and motor control applications.

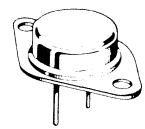
- V_{CE} Sat Specified at -40°C = 2 V Max. at I_C = 6 A.
- 550 mJ Energy Capability Tested in Automotive Ignition Circuit.
- Photoglass Passivation for Reliability and Stability.



16 AMPERE PEAK

POWER TRANSISTORS DARLINGTON NPN SILICON

350 - 400 VOLTS
175 WATTS



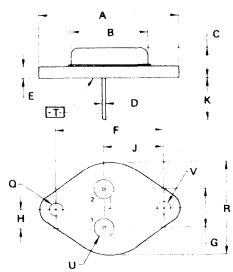
MAXIMUM RATINGS

Rating	Symbol	BU323	BU323A	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	350	400	Vdc
Collector-Base Voltage	V_{CBO}	500	600	Vdc
Emitter-Base Voltage	V_{EBO}	8	8	Vdc
Collector Current — Continuous Peak (1)	I_C	10 16	10 16	Adc
Base Current — Continuous	I_B	3	3	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1	175 100 1	Watts Watts W/°C
Operating and Storage Junction	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



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U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS[1]						
Collector-Emitter Sustaining Voltage (Figure 1) L = 10 mH (I_C = 200 mAdc, I_B = 0, V_{clamp} = Rated V_{CEO})	 BU323 BU323A	$V_{CEO(sus)}$	 350 400			Vdc
Collector-Emitter sustaining Voltage (Figure 1) (I_C = 3 A, R_{BE} = 100 Ohms, L = 500 μH) Unclamped	 BU323 BU323A	$V_{CER(sus)}$	 400 475			Vdc
Collector Cutoff Current (Rated V_{CER}, R_{BE} = 100 Ohms)		I_{CER}			1	mAdc
Collector Cutoff Current (Rated V_{CBO}, I_E = 0)		I_{CBO}			1	mAdc
Emitter Cutoff Current (V_{EB} = 6 Vdc, I_C = 0)		I_{EBO}			40	mAdc
ON CHARACTERISTICS[1]						
DC Current Gain (I_C = 3 Adc, V_{CE} = 6 Vdc) (I_C = 6 Adc, V_{CE} = 6 Vdc) (I_C = 10 Adc, V_{CE} = 6 Vdc)		h_{FE}	 300 150 50	 550 350 150	 2000	
Collector-Emitter Saturation Voltage (I_C = 3 Adc I_B = 60 mAdc) (I_C = 6 Adc, I_B = 120 mAdc) (I_C = 10 Adc, I_B = 300 mAdc) (I_C = 6 Adc, I_B = 120 mAdc, T_C = -40 °C)		$V_{CE(sat)}$			 1.5 1.7 2.7 2.0	Vdc
Base-Emitter Saturation Voltage (I_C = 6 Adc, I_B = 120 mAdc) (I_C = 10 Adc, I_B = 300 mAdc) (I_C = 6 Adc, I_B = 120 mAdc, T_C = -40 °C)		$V_{BE(sat)}$			 2.2 3 2.4	Vdc
Base-Emitter On Voltage (I_C = 10 Adc, V_{CE} = 6 Vdc)		$V_{BE(on)}$			2.5	Vdc
Diode Forward Voltage (I_F = 10 Adc)		V_f		2	3.5	Vdc
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)		C_{ob}		165	350	pF
SWITCHING CHARACTERISTICS						
Storage Time	(V_{CC} = 12 Vdc, I_C = 6 Adc, I_{B1} = I_{B2} = 0.3 Adc) Fig. 2	t_s		7.5	15	μs
Fall Time		t_f		5.2	15	μs
FUNCTIONAL TESTS						
Second Breakdown Collector Current with Base-Forward Biased		$I_{S/B}$		See Figure 10		
Pulsed Energy Test (See Figure 12)		$\frac{I_C^2 L}{2}$	550			mJ

[1] Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

FIGURE 1 – SUSTAINING VOLTAGE TEST CIRCUIT

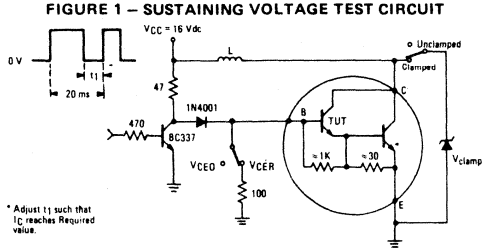

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

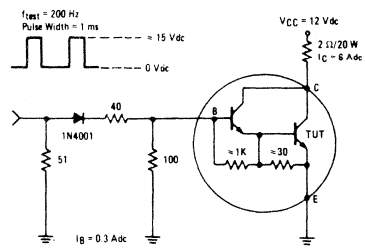

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FIGURE 3 – DC CURRENT GAIN

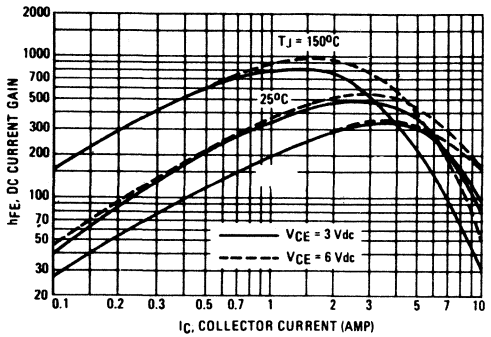


FIGURE 4 – COLLECTOR-SATURATION REGION

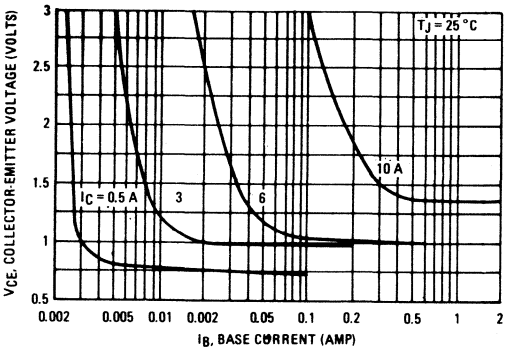


FIGURE 5 – COLLECTOR-EMITTER SATURATION VOLTAGE

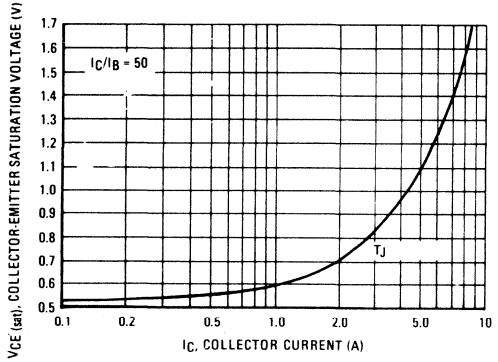


FIGURE 6 – BASE-EMITTER VOLTAGE

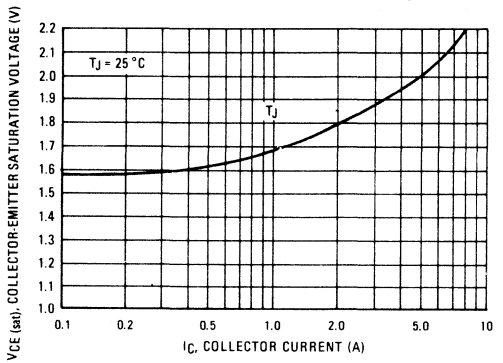


FIGURE 7 – TURN-OFF SWITCHING TIME

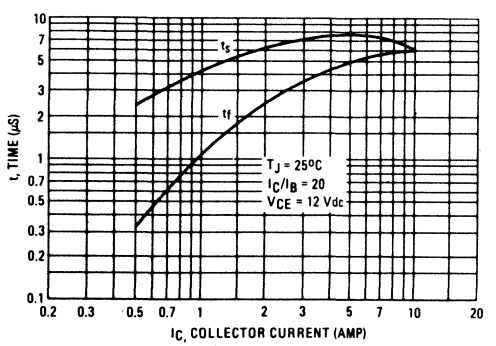


FIGURE 8 – COLLECTOR CUTOFF REGION

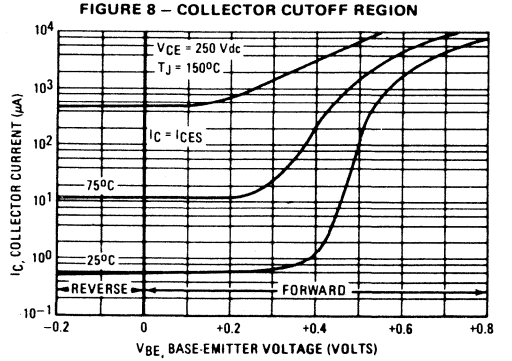


FIGURE 9 – THERMAL RESPONSE

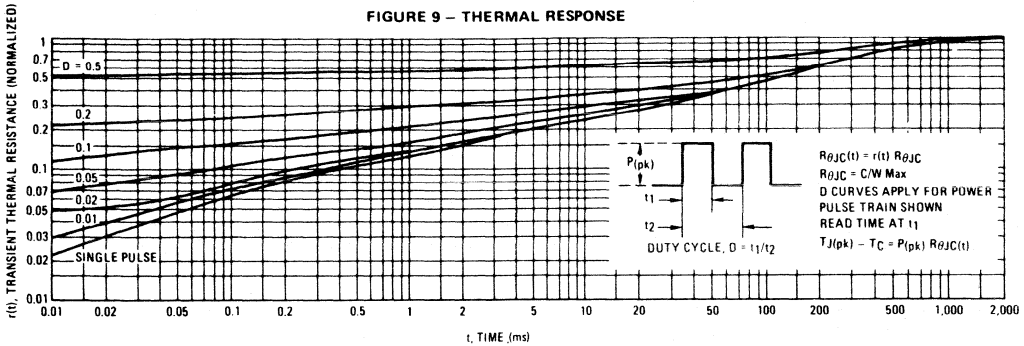
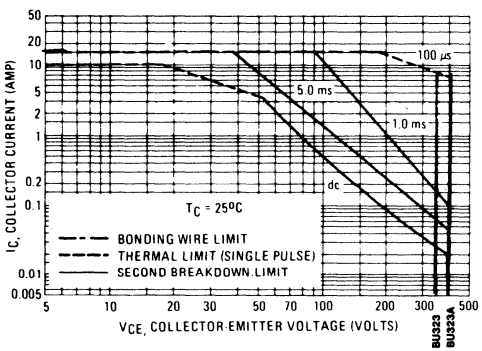


FIGURE 10 – FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 11 – POWER DERATING

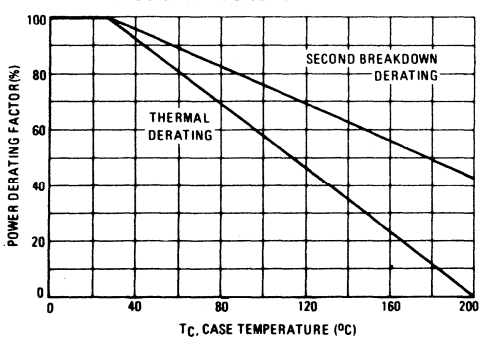
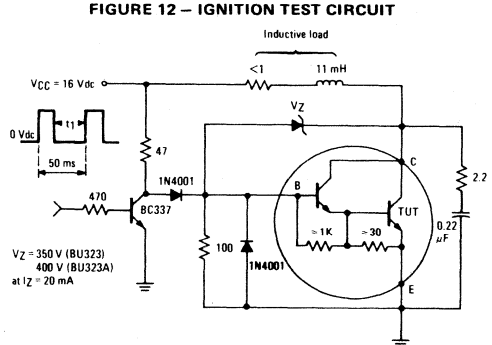


FIGURE 12 – IGNITION TEST CIRCUIT



t1 to be selected such that I_C reaches 10 Adc before switch-off.

NOTE: Figure 12 specifies energy handling capabilities in an automotive ignition circuit.

BU 326
BU 326A

HIGH VOLTAGE NPN SILICON TRANSISTOR

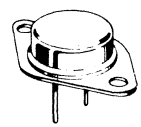
. . . Designed for use in the switch-mode power supplies of colour television receivers.

- Collector-Emitter Voltage V_{CES} = 800 V and 900 V
- Collector-Current I_C = 6 A DC
- Low collector emitter saturation voltage
  $V_{CE\ (sat)}$ = 3 V max. at I_C = 4 A
- Fall time at I_C = 2.5 A
  T_F = 1 μs max. at T_C = 100 °C

6 AMPERES

NPN SILICON POWER TRANSISTORS

375, 400 VOLTS
90 WATTS



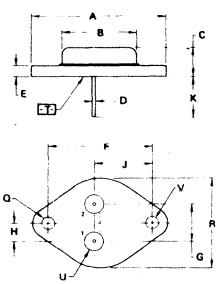
MAXIMUM RATINGS

Rating	Symbol	BU326	BU326A	Unit
Collector-Emitter Voltage	$V_{CEO\ (sus)}$	375	400	Vdc
Collector-Emitter Voltage	V_{CES}	800	900	Vdc
Emitter Base Voltage	V_{EB}	10		Vdc
Collector Current – Continuous – Peak[1]	I_C I_{CM}	6 8		Adc
Base Current – Continuous – Peak[1]	I_B I_{BM}	2 3		Adc
Reverse Base Current 20 ms max. – Peak during turn off	I_B I_{BM}	100 3		mA A
Total Power Dissipation Derate above 25 °C	P_D	90 0.6		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +175		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	$R\theta_{JC}$	1.65	°C/W

[1] Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. T IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q
   ⌖ ⌀.13 (0.005) M T V M
   FOR LEADS:
   ⌖ ⌀.13 (0.005) M T V M Q M
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

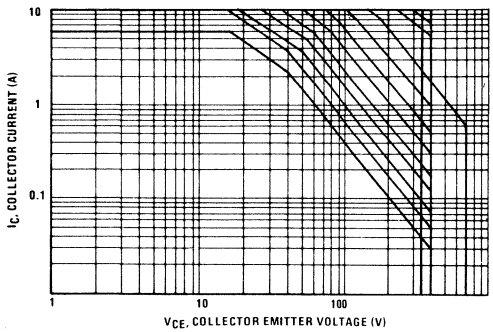
ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS[1]						
Collector-Emitter Sustaining Voltage (I_C = 100 mA, I_B = 0, L = 25 mH)	BU326	$V_{CEO\ (sus)}$	375			Vdc
	BU326A		400			
Collector-Cutoff Current (V_{CE} = 800 V, V_{BE} = 0)	BU326	I_{CES}			1.0	mAdc
(V_{CE} = 900 V, V_{BE} = 0)	BU326A				1.0	
Collector Cutoff Current (V_{CE} = 800 V, V_{BE} = 0, T_J = 125 °C)	BU326	I_{CES}			2.0	mAdc
(V_{CE} = 900 V, V_{BE} = 0, T_J = 125 °C)	BU326A				2.0	
Emitter Cutoff Current (V_{EB} = 10 V, I_C = 0)		I_{EBO}			10	mAdc
ON CHARACTERISTICS[1]						
DC Current Gain (I_C = 0.6 A, V_{CE} = 5 V)		h_{FE}		30		–
Collector-Emitter Saturation Voltage (I_C = 2.5 A, I_B = 0.25 A)		$V_{CE\ (sat)}$			10	Vdc
(I_C = 4.0 A, I_B = 1.25 A)					3	
Base-Emitter Saturation Voltage (I_C = 2.5 A, I_B = 0.25 A)		$V_{BE\ (sat)}$			1.4	Vdc
(I_C = 4.0 A, I_B = 1.25 A)					1.6	
DYNAMIC CHARACTERISTICS						
Current-Gain – Bandwidth Product (I_C 200 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T		6		MHz
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Turn On Time	(I_C = 2.5 A, I_{B1} = 0.5 A) (I_{B2} = 1.0 A, V_{CC} = 250 V)	t_{on}			0.5	μs
Storage Time		t_s			3.5	μs
Fall Time		t_f		0.3		μs
Fall Time	(I_C = 2.5 A, I_{B1} = 0.5 A) (I_{B2} = 1.0 A, V_{CC} = 250 V, T_C = 100 °C)	t_f			1.0	μs

[1] Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

3

FIGURE 1 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 2 – "ON" VOLTAGES

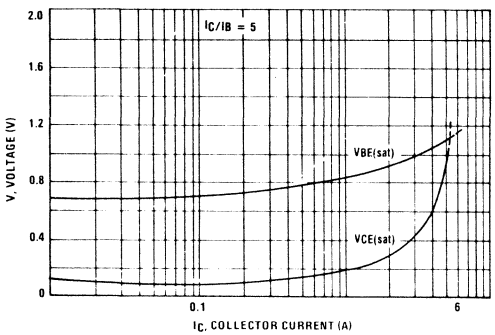


FIGURE 3 – DC CURRENT GAIN

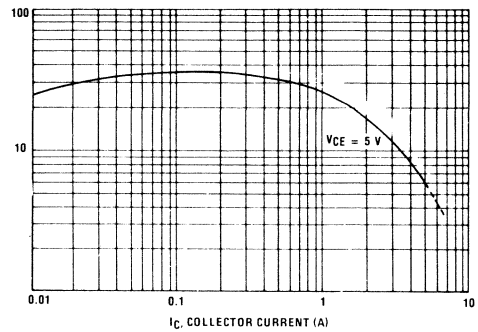


FIGURE 4 – RESISTIVE SWITCHING PERFORMANCE

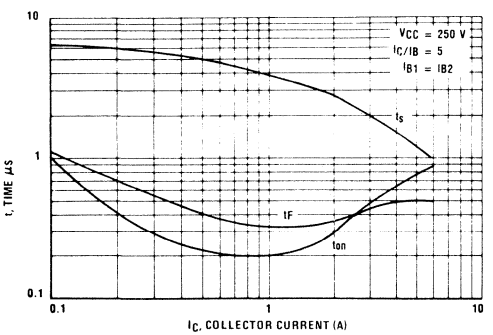
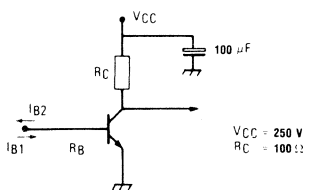


FIGURE 5 – SWITCHING TIMES TEST CIRCUIT



R_C – R_B: Non inductive resistances

BU 406
BU 407

HIGH VOLTAGE NPN SILICON TRANSISTOR

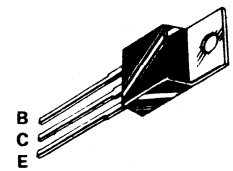
. . . designed for use in the switched mode power supply and television horizontal deflection.

- High Collector-Emitter Voltage
  V_{CES} = 400 V, 330 V
- Collector Current
  I_C = 7 Adc
- Low Collector Emitter Saturation Voltage
  $V_{CE(sat)}$ = 1 Vdc, @ I_C = 5 A, I_B = 0.5 A
- Fall Time @ I_C = 5 A, $I_{B\ (end)}$ = 0.5 A, V_{CC} = 40 V
  t_f = 0.75 μs (max.)
- TO–66 lead form also available ordered with "–66" suffix

7 AMPERES

NPN SILICON POWER TRANSISTOR

200, 150 VOLTS
60 WATTS



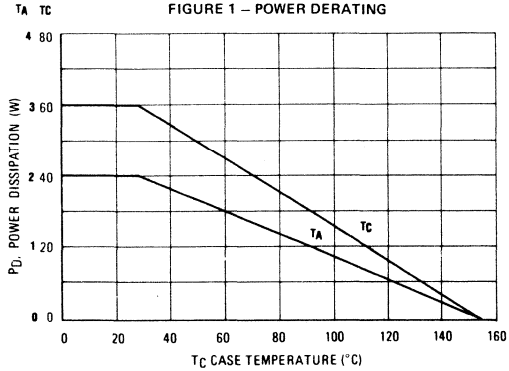
MAXIMUM RATINGS

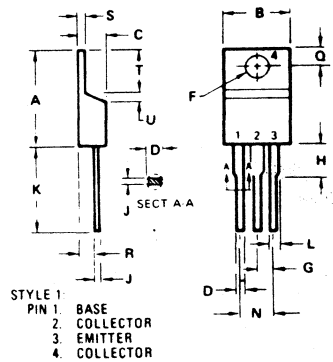
Rating	Symbol	BU406	BU407	Unit
Collector-Emitter Voltage	V_{CEO}	200	150	Vdc
Collector-Emitter Voltage V_{BE} = 0	V_{CES}	400	330	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current – Continuous – Peak	I_C	7.0 15.0		Adc
Base Current	I_B	4.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	60 0.48		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.08	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	°C/W

FIGURE 1 – POWER DERATING





STYLE 1
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 100 mA)	BU406	V_{CEO}	200		Vdc
	BU407		150		
Collector Cutoff Current		I_{CES}			mAdc
V_{CES} = 400 Vdc	BU406			5	
V_{CES} = 250 Vdc	BU406			0.1	
V_{CES} = 250 Vdc, Tc = 150°C	BU406			1	
V_{CES} = 330 Vdc	BU407			5	
V_{CES} = 200 Vdc	BU407			0.1	
V_{CES} = 200 Vdc, Tc = 150°C	BU407			1	
Emitter Cutoff Current (V_{EB} = 6 Vdc, I_C = 0)		I_{EBO}		1	mAdc
ON CHARACTERISTICS					
Collector-Emitter Saturation Voltage (I_C = 5 Adc, I_B = 0.5 Adc)		$V_{CE(sat)}$	–	1.0	Vdc
Base-Emitter Saturation Voltage (I_C = 5 Adc, I_B = 0.5 Adc)		$V_{BE(sat)}$	–	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	10		MHz

SWITCHING CHARACTERISTICS (Resistive Load)

Fall Time	(I_C = 5 Adc, I_{B1} = I_{B2} = 0.5 Adc, V_{CC} = 40 V)	t_f		0.75	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – DC CURRENT GAIN

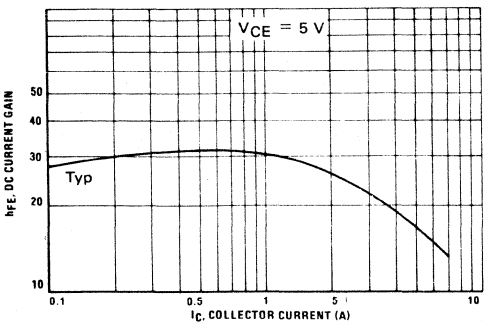


FIGURE 3 – COLLECTOR SATURATION REGION

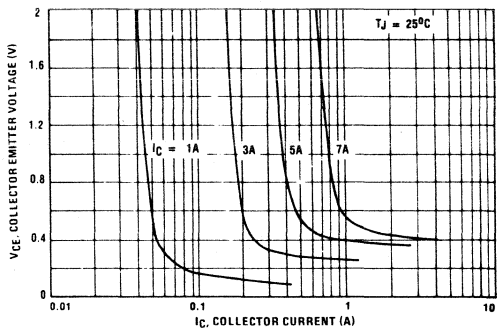


FIGURE 4 – "SATURATION" AND "ON" VOLTAGES

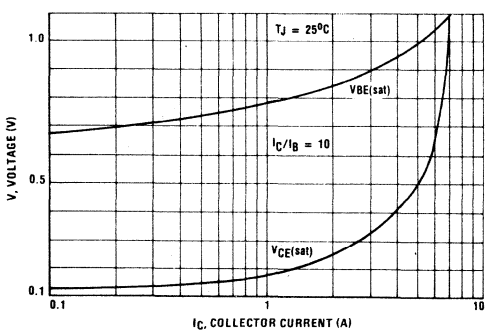
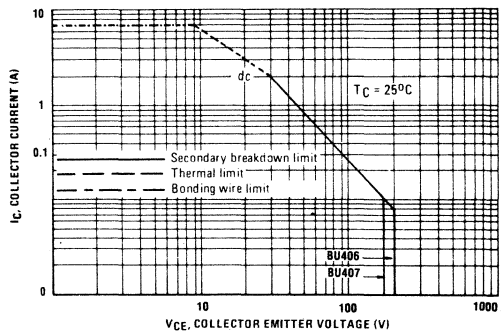


FIGURE 5 – FORWARD BIAS SAFE OPERATING AREA



3

FIGURE 7 – STORAGE TIME

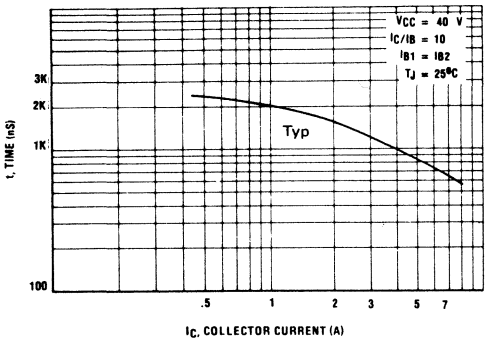
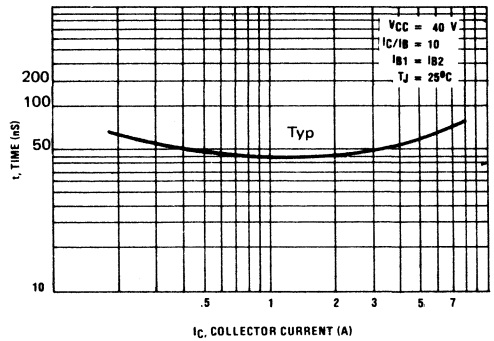


FIGURE 8 – FALL TIME



BU 426
BU 426A

HIGH VOLTAGE NPN SILICON TRANSISTOR

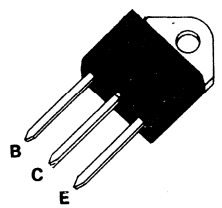
. . . designed for use in the switched mode power supply of 90° and 110° colour television receivers.

- High Collector-Emitter Voltage
  V_{CES} = 800 V, 900 V
- Collector Current
  I_C = 6 Adc
- Low Collector Emitter Saturation Voltage
  $V_{CE(sat)}$ = 3 Vdc, @ I_C = 4 A, I_B = 1.25 Adc
- Fall Time @ I_C = 2.5 A, $I_{B\,(end)}$ = 1 A
  t_f = 0,3 μsec (typ)

6 AMPERES

TRIPLE DIFFUSED NPN SILICON POWER TRANSISTORS

800, 900 VOLTS
113 WATTS

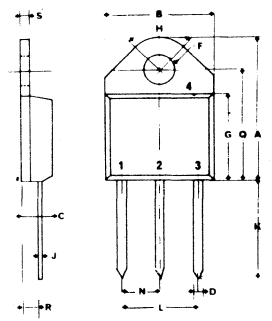


MAXIMUM RATINGS

Rating	Symbol	BU426	BU426A	Unit
Collector-Emitter Voltage	V_{CEO}	375	400	Vdc
Collector-Emitter Voltage V_{BE} = 0	V_{CES}	800	900	Vdc
Emitter-Base Voltage	V_{EB}	10		Vdc
Collector Current — Continuous — Peak	I_C	6 12		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	113 0.90		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.1	°C/W

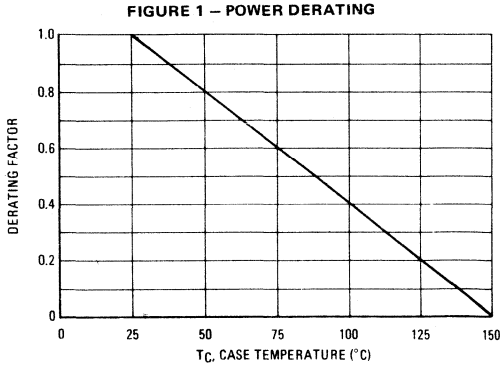


PIN 1: Base
PIN 2: Collector
PIN 3: Emitter
CASE (4): Collector

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.30	21.10	0.800	0.830
B	15.50	15.90	0.610	0.626
C	4.20	5.00	0.165	0.197
D	1.00	1.60	0.040	0.063
F	4.00	4.20	0.157	0.165
G	12.30	12.70	0.484	0.500
H	90° typ.		90° typ.	
J	0.45	0.70	0.018	0.028
K	12.7	15.5	0.500	0.610
L	10.65	11.15	0.420	0.440
N	5.20	5.70	0.205	0.225
Q	15.90	16.50	0.626	0.650
R	2.40	3.20	0.094	0.126
S	1.35	1.65	0.053	0.065

CASE 340

FIGURE 1 — POWER DERATING



ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage See Figure 8 (I_C = 100 mA, L = 25 mH)	BU426	V_{CEO}	375	–	–	Vdc
	BU426A		400	–	–	
Collector-Cutoff Current		I_{CES}				mAdc
(V_{CES} = Rated Value, T_C = 25°C)			–	–	1.0	
(V_{CES} = Rated Value, T_C = 125°C)			–	–	2.0	
Emitter Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)		I_{EBO}	–	–	10	mAdc
ON CHARACTERISTICS						
DC Current Gain (I_C = 0.6 Adc, V_{CE} = 5 Vdc)		h_{FE}		30	–	–
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 2.5 Adc, I_B = 0.5 Adc)			–	–	1.5	
(I_C = 4 Adc, I_B = 1.25 Adc)			–	–	3	
			–	–		
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 4 Adc, I_B = 1.25 Adc)			–	–	1.6	
(I_C = 2.5 Adc, I_B = 0.5 Adc)			–	–	1.4	
DYNAMIC CHARACTERISTICS						
Current Gain – Bandwidth Product (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T		6		MHz

SWITCHING CHARACTERISTICS (Resistive Load)

			MIN.	TYP.	MAX.	
Turn on Time	(I_C = 2.5 A, I_{B1} = 0.5 A) (I_{B2} = 1.0 A, V_{CC} = 250 V)	t_{on}		0.2	0.6	μs
Storage Time		t_s		2	3.5	
Fall Time		t_f		0.5		
Fall Time	(I_C = 2.5 A, I_{B1} = 0.5 A) (I_{B2} = 1.0 A, V_{CC} = 250 V, T_C = 95°C)	t_f			0.75	μs
		t_f				

FIGURE 2 – DC CURRENT GAIN

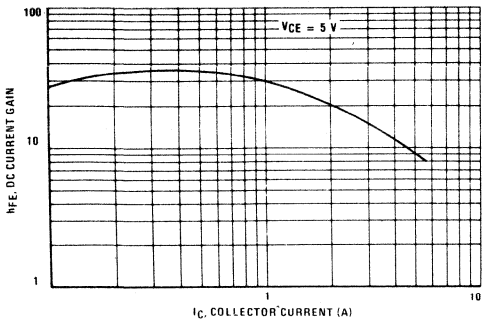


FIGURE 3 – "ON VOLTAGE"

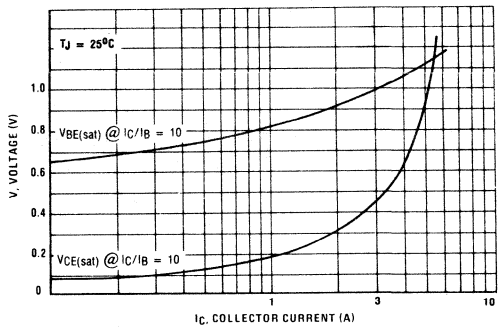


FIGURE 4 – TURN ON TIMES

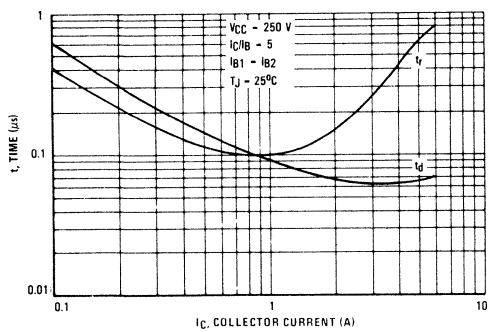


FIGURE 5 – TURN OFF TIMES

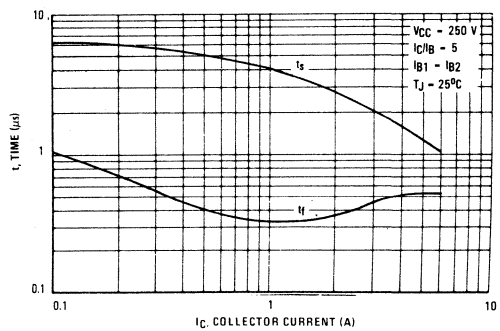
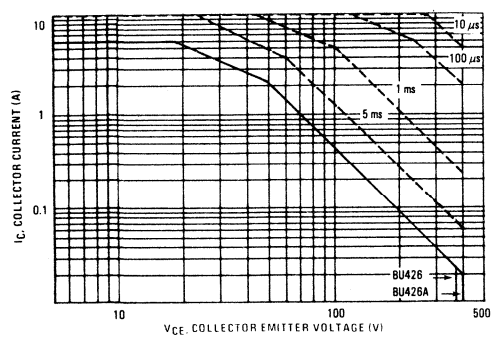


FIGURE 6 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 6 is based on $T_{J(pk)}$ 150°C, T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10° o provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in figure 7. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN 415A)

3

FIGURE 7 – THERMAL RESPONSE

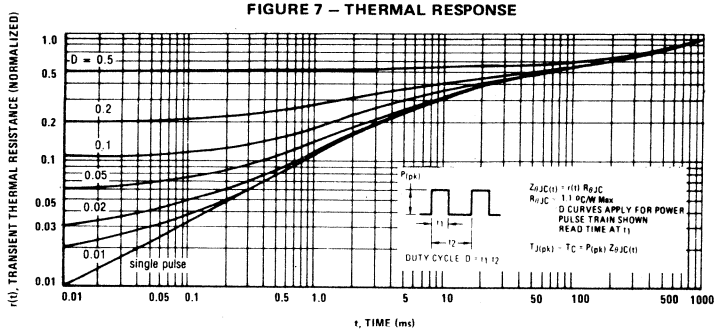
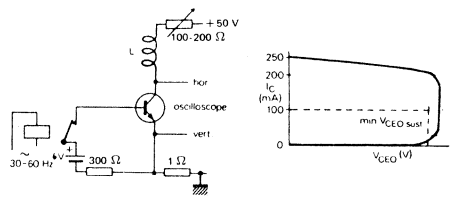


FIGURE 8 – SUSTAINING VOLTAGE TEST CIRCUIT



BU 522
BU 522A
BU 522B

HIGH VOLTAGE SILICON POWER DARLINGTONS

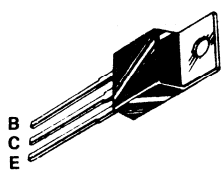
Power Transistor mainly intended for use as ignition circuit output transistor.

- Specified minimum sustaining voltage:
  $V_{CER(sus)}$ = 350 V (BU522)
  at I_C = 1 A 400 V (BU522A)
  425 V (BU522B)
- High S.O.A. capability:
  V_{CE} = 350 V (BU522) at I_C = 5 A
  400 V (BU522A, BU522B)
- Low $V_{CE(sat)}$ = 2.0 V max. at I_C = 4 A (BU522A, BU522B)

7 AMPERES

DARLINGTON TRIPLE DIFFUSED POWER TRANSISTORS NPN SILICON

375, 425, 450 VOLTS
75 WATTS



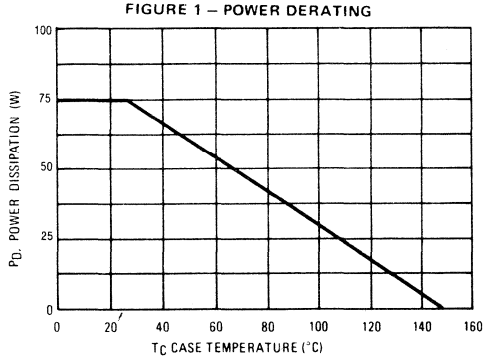
MAXIMUM RATINGS

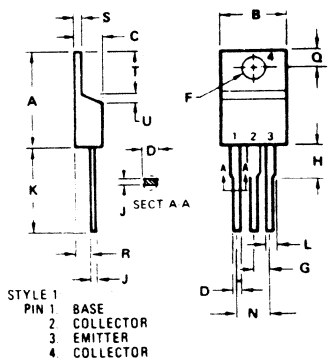
Rating	Symbol	BU522	BU522A	BU522B	Unit
Collector-Emitter Voltage Sust.	$V_{CER(sus)}$	350	400	425	Vdc
Collector-Emitter Voltage	V_{CER}	375	425	450	Vdc
Collector-Base Voltage	V_{CBO}	400	450	475	Vdc
Emitter-Base Voltage	V_{EBO}	5.0			Vdc
Collector Current - Continuous	I_C	7.0			Adc
Base Current	I_B	2.0			Adc
Total Device Dissipation @ T_C = 25°C	P_D	75			Watts
Derate above 25°C		0.60			W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.67	°C/W

FIGURE 1 – POWER DERATING





STYLE 1
PIN 1 BASE
2 COLLECTOR
3 EMITTER
4 COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

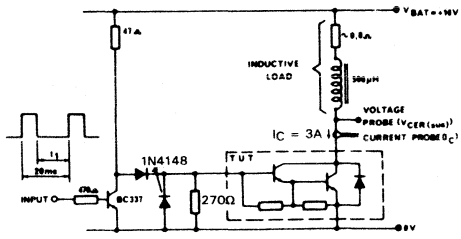
CASE 221A-02
TO-220AB

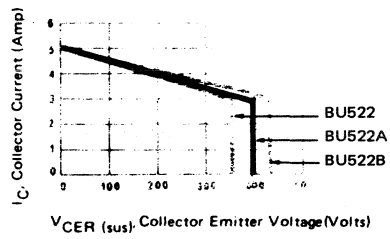
3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (See Figure 2) (I_C = 1.0 A) See Figure 2 BU522 / BU522A / BU522B	$V_{CER(sus)}$	350 / 400 / 425			Vdc
Collector Cutoff Current (Rated V_{CER}, R_{BE} = 270 Ω)	I_{CER}			1.0	mAdc
Collector Cutoff Current (Rated V_{CBO}, I_E = 0)	I_{CBO}			1.0	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}			40	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.5 Adc, V_{CE} = 5 Vdc)	h_{FE}	250			–
Collector-Emitter Saturation Voltage BU522 / BU522A, BU522B (I_C = 4 Adc, I_B = 80 mAdc)	$V_{CE(sat)}$			2.5 / 2	Vdc
Base-Emitter Saturation Voltage (I_C = 4 Adc, I_B = 80 mAdc)	$V_{BE(sat)}$			2.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (I_C = 0.3 mAdc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	f_T		7.5		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz	C_{ob}		150		pF

FIGURE 2 – SUSTAINING VOLTAGE TEST $V_{CER\ (sus)}$

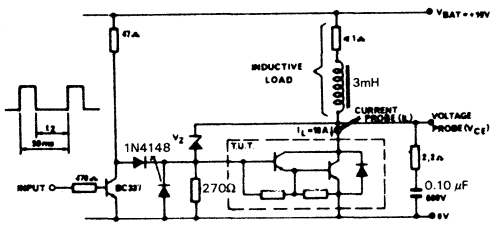




t_1 to be selected that I_C reaches 3 Adc before switch-off

Case temperature of the power transistor: T_C = 25°C

Test conditions of the Collector-Base Clamping Circuit:



Clamping device characteristics:

V_Z = 350 V (BU522) / 400 V (BU522A/B) ± 1% at I_Z = 20 mA

Clamping duration is around 45 μsec (BU522) / 40 μsec (BU522A/B)

t_2 to be selected that I_L reaches 5 Adc before switch-off

Case temperature of the power transistor: T_C = 25°C.

FIGURE 3 – S.O.A. TEST

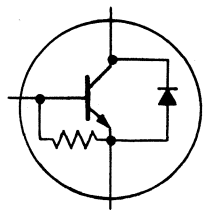
3

BU 800

NPN SILICON HORIZONTAL DEFLECTION TRANSISTOR WITH INTEGRATED DAMPER DIODE

. . . specifically designed for use in large screen color deflection circuits

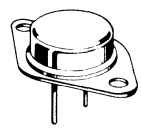
- V_{CES} = 1500 V
- $V_{CEO(sus)}$ = 700 V



5 AMPERES

NPN SILICON POWER TRANSISTOR

1500 VOLTS
60 WATTS



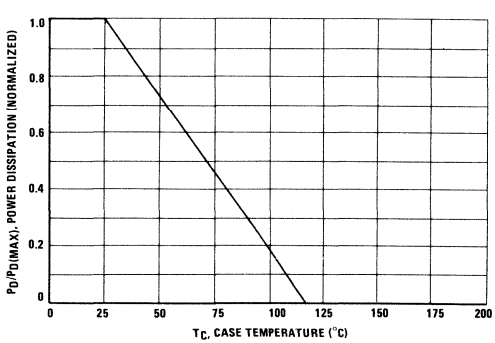
MAXIMUM RATINGS

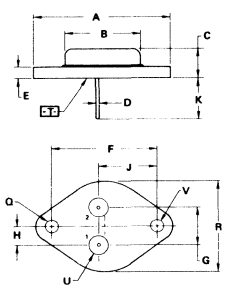
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	700	Vdc
Collector-Emitter Voltage ($R_{BE}=0$)	V_{CES}	1500	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Collector-Current — Continuous — Peak	I_C I_{CM}	5 10	Adc
Base Current — Peak	I_B	2.5	Adc
Total Device Dissipation $T_C=25°C$ Derate above 25°C	P_D	60 0.666	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 115	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.5	°C/W

FIGURE 1 – POWER DERATING





NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. [T] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q.
   ⌖ ⌀13 (0.005) M T V M
   FOR LEADS:
   ⌖ ⌀13 (0.005) M T V M Q M
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0, L = 25 mH, Vclamp = 800 V)	$V_{CEO(sus)}$	700		Vdc
Collector Cutoff Current (V_{CES} = 1500 Vdc, R_{BE} = 0)	I_{CES}		1.0	mAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}		300	mAdc
ON CHARACTERISTICS				
Diode Forward Voltage (I_F = 4 A)	V_F		2.0	Vdc
Collector-Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 2.0 Adc)	$V_{CE(sat)}$		1.0	Vdc
Base-Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 2.0 Adc)	$V_{BE(sat)}$		1.5	Vdc

SWITCHING CHARACTERISTICS (Resistive Load)

Fall Time	I_C end = 4.5 A, V_{CC} = 140 V I_B end = 1.8 A, L_C = 0.9 mH, L_B = 10 μH	t_f	–	0.6 (typ)	μs

3

MJ802 (SILICON)

HIGH-POWER NPN SILICON TRANSISTOR

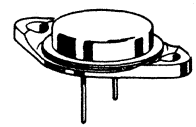
. . . for use as an output device in complementary audio amplifiers to 100-Watts music power per channel.

- High DC Current Gain – h_{FE} = 25-100 @ I_C = 7.5 A
- Excellent Safe Operating Area
- Complement to the PNP MJ4502

30 AMPERE
POWER TRANSISTOR

NPN SILICON

100 VOLTS
200 WATTS



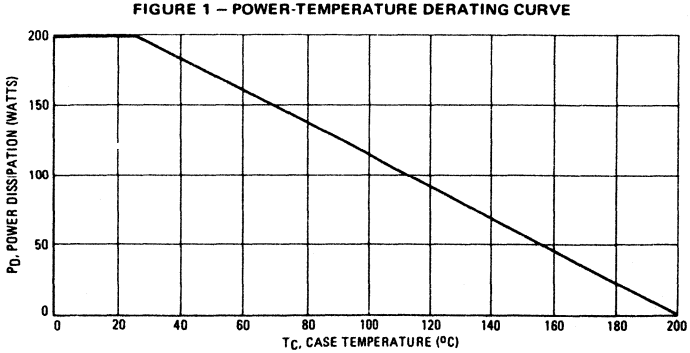
MAXIMUM RATINGS

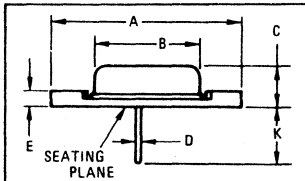
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CER}	100	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Collector-Emitter Voltage	V_{CEO}	90	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	30	Adc
Base Current	I_B	7.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

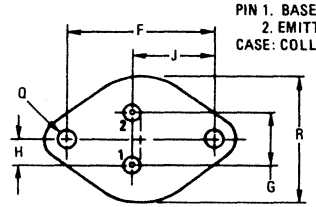
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

NOTE:
1. DIM "Q" IS DIA.

CASE 11-01
TO-3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 200 mAdc, R_{BE} = 100 Ohms)	BV_{CER}	100	–	Vdc
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc)	$V_{CEO(sus)}$	90	–	Vdc
Collector-Base Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	–	1.0	mAdc
(V_{CB} = 100 Vdc, I_E = 0, T_C = 150°C)		–	5.0	
Emitter-Base Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (1) (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	25	100	–
Base-Emitter "On" Voltage (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	–	1.3	Vdc
Collector-Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{CE(sat)}$	–	0.8	Vdc
Base-Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{BE(sat)}$	–	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.0	–	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – DC CURRENT GAIN

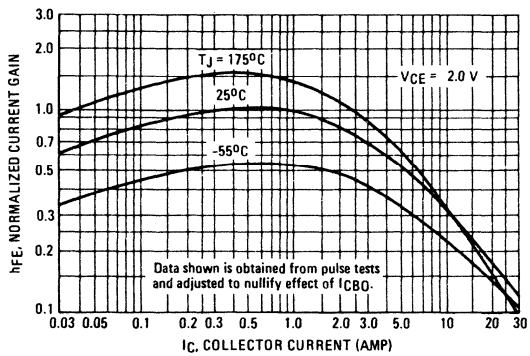


FIGURE 3 – "ON" VOLTAGES

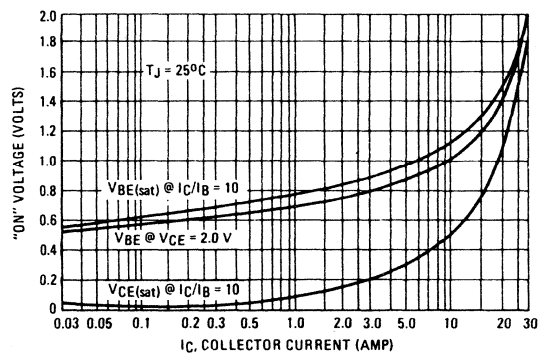
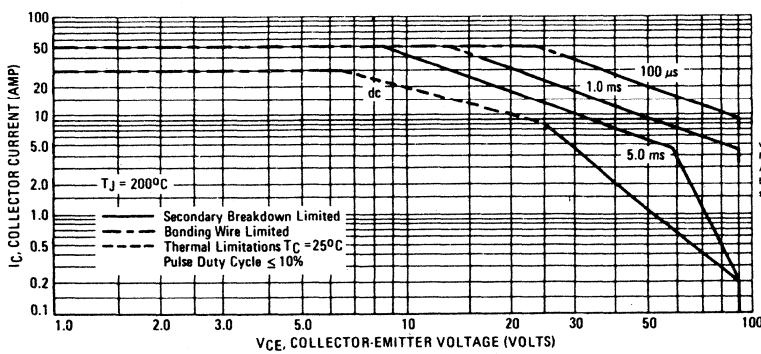


FIGURE 4 – ACTIVE REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C – V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

MJ900, MJ901 PNP (SILICON)
MJ1000, MJ1001 NPN

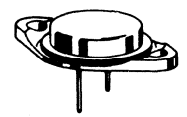
MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain — h_{FE} = 6000 (Typ) @ I_C = 3.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

8.0 AMPERE DARLINGTON POWER TRANSISTORS COMPLEMENTARY SILICON

60-80 VOLTS
90 WATTS



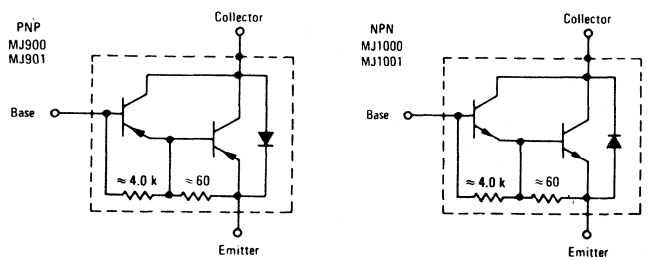
MAXIMUM RATINGS

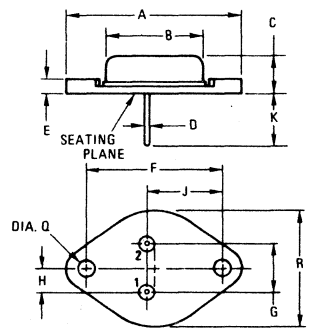
Rating	Symbol	MJ900 MJ1000	MJ901 MJ1001	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	8.0		Adc
Base Current	I_B	0.1		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	90 0.515		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.94	°C/W

FIGURE 1 – DARLINGTON CIRCUIT SCHEMATIC





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
(TO-3)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1)		BV_{CEO}			Vdc
(I_C = 100 mAdc, I_B = 0)	MJ900, MJ1000		60	–	
	MJ901, MJ1001		80	–	
Collector Emitter Leakage Current		I_{CER}			mAdc
(V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm)	MJ900, MJ1000		–	1.0	
(V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm)	MJ901, MJ1001		–	1.0	
(V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ900, MJ1000		–	5.0	
(V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ901, MJ1001		–	5.0	
Emitter Cutoff Current		I_{EBO}	–	2.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
Collector-Emitter Leakage Current		I_{CEO}			μAdc
(V_{CE} = 30 Vdc, I_B = 0)	MJ900, MJ1000		–	500	
(V_{CE} = 40 Vdc, I_B = 0)	MJ901, MJ1001		–	500	
ON CHARACTERISTICS					
DC Current Gain(1)		h_{FE}			–
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)			1000	–	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			750	–	
Collector-Emitter Saturation Voltage(1)		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 12 mAdc)			–	2.0	
(I_C = 8.0 Adc, I_B = 40 mAdc)			–	4.0	
Base-Emitter Voltage(1)		V_{BE}	–	2.5	Vdc
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)					

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – DC CURRENT GAIN

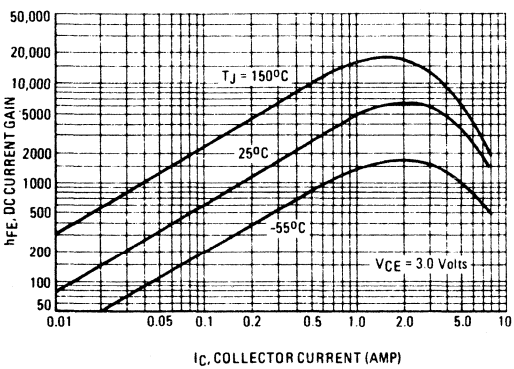


FIGURE 3 – SMALL-SIGNAL CURRENT GAIN

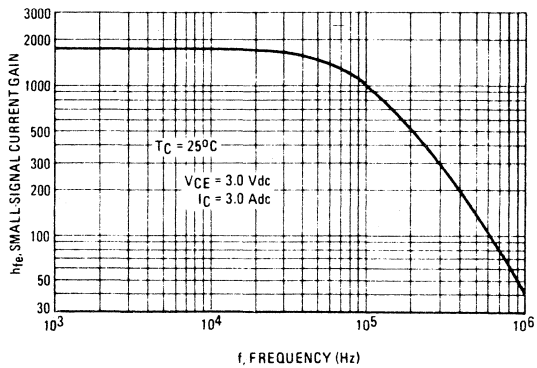


FIGURE 4 – "ON" VOLTAGES

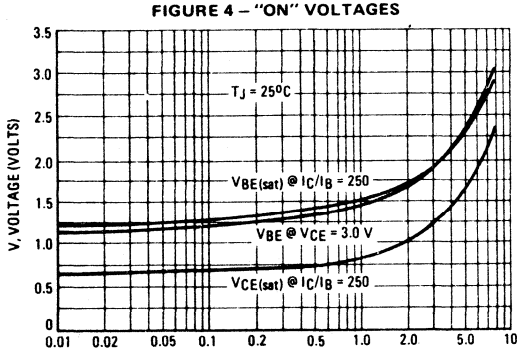
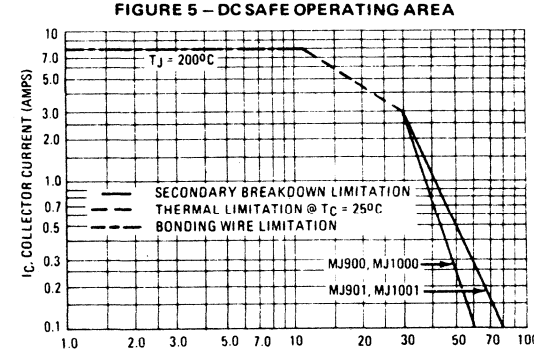


FIGURE 5 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

MJ2500, MJ2501 PNP (SILICON)
MJ3000, MJ3001 NPN

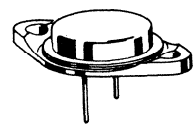
MEDIUM-POWER COMPLEMENTARY
SILICON TRANSISTORS

. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain – h_{FE} = 4000 (Typ) @ I_C = 5.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

10 AMPERE
DARLINGTON
POWER TRANSISTORS
COMPLEMENTARY SILICON

60-80 VOLTS
150 WATTS



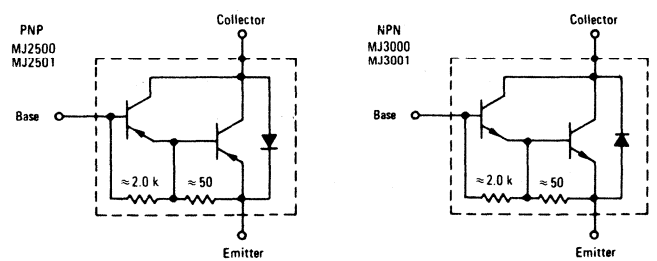
MAXIMUM RATINGS

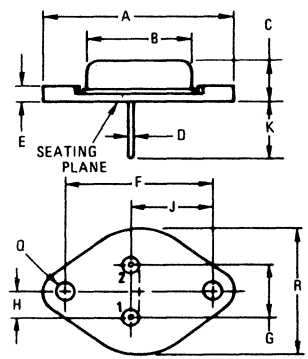
Rating	Symbol	MJ2500 MJ3000	MJ2501 MJ3001	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	10		Adc
Base Current	I_B	0.2		Adc
Total Device Dissipation @ T_C = 25°C	P_D	150		Watts
Derate above 25°C		0.857		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

FIGURE 1 – DARLINGTON CIRCUIT SCHEMATIC





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-01
TO-3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 100 mAdc, I_B = 0)	MJ2500, MJ3000	BV_{CEO}	60	–	Vdc
	MJ2501, MJ3001		80	–	
Collector Emitter Leakage Current		I_{CER}			mAdc
(V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm)	MJ2500, MJ3000		–	1.0	
(V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm)	MJ2501, MJ3001		–	1.0	
(V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ2500, MJ3000		–	5.0	
(V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ2501, MJ3001		–	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
Collector-Emitter Leakage Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	MJ2500, MJ3000		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	MJ2501, MJ3001		–	1.0	
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	1000	–	–
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 20 mAdc)			–	2.0	
(I_C = 10 Adc, I_B = 50 mAdc)			–	4.0	
Base-Emitter Voltage (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)		V_{BE}	–	3.0	Vdc

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – DC CURRENT GAIN

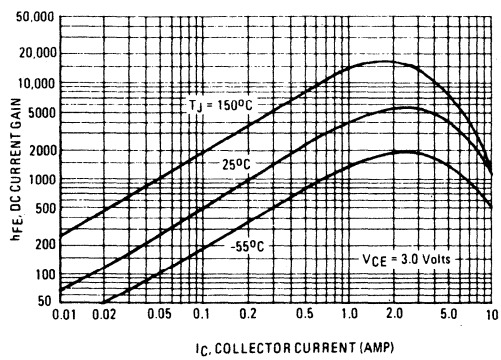


FIGURE 3 – SMALL-SIGNAL CURRENT GAIN

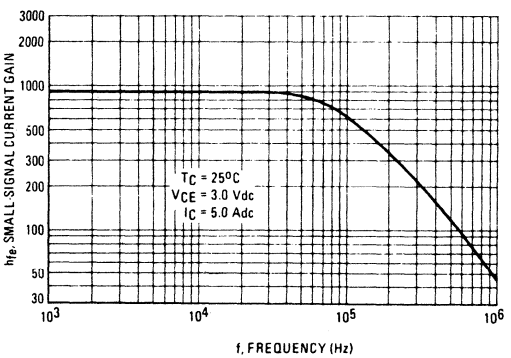


FIGURE 4 – "ON" VOLTAGES

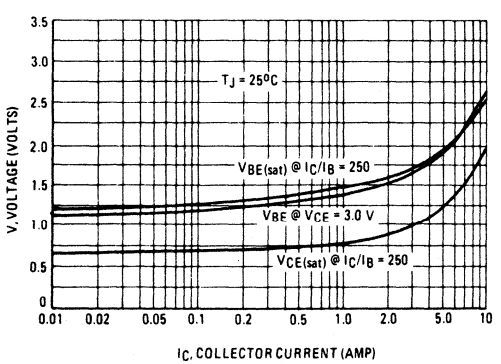
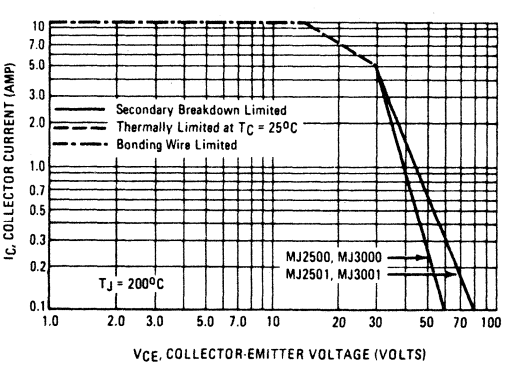


FIGURE 5 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

NPN 2N3055 PNP MJ2955

COMPLEMENTARY SILICON POWER TRANSISTORS

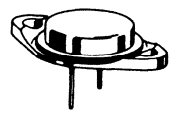
. . . designed for general-purpose switching and amplifier applications.

- DC Current Gain – h_{FE} = 20-70 @ I_C = 4 Adc
- Collector-Emitter Saturation Voltage – $V_{CE(sat)}$ = 1.1 Vdc (Max) @ I_C = 4 Adc
- Excellent Safe Operating Area

15 AMPERE
POWER TRANSISTORS

COMPLEMENTARY SILICON

60 VOLTS
115 WATTS



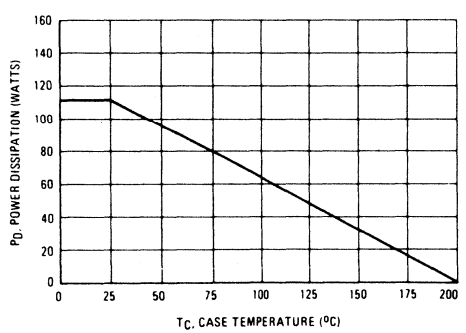
MAXIMUM RATINGS

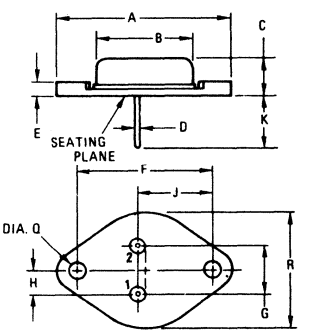
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Emitter Voltage	V_{CER}	70	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	7	Vdc
Collector Current – Continuous	I_C	15	Adc
Base Current	I_B	7	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	115 0.657	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.52	°C/W

FIGURE 1 – POWER DERATING





NOTE:
1. DIM "Q" IS DIA.

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
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J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
(TO-3)

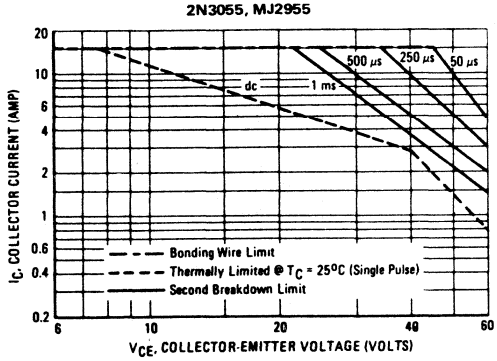
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**				
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	–	Vdc
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, R_{BE} = 100 Ohms)	$V_{CER(sus)}$	70	–	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	–	0.7	mAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	– –	1.0 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	–	5.0	mAdc
***ON CHARACTERISTICS (1)**				
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	20 5.0	70 –	–
Collector-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 400 mAdc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	–	1.1 3.0	Vdc
Base-Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	1.5	Vdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 1.0 s; Nonrepetitive)	$I_{s/b}$	2.87	–	Adc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.5	–	MHz
*Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	h_{fe}	15	120	–
*Small-Signal Current Gain Cutoff Frequency (V_{CE} = 4.0 Vdc, I_C = 1.0 Adc, f = 1.0 kHz)	f_{hfe}	10	–	kHz

* Indicates Within JEDEC Registration. (2N3055)

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 1.

NPN
2N3055

PNP
MJ2955

FIGURE 3 – DC CURRENT GAIN

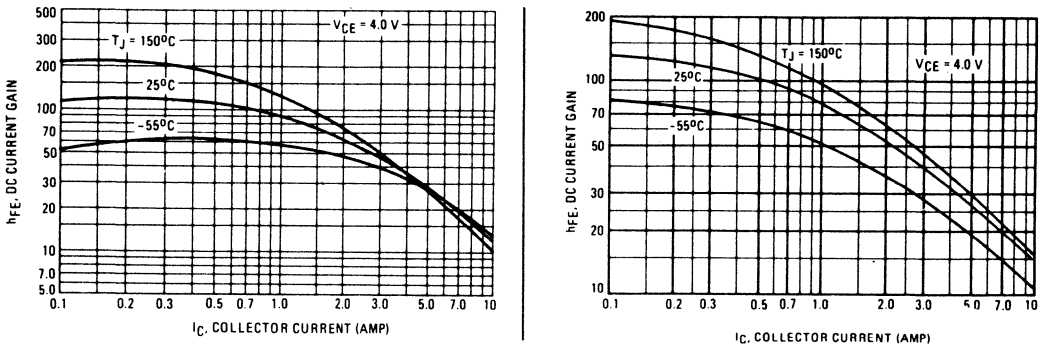


FIGURE 4 – COLLECTOR SATURATION REGION

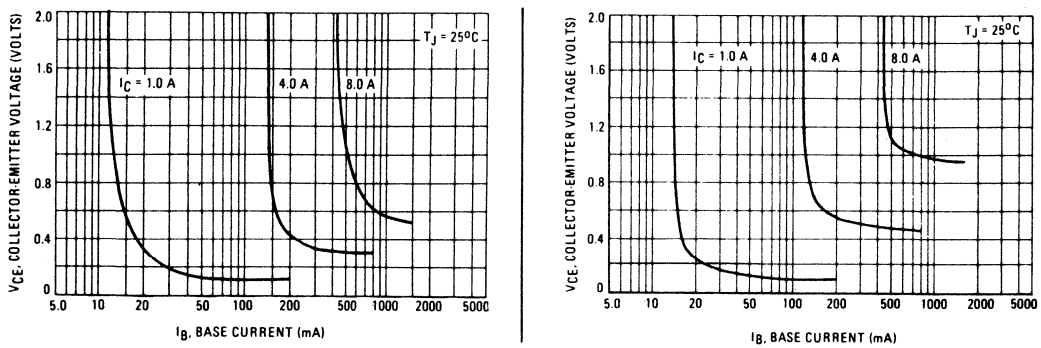


FIGURE 5 – "ON" VOLTAGES

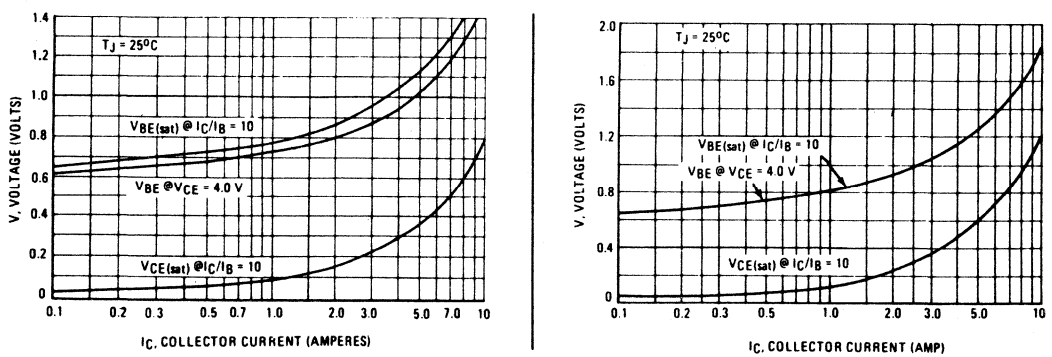
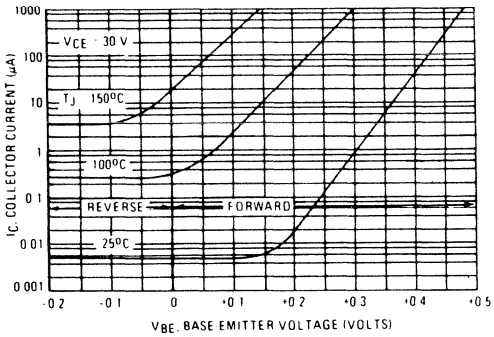


FIGURE 6 – COLLECTOR CUTOFF REGION

NPN – 2N3055



PNP – MJ2955

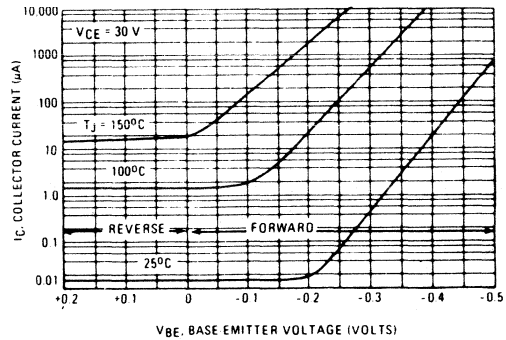


FIGURE 7 – SWITCHING TIMES TEST CIRCUIT

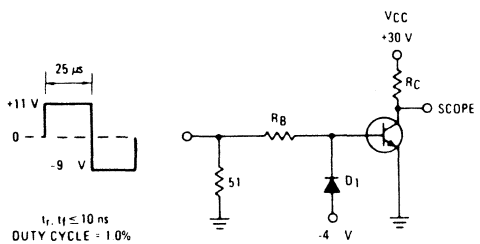


FIGURE 8 – TURN-ON TIME

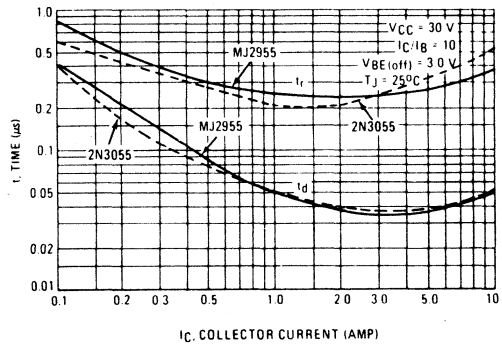


FIGURE 9 – TURN-OFF TIME

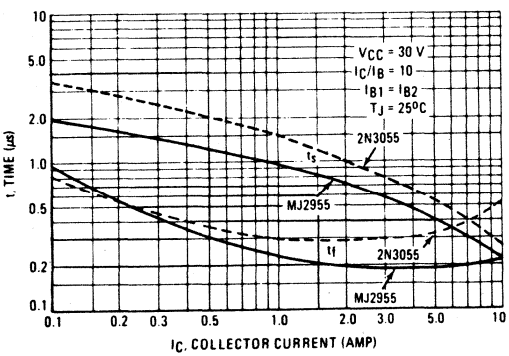
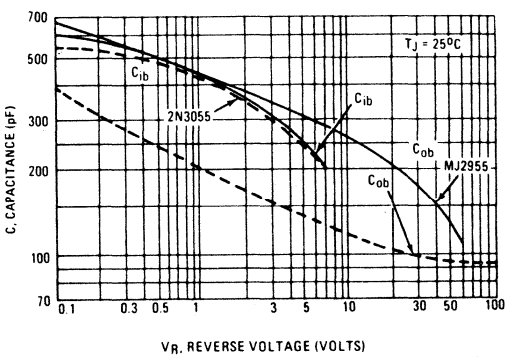


FIGURE 10 – CAPACITANCE



3

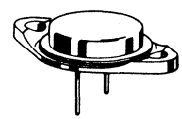
MJ4030, MJ4031, MJ4032 PNP (SILICON)
MJ4033, MJ4034, MJ4035 NPN

MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain – h_{FE} = 3500 (Typ) @ I_C = 10 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistor

16 AMPERE
DARLINGTON POWER TRANSISTORS COMPLEMENTARY SILICON
60–100 VOLTS
150 WATTS



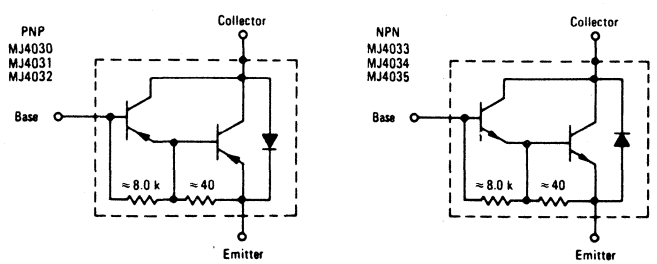
MAXIMUM RATINGS

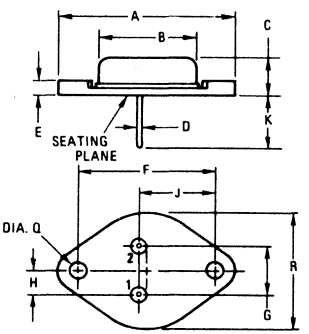
Rating	Symbol	MJ4030 MJ4033	MJ4031 MJ4034	MJ4032 MJ4035	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current	I_C	16			Adc
Base Current	I_B	0.5			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.857			Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-55 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

FIGURE 1 – DARLINGTON CIRCUIT SCHEMATIC





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
(TO-3)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 100 mAdc, I_B = 0)	MJ4030, MJ4033	BV_{CEO}	60		Vdc
	MJ4031, MJ4034		80	–	
	MJ4032, MJ4035		100	–	
Collector Emitter Leakage Current		I_{CER}			mAdc
(V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm)	MJ4030, MJ4033		–	1.0	
(V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm)	MJ4031, MJ4034		–	1.0	
(V_{CB} = 100 Vdc, R_{BE} = 1.0 k ohm)	MJ4032, MJ4035		–	1.0	
(V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ4030, MJ4033		–	5.0	
(V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ4031, MJ4034		–	5.0	
(V_{CB} = 100 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ4032, MJ4035		–	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	5.0	mAdc
Collector-Emitter Leakage Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	MJ4030, MJ4033		–	3.0	
(V_{CE} = 40 Vdc, I_B = 0)	MJ4031, MJ4034		–	3.0	
(V_{CE} = 50 Vdc, I_B = 0)	MJ4032, MJ4035		–	3.0	
ON CHARACTERISTICS(1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	1000		–
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 40 mAdc)			–	2.5	
(I_C = 16 Adc, I_B = 80 mAdc)			–	4.0	
Base-Emitter Voltage (I_C = 10 Adc, V_{CE} = 3.0 Vdc)		V_{BE}	–	3.0	Vdc

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

FIGURE 2 – DC CURRENT GAIN

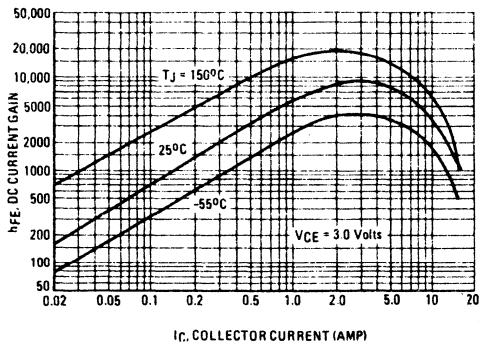


FIGURE 3 – SMALL-SIGNAL CURRENT GAIN

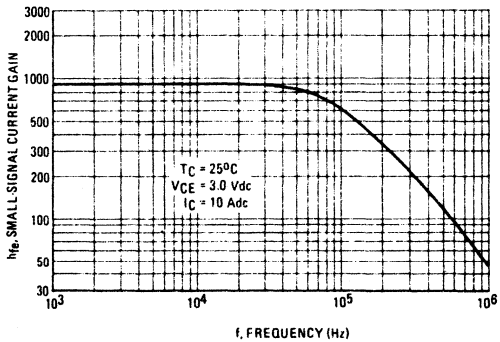


FIGURE 4 – "ON" VOLTAGES

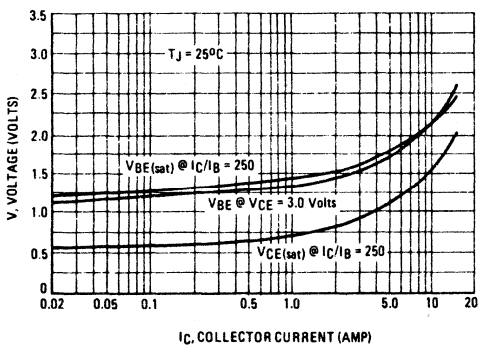
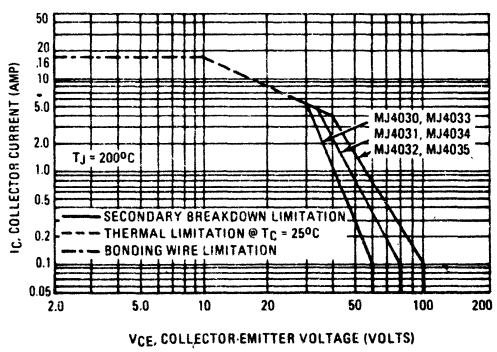


FIGURE 5 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

MJ8500
MJ8501

Designers▲ Data Sheet

SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTORS

The MJ8500 and MJ8501 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times
- 300 ns Inductive Fall Time – 25°C (Typ)
- 500 ns Inductive Crossover Time – 25°C (Typ)
- 900 ns Inductive Storage Time – 25°C (Typ)

Operating Temperature Range –65 to +200°C

100°C Performance Specified for:
- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

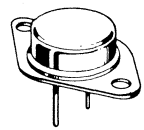
2.5 AMPERE

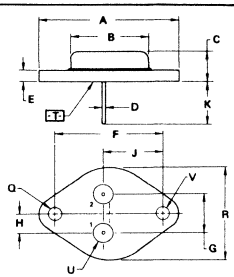
NPN SILICON POWER TRANSISTORS

700 and 800 VOLTS
125 WATTS

Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.





NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. T IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ ⌀.13 (0.005) M T V M
   FOR LEADS:
   ⌖ ⌀.13 (0.005) M T V M Q M
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

MAXIMUM RATINGS

Rating	Symbol	MJ8500	MJ8501	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	700	800	Vdc
Collector-Emitter Voltage	V_{CEV}	1200	1400	Vdc
Emitter Base Voltage	V_{EB}	8.0	8.0	Vdc
Collector Current – Continuous Peak (1)	I_C I_{CM}	2.5 5.0	2.5 5.0	Adc
Base Current – Continuous Peak (1)	I_B I_{BM}	2.0 4.0	2.0 4.0	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	125 71 0.71	125 71 0.71	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	MJ8500 MJ8501	$V_{CEO(sus)}$	700 800	– –	– –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEV}	– –	– –	0.25 5.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	–	–	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	–	1.0	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 13			
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	7.5	–	–	–
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.33 Adc) (I_C = 2.5 Adc, I_B = 1.0 Adc) (I_C = 1.0 Adc, I_B = 0.33 Adc, T_C = 100°C)		$V_{CE(sat)}$	– – –	– – –	2.0 5.0 3.0	Vdc
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.33 Adc) (I_C = 1.0 Adc, I_B = 0.33 Adc, TC = 100°C)		$V_{BE(sat)}$	– –	– –	1.5 1.5	Vdc
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	50	–	250	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 500 Vdc, I_C = 1.0 A, I_{B1} = 0.33 A, $V_{BE(off)}$ = 5.0 Vdc, t_p = 50 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.045	0.20	μs
Rise Time		t_r	–	0.2	2.0	μs
Storage Time		t_s	–	1.0	4.0	μs
Fall Time		t_f	–	0.5	2.0	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 1.0 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 0.33 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	–	1.3	4.0	μs
Crossover Time		t_c	–	0.6	2.0	μs
Storage Time	(I_C = 1.0 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 0.33 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	–	0.9	–	μs
Crossover Time		t_c	–	0.5	–	μs
Fall Time		t_{fi}	–	0.3	–	μs

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤ 2%.

FIGURE 1 – DC CURRENT GAIN

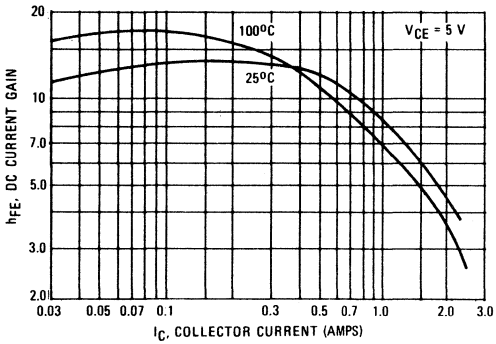


FIGURE 2 – COLLECTOR SATURATION REGION

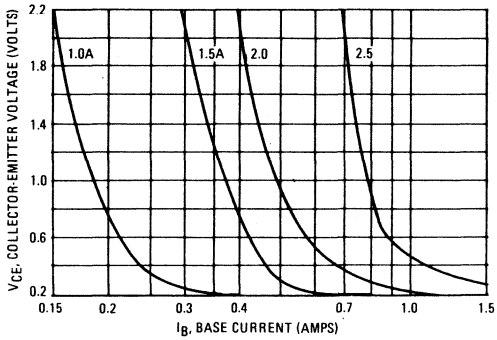


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

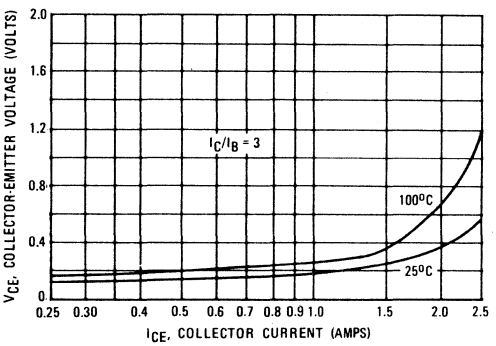


FIGURE 4 – BASE-EMITTER VOLTAGE

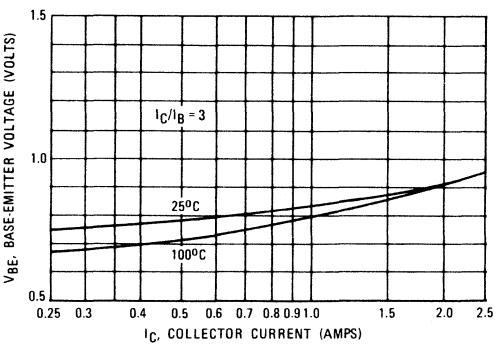


FIGURE 5 – COLLECTOR CUTOFF REGION

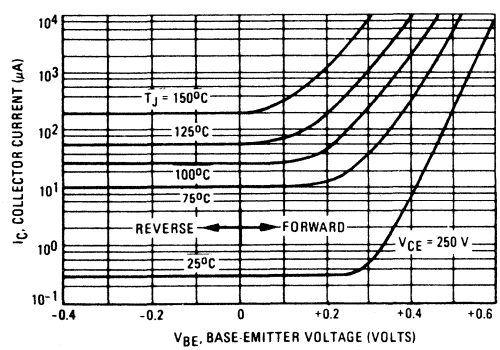


FIGURE 6 – CAPACITANCE

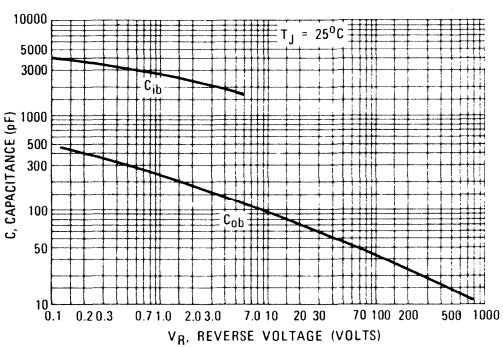


FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

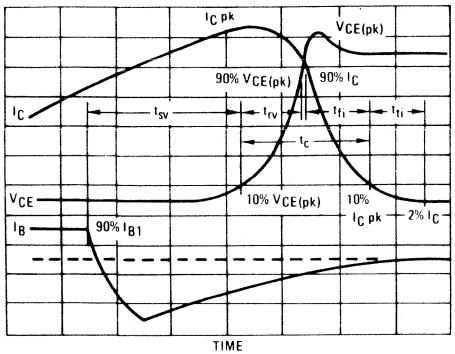
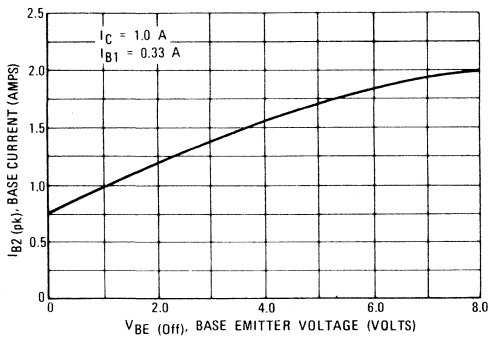


FIGURE 8 – PEAK REVERSE BASE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CE} (pk)
t_{rv} = Voltage Rise Time, 10–90% V_{CE} (pk)
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{CE} (pk) to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 – TURN - ON SWITCHING TIMES

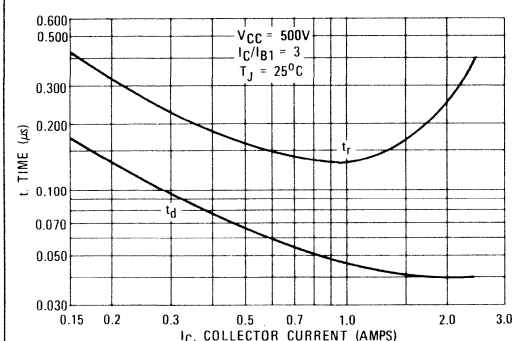


FIGURE 10 – TURN - OFF SWITCHING TIMES

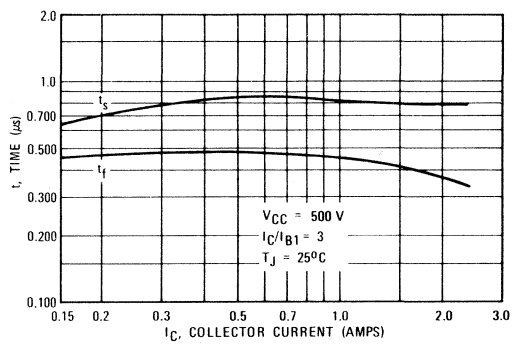


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TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

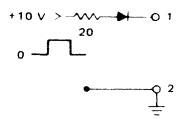
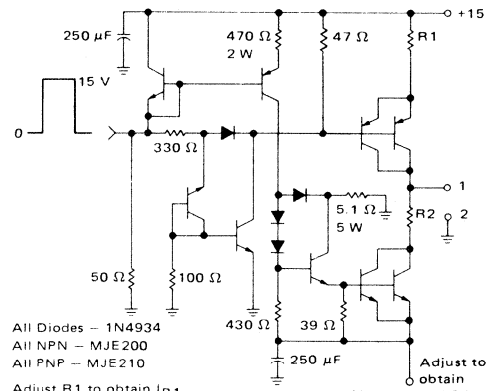
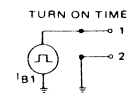
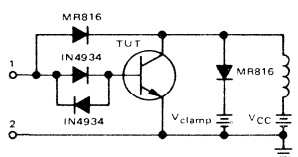
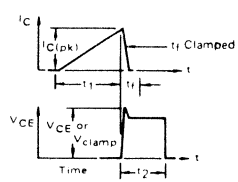
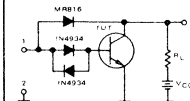
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 All Diodes – 1N4934 All NPN – MJE200 All PNP – MJE210 Adjust R1 to obtain I_{B1} For switching and RB_{SOA}, R2 = 0 For $BV_{CEO(sus)}$, R2 = ∞	 I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 500 V	V_{CC} = 500 V R_L = 500 Ω Pulse Width = 10 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS 	t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 11 – THERMAL RESPONSE

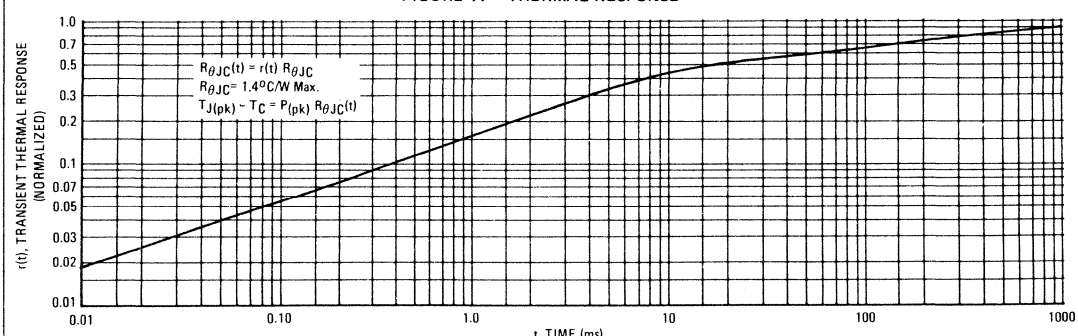


FIGURE 12 – MAXIMUM FORWARD BIAS SAFE OPERATING AREA

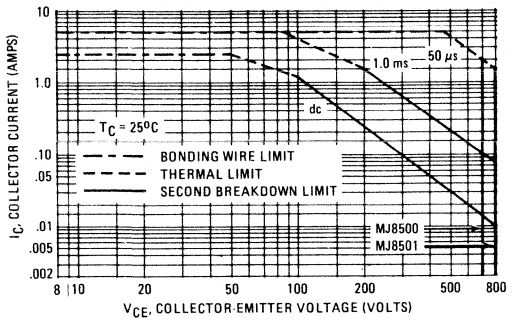
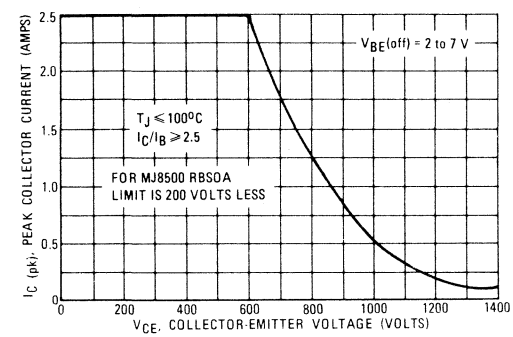


FIGURE 13 – RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

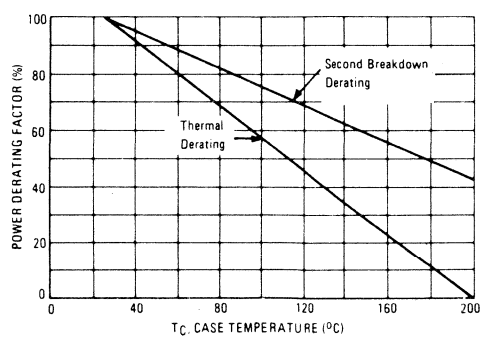
The data of Figure 12 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

FIGURE 14 – POWER DERATING



3

MJ8502
MJ8503

Designers▲ Data Sheet

SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTORS

The MJ8502 and MJ8503 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times

150 ns Inductive Fall Time–25°C (Typ)

400 ns Inductive Crossover Time–25°C (Typ)

1200 ns Inductive Storage Time–25°C (Typ)

Operating Temperature Range –65 to + 200°C

100°C Performance Specified for:

Reverse-Biased SOA with Inductive Loads

Switching Times with Inductive Loads

Saturation Voltages

Leakage Currents

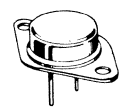
5.0 AMPERE

NPN SILICON POWER TRANSISTORS

700 and 800 VOLTS
150 WATTS

Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



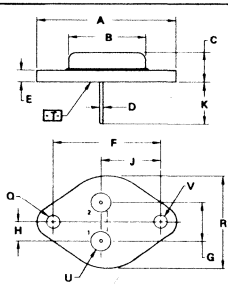
MAXIMUM RATINGS

Rating	Symbol	MJ8502	MJ8503	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	700	800	Vdc
Collector-Emitter Voltage	V_{CEV}	1200	1400	Vdc
Emitter Base Voltage	V_{EB}	8.0	8.0	Vdc
Collector Current – Continuous Peak (1)	I_C I_{CM}	5.0 10	5.0 10	Adc
Base Current – Continuous Peak (1)	I_B I_{BM}	4.0 8.0	4.0 8.0	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	150 86 0.85	150 86 0.85	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.16	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. T IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ⌀.13 (0.005) M | T | V M
   FOR LEADS:
   ⌖ | ⌀.13 (0.005) M T | V M | Q M
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	MJ8502	$V_{CEO(sus)}$	700	–	–	Vdc
	MJ8503		800	–	–	
Collector Cutoff Current		I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	–	0.25	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			–	–	5.0	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	–	–	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	–	1.0	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 13			
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	7.5	–	–	–
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 2.5 Adc, I_B = 1.0 Adc)			–	–	2.0	
(I_C = 5.0 Adc, I_B = 2.0 Adc)			–	–	5.0	
(I_C = 2.5 Adc, I_B = 1.0 Adc, T_C = 100°C)			–	–	3.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 2.5 Adc, I_B = 1.0 Adc)			–	–	1.5	
(I_C = 2.5 Adc, I_B = 1.0 Adc, T_C = 100°C)			–	–	1.5	
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	60	–	300	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 500 Adc, IC = 2.5 A, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5.0 Vdc, t_p = 50 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.040	0.20	μs
Rise Time		t_r	–	0.125	2.0	μs
Storage Time		t_s	–	1.2	4.0	μs
Fall Time		t_f	–	0.65	2.0	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 2.5 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, TC = 100°C)	t_{sv}	–	1.6	5.0	μs
Crossover Time		t_c	–	0.60	2.0	μs
Storage Time	(I_C = 2.5 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	–	1.2	–	μs
Crossover Time		t_c	–	0.4	–	μs
Fall Time		t_{fi}	–	0.15	–	μs

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤ 2%.

3

FIGURE 1 – DC CURRENT GAIN

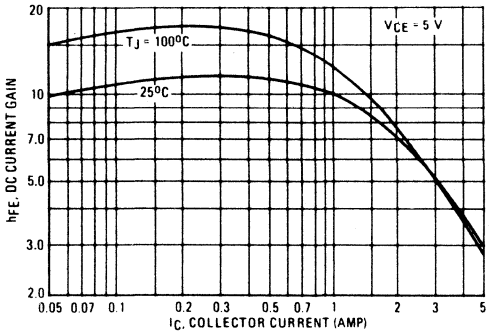


FIGURE 2 – COLLECTOR SATURATION REGION

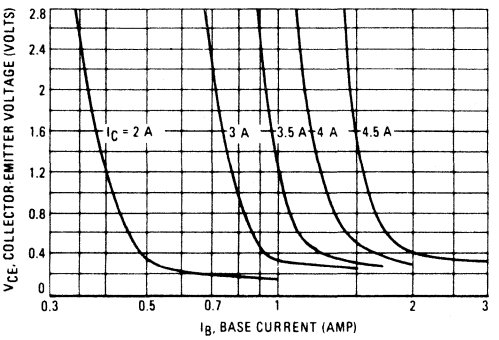


FIGURE 3 – COLLECTOR -EMITTER SATURATION REGION

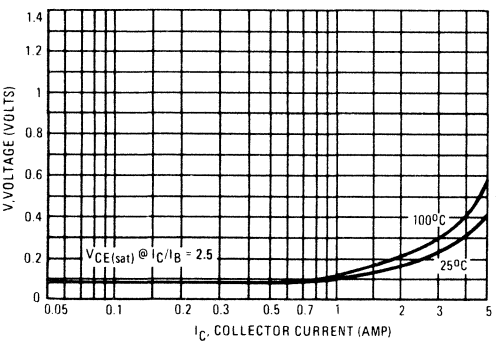


FIGURE 4 – BASE-EMITTER VOLTAGE

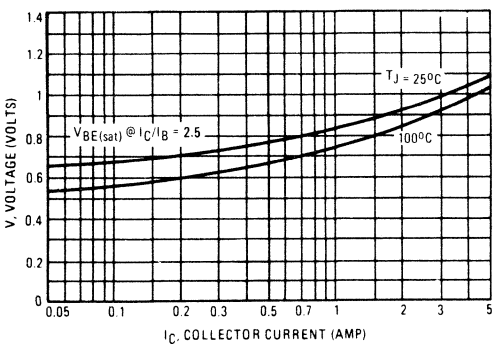


FIGURE 5 – COLLECTOR CUTOFF REGION

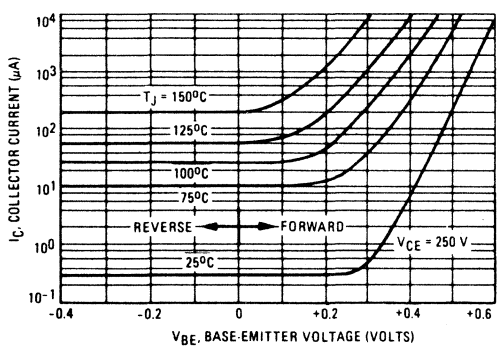


FIGURE 6 – CAPACITANCE

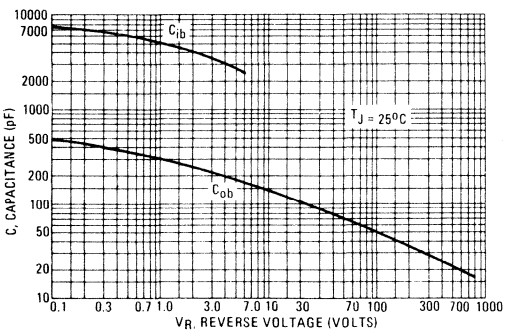


FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

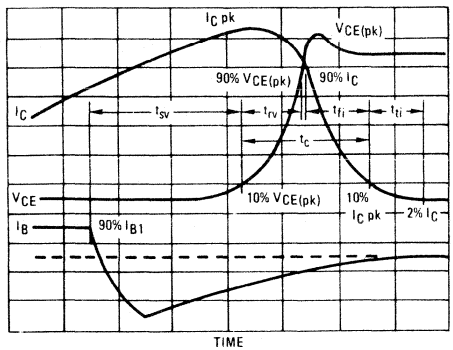
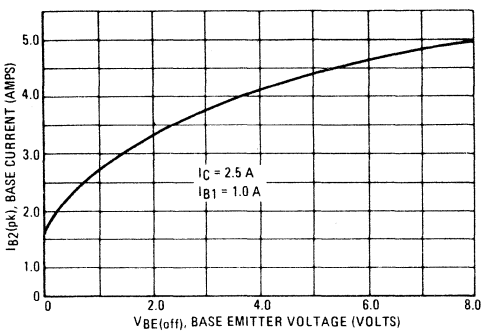


FIGURE 8 – PEAK REVERSE BASE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% $V_{CE(pk)}$
t_{rv} = Voltage Rise Time, 10–90% $V_{CE(pk)}$
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% $V_{CE(pk)}$ to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 – TURN-ON SWITCHING TIMES

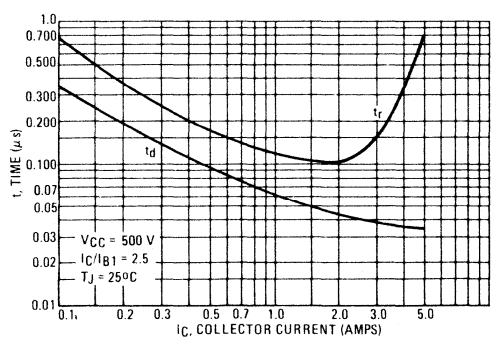


FIGURE 10 – TURN-OFF SWITCHING TIMES

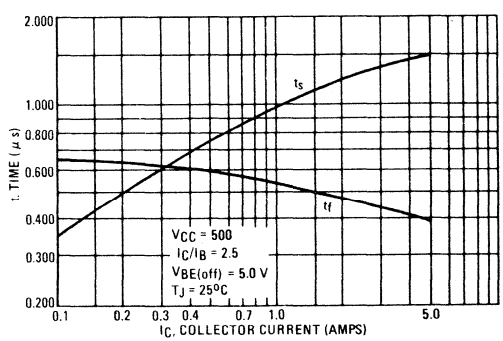


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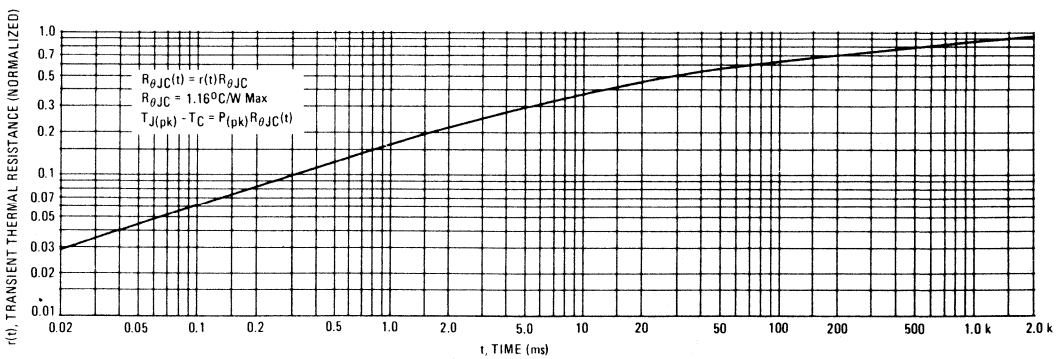
TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	+10 V, 20, 0, 1, 2 PW Varied to Attain I_C = 100 mA	250 µF, 470 Ω 2 W, 47 Ω, R1, +15, 15 V, 0, 330 Ω, 5.1 Ω 5 W, R2, 50 Ω, 100 Ω, 430 Ω, 39 Ω, 250 µF, Adjust to obtain $V_{BE(off)}$ = 5.0 V All Diodes – 1N4934 All NPN – MJE200 All PNP – MJE210 Adjust R1 to obtain I_{B1} For switching and RBB_{SOA}, R2 = 0 For $BV_{CEO(sus)}$, R2 = ∞	TURN ON TIME I_{B1} I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 500 V	V_{CC} = 500 V R_L = 200 Ω Pulse Width = 10 µs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT MR816, TUT, 1N4934, 1N4934, MR816, 1, 2, V_{clamp}, V_{CC}	OUTPUT WAVEFORMS I_C, $I_{C(pk)}$, t_f Clamped, t_1, t_f, t, V_{CE}, V_{CE} or V_{clamp}, Time, t_2 t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT MR816, TUT, 1N4934, 1N4934, 1, 2, R_L, V_{CC}

FIGURE 11 – THERMAL RESPONSE



SAFE OPERATING AREA INFORMATION

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

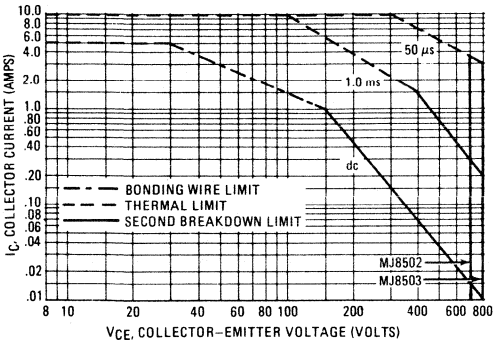
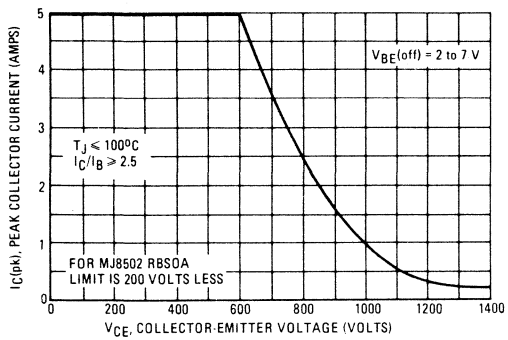


FIGURE 13 – RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA



FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

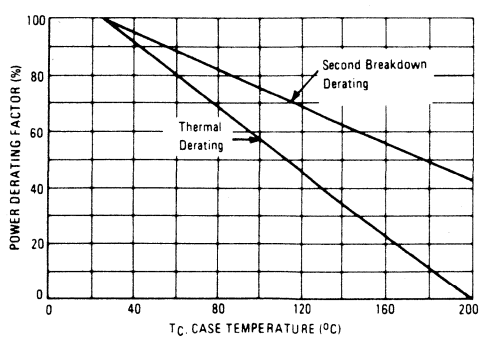
The data of Figure 12 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

FIGURE 14 – POWER DERATING



3

MJE340

PLASTIC MEDIUM POWER NPN SILICON TRANSISTOR

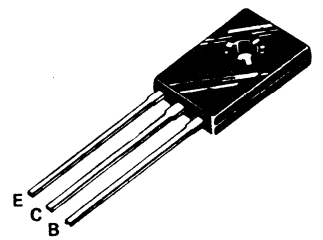
. . . designed for power output stages for television, radio, phonograph and other consumer product applications.

- Suitable for Transformerless, Line-Operated Equipment
- Thermopad ▲ Construction Provides High Power Dissipation Rating for High Reliability

0.5 AMPERE POWER TRANSISTOR

NPN SILICON

300 VOLTS
20.8



MAXIMUM RATINGS

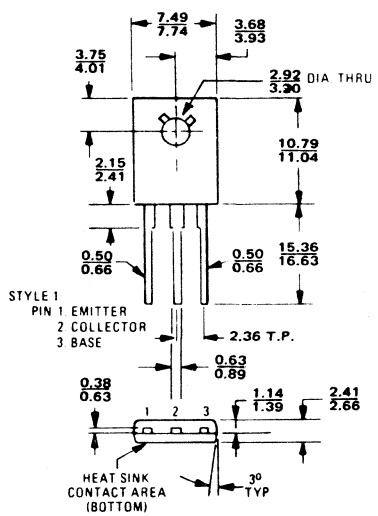
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	300	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current – Continuous	I_C	500	mAdc
		MJE340	
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	20.8 0.167	Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	MJE340	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.0	$^oC/W$

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	300	–	Vdc
Collector Cutoff Current (V_{CB} = 300 Vdc, I_E = 0)	I_{CBO}	–	100	μAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	240	–



When mounting the device, torque not to exceed 0.07 m-kg

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend

All dimensions in millimeters

CASE 77-04

FIGURE 1 – POWER TEMPERATURE DERATING

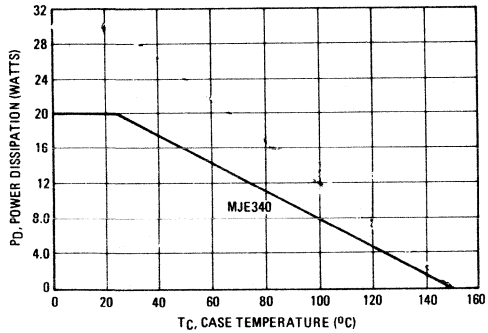
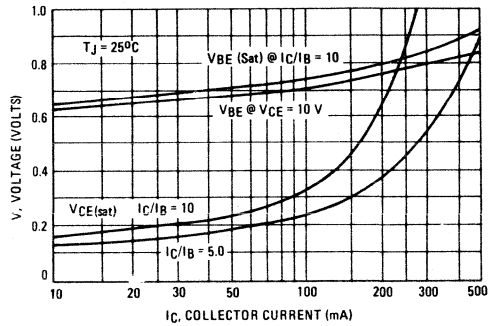
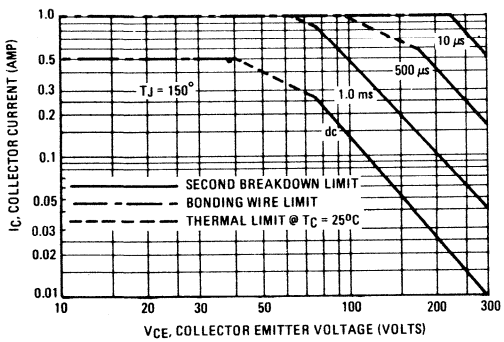


FIGURE 2 – "ON" VOLTAGES



ACTIVE-REGION SAFE OPERATING AREA

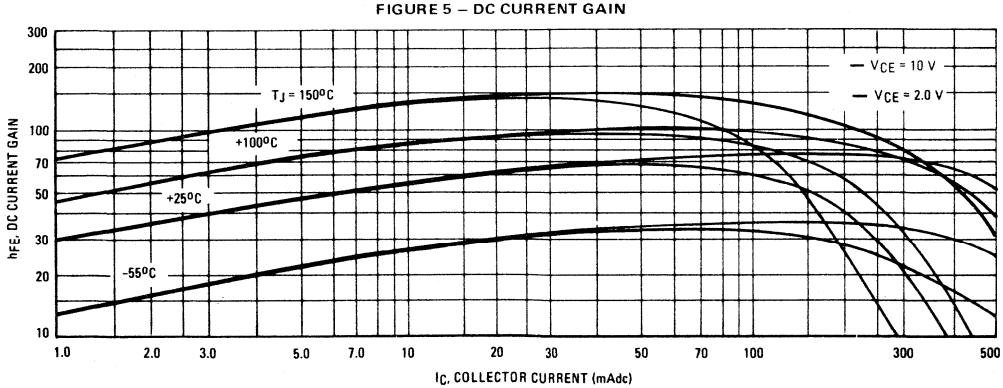
FIGURE 3 – MJE340



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 3 and 4 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^oC$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (Seee AN-415)

FIGURE 5 – DC CURRENT GAIN



MJE350

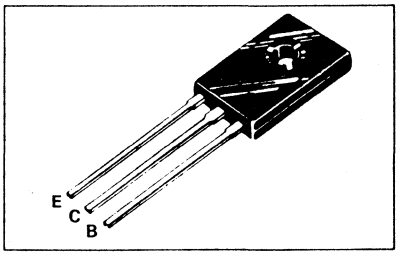
PLASTIC MEDIUM POWER PNP SILICON TRANSISTOR

. . . designed for use in line-operated audio and television applications and as low power, line-operated series pass and switching regulators.

- High Collector-Emitter Sustaining Voltage — $V_{CEO(sus)}$ = 300 Vdc @ I_C = 1.0 mAdc
- Excellent DC Current Gain — h_{FE} = 30-240 @ I_C = 50 mAdc
- Plastic Thermopad▲ Package

0.5 AMPERE
POWER TRANSISTOR
PNP SILICON

300 VOLTS
20 WATTS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	300	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current — Continuous	I_C	500	mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

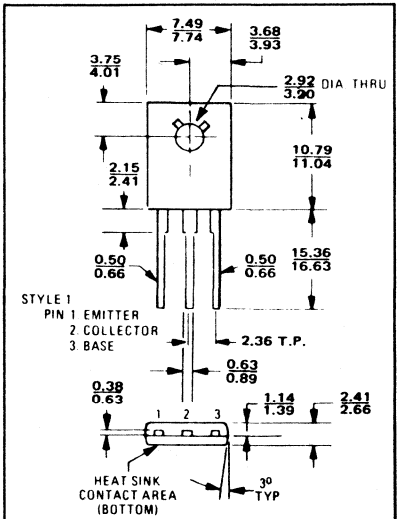
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	300	–	Vdc
Collector Cutoff Current (V_{CB} = 300 Vdc, I_E = 0)	I_{CBO}	–	100	μAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	240	–

▲Trademark of Motorola Inc., 1972



When mounting the device, torque not to exceed 0.07 m-kg

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

All dimensions in millimeters

CASE 77-04

FIGURE 1 – DC CURRENT GAIN

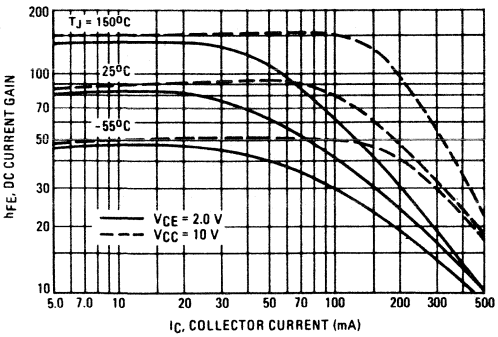


FIGURE 2 – "ON" VOLTAGES

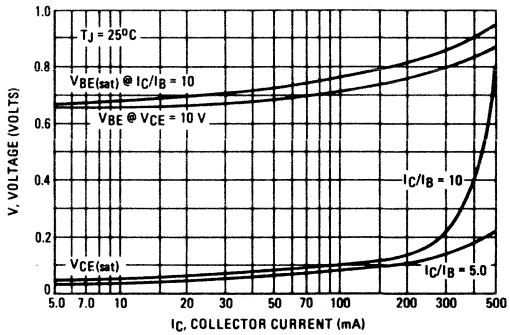


FIGURE 3 – ACTIVE-REGION SAFE OPERATING AREA

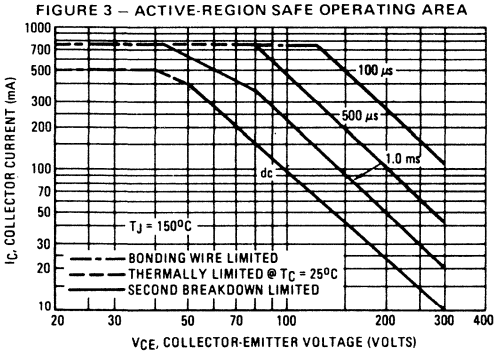
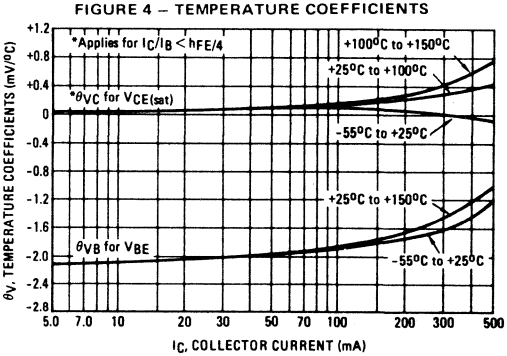


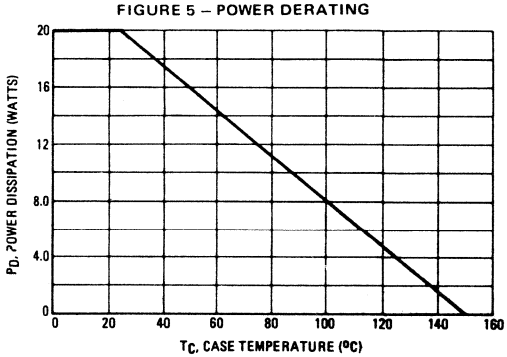
FIGURE 4 – TEMPERATURE COEFFICIENTS



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415).

FIGURE 5 – POWER DERATING



PNP

MJE700, T thru MJE703, T

NPN

MJE800, T thru MJE803, T

PLASTIC DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

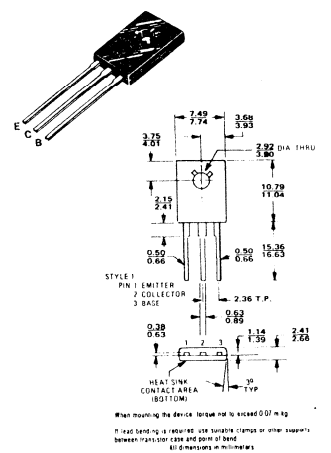
. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain –
  h_{FE} = 2000 (Typ) @ I_C = 2.0 Adc
- Monolithic Construction with Built-in Base-Emitter Resistors to Limit Leakage Muliplication
- Choice of Packages –
  TO126, MJE700 and MJE800 series
  TO220AB, MJE700T and MJE800T series

4.0 AMPERE

DARLINGTON POWER TRANSISTORS COMPLEMENTARY SILICON

40 WATT – TO-126
50 WATT – TO-220AB



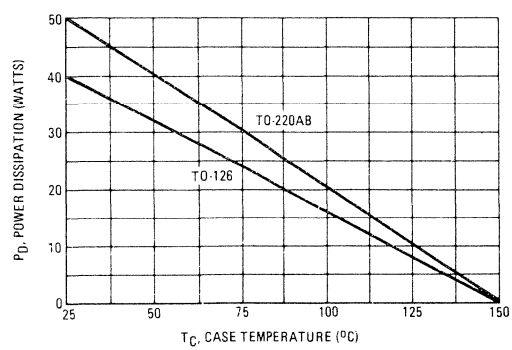
MAXIMUM RATINGS

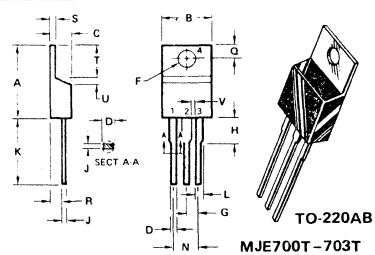
Rating	Symbol	MJE700,T MJE701,T MJE800,T MJE801,T	MJE702,T MJE703,T MJE802,T MJE803,T	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	4.0		Adc
Base Current	I_B	0.1		Adc
		TO-126	TO-220	
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32	50 0.40	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case TO-126 TO-220	$R_{\theta JC}$	 3.13 2.50	°C/W

FIGURE 1 – POWER DERATING





TO-220AB
MJE700T–703T
MJE800T–803T

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTE:
1. DIM. L & H APPLIES TO ALL LEADS.

CASE 221A-02

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1)		BV_{CEO}			Vdc
(I_C = 50 mAdc, I_B = 0)	MJE700,T, MJE701,T, MJE800,T, MJE801,T		60	–	
	MJE702,T, MJE703,T, MJE802,T, MJE803,T		80	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 60 Vdc, I_B = 0)	MJE700,T, MJE701,T, MJE800,T, MJE801,T		–	100	
(V_{CE} = 80 Vdc, I_B = 0)	MJE702,T, MJE703,T, MJE802,T, MJE803,T		–	100	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = Rated BV_{CEO}, I_E = 0)			–	100	
(V_{CB} = Rated BV_{CEO}, I_E = 0, T_C = 100°C)			–	500	
Emitter Cutoff Current		I_{EBO}	–	2.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
(I_C = 1.5 Adc, V_{CE} = 3.0 Vdc)	MJE700,T, MJE702,T, MJE800,T, MJE802,T		750	–	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	MJE701,T, MJE703,T, MJE801,T, MJE803,T		750	–	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	All devices		100	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 30 mAdc)	MJE700,T, MJE702,T, MJE800,T, MJE802,T		–	2.5	
(I_C = 2.0 Adc, I_B = 40 mAdc)	MJE701,T, MJE703,T, MJE801,T, MJE803,T		–	2.8	
(I_C = 4.0 Adc, I_B = 40 mAdc)	All Device		–	3.0	
Base-Emitter On Voltage (1)		$V_{BE(on)}$			Vdc
(I_C = 1.5 Adc, V_{CE} = 3.0 Vdc)	MJE700,T, MJE702,T, MJE800,T, MJE802,T		–	2.5	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	MJE701,T, MJE703,T, MJE801,T, MJE803,T		–	2.5	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	All Devices		–	3.0	
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain		$\|h_{fe}\|$	1.0	–	–
(I_C = 1.5 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)					

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

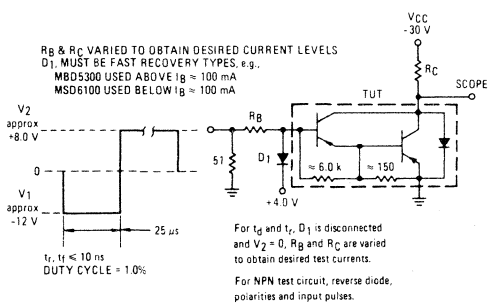


FIGURE 3 – SWITCHING TIMES

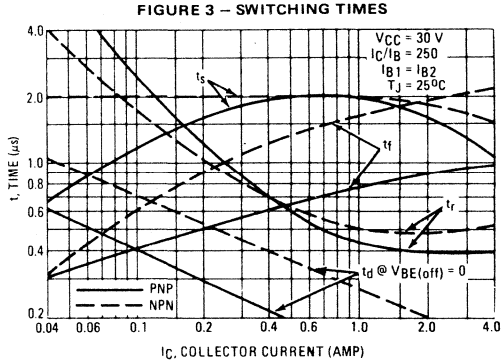


FIGURE 4 – THERMAL RESPONSE (MJE700T, 800T series)

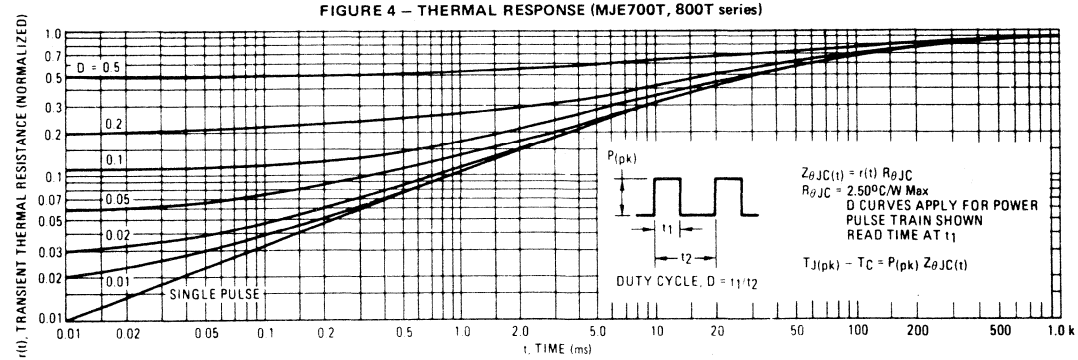
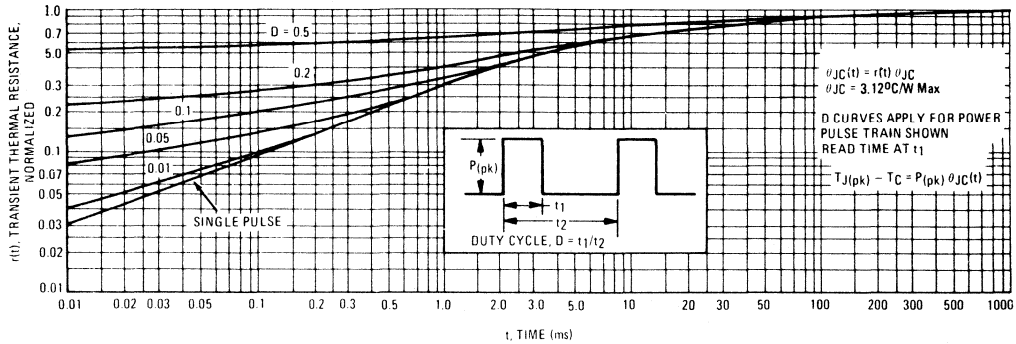


FIGURE 5 – THERMAL RESPONSE (MJE700, 800 series)



ACTIVE-REGION SAFE-OPERATING AREA

FIGURE 6 – MJE700 series

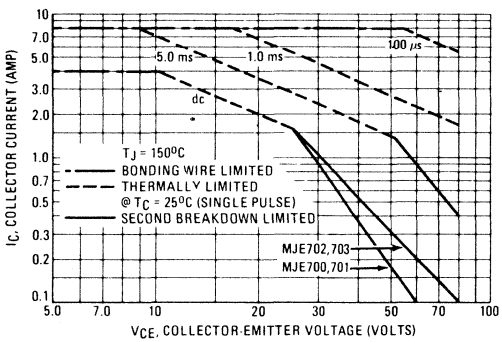
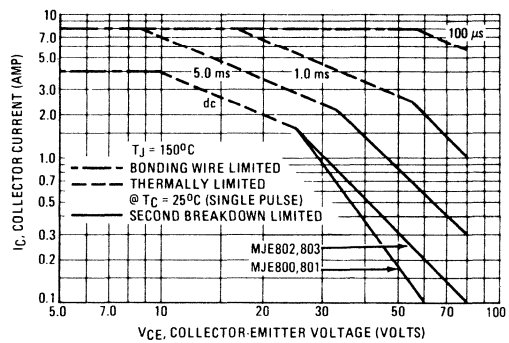


FIGURE 7 – MJE800 series



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 6 and 7 are based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4 or 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 8 – MJE700T series

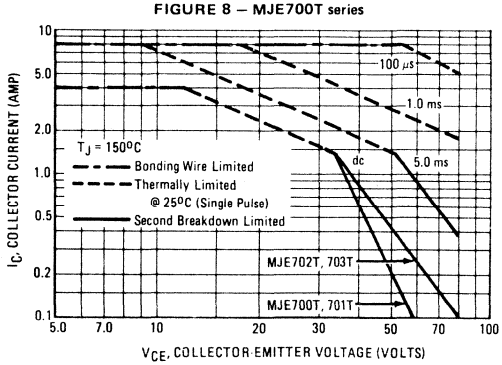
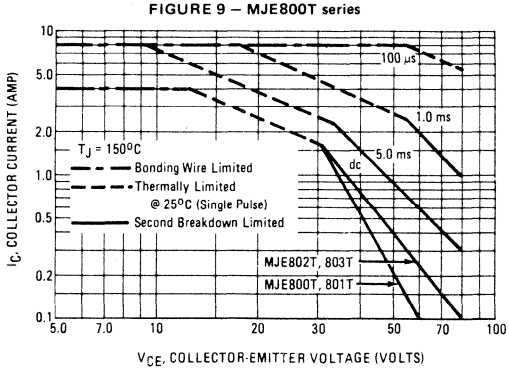


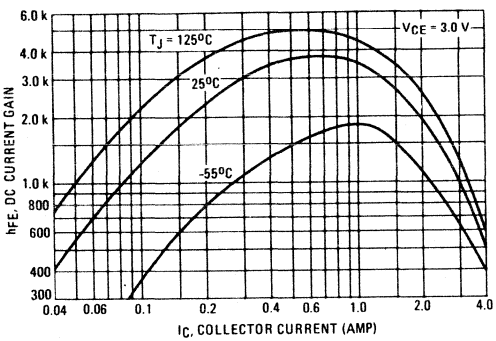
FIGURE 9 – MJE800T series



PNP
MJE700,T series

NPN
MJE800,T series

FIGURE 10 – DC CURRENT GAIN



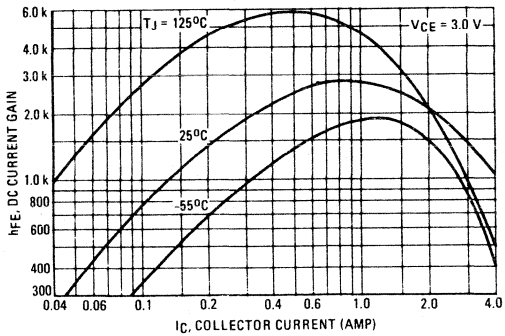
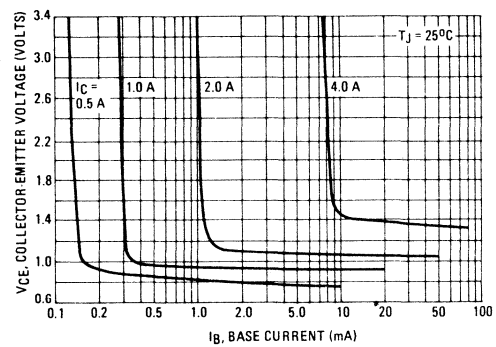


FIGURE 11 – COLLECTOR SATURATION REGION



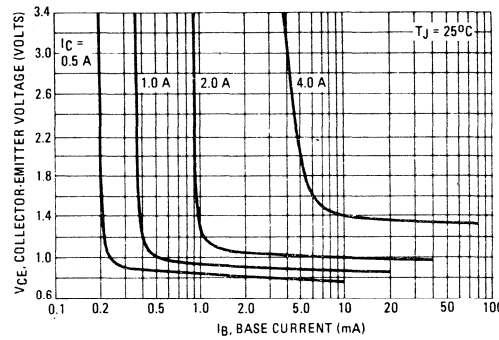
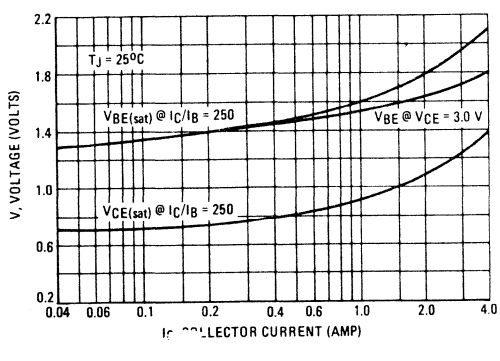
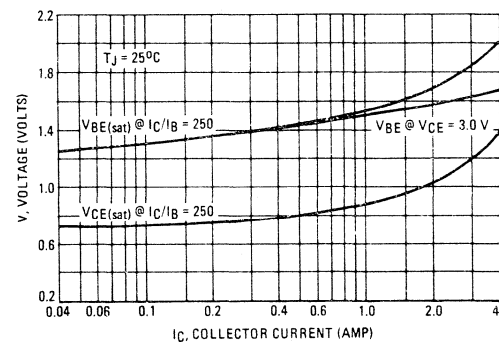


FIGURE 12 – "ON" VOLTAGES





3

PNP
MJE700,T series

NPN
MJE800,T series

FIGURE 13 – TEMPERATURE COEFFICIENTS

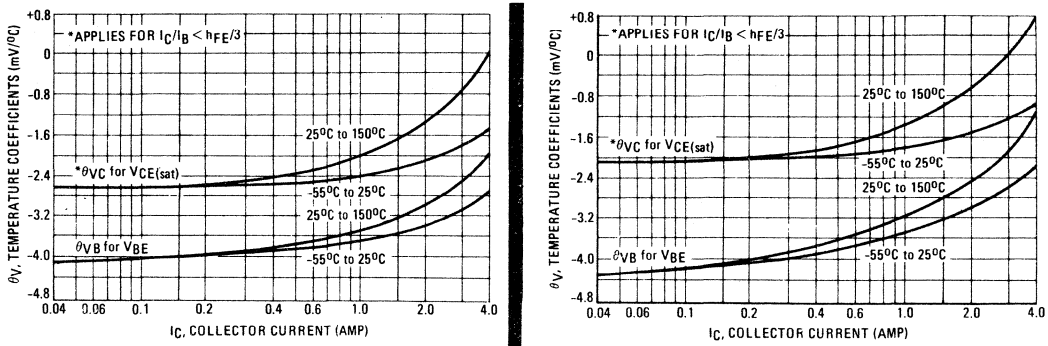


FIGURE 14 – COLLECTOR CUT-OFF REGION

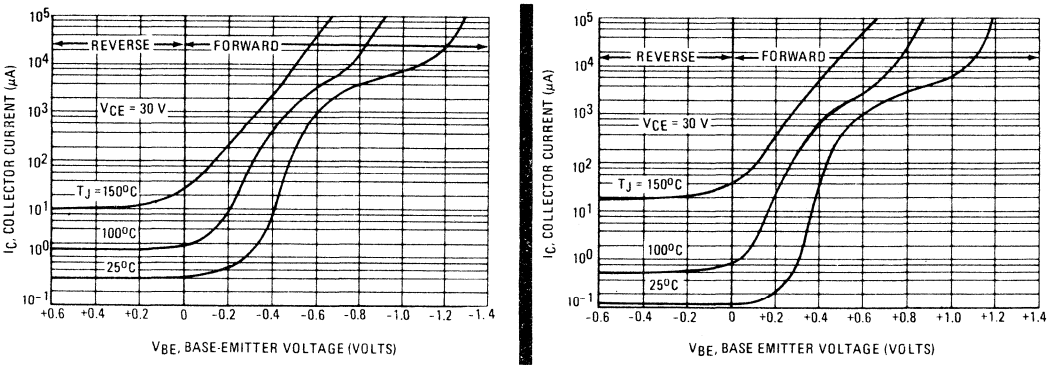


FIGURE 15 – CAPACITANCE

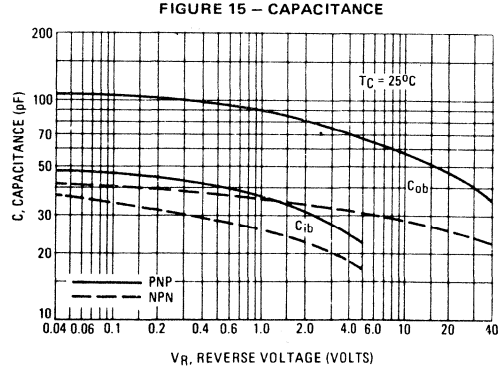
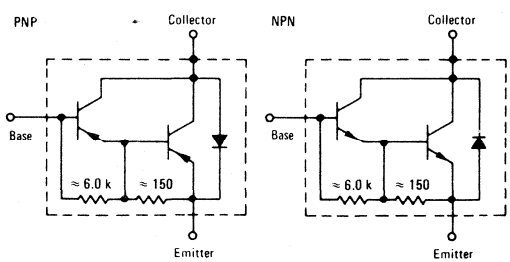


FIGURE 16 – DARLINGTON SCHEMATIC



MJE2955 • MJE2955T

HIGH POWER PNP SILICON TRANSISTORS

. . . designed for use in general-purpose amplifier and switching applications.

- DC Current Gain Specified to 10 Amperes
- High Current-Gain – Bandwidth Product – f_T = 2.0 MHZ (Min) @ I_C = 500 mAdc
- Thermopad▲ High-Efficiency Compact Package
- **Complement to NPN MJE3055, MJE3055T**
- **Choice of Packages – MJE2955-Case 90, MJE2955T TO-220**

10 AMPERE POWER TRANSISTORS PNP SILICON

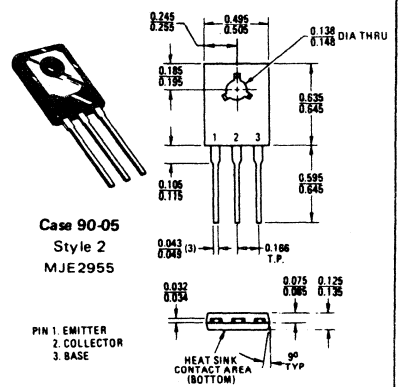
60 VOLTS
90, 75 WATTS

MAXIMUM RATINGS

Rating	Symbol	MJE 2955	MJE 2955T	Unit
Collector-Emitter Voltage	V_{CEO}	60		Vdc
Collector-Base Voltage	V_{CB}	70		Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current-Continuous	I_C	10		Adc
Base Current-Continuous	I_B	6.0		Adc
Total Device Dissipation @ T_C = 25 °C[1] Derate above 25 °C	P_D	90 0.718	75 0.6	Watts W/°C
Operating and Storage Junction	T_J, T_{stg}	−55 to +150		°C

THERMAL CHARACTERISTICS

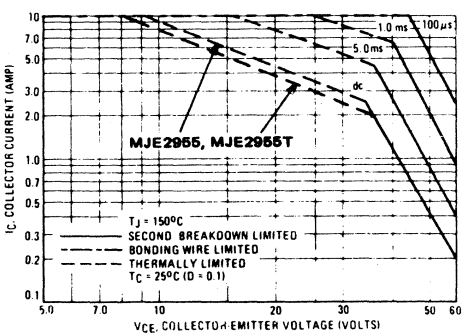
Characteristic	Symbol	Max.		Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.39	1.67	°C/W



Case 90-05
Style 2
MJE2955

To convert inches to millimeters multiply by 25.4

FIGURE 1 – ACTIVE REGION SAFE OPERATING AREAS

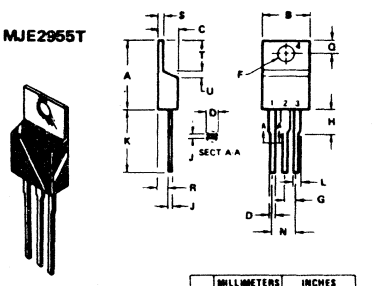


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C. T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN 415)

(1)Safe Area Curves are indicated by Figure 1 – Both thermal and safe area limits are applicable and must be observed.

MJE2955T



CASE 221A-02
TO-220AB

STYLE 1
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTE
1. DIM. L & H APPLIES TO ALL LEADS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	–	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	–	700	μAdc
Collector Cutoff Current (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	– –	1.0 5.0	mAdc
Collector Cutoff Current (V_{CB} = 70 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	– –	1.0 10	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	20 5.0	70 –	–
Collector-Emitter Saturation Voltage (1) (I_C = 4.0 Adc, I_B = 0.4 Adc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	– –	1.1 8.0	Vdc
Base-Emitter On Voltage (1) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 500 kHz)	f_T	2.0	–	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – DC CURRENT GAIN

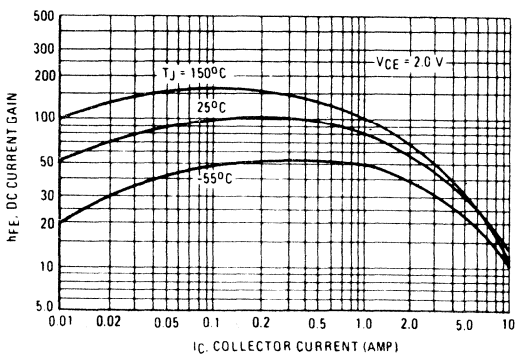
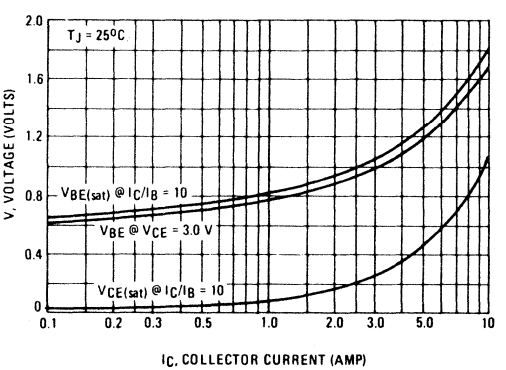


FIGURE 3 – "ON" VOLTAGES



MJE3055 • MJE3055T

HIGH POWER NPN SILICON TRANSISTORS

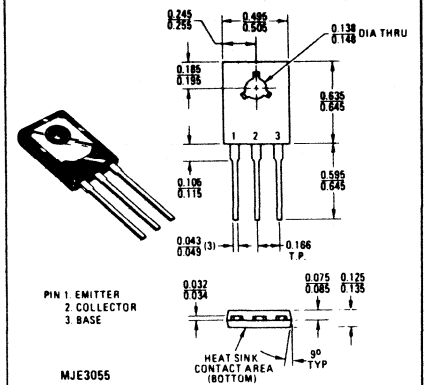
. . . designed for use in general-purpose amplifier and switching applications.

- DC Current Gain Specified to 10 Amperes
- High Current Gain – Bandwidth Product – f_T = 2.0 MHz (Min) @ I_C = 500 mAdc
- Thermopad ▲ High-Efficiency Compact Package
- Complement to PNP MJE2955, MJE2955T
- Choice of Packages – MJE3055 – Case 90
  MJE3055T – TO-220

10 AMPERE POWER TRANSISTORS

NPN SILICON

60 VOLTS
90, 75 WATTS



To convert inches to millimeters multiply by 25.4

CASE 90-05

MAXIMUM RATINGS

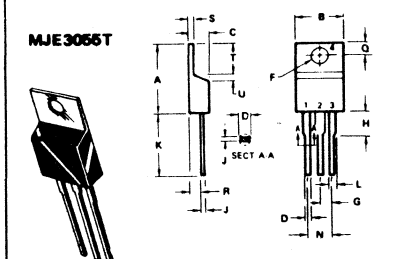
Rating	Symbol	MJE 3055	MJE 3055T	Unit
Collector-Emitter Voltage	V_{CEO}	60		Vdc
Collector-Base Voltage	V_{CB}	70		Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current-Continuous	I_C	10		Adc
Base Current-Continuous	I_B	6.0		Adc
Total Device Dissipation @ T_C = 25 °C[1] Derate above 25 °C	P_D	90 0.718	75 0.6	Watts W/°C
Operating and Storage Junction	T_J, T_{stg}	−55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.		Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.39	1.67	°C/W

[1] Safe Area Curves are indicated by figure 1 – Both thermal and safe area limits are applicable and must be observed.

▲ Trademark of Motorola Inc.



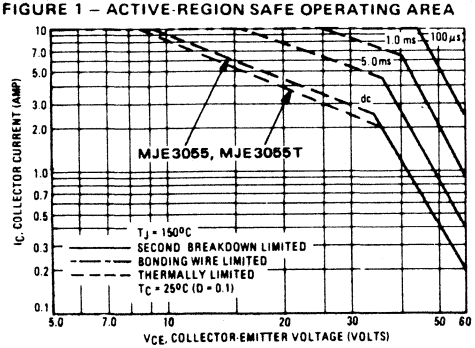
CASE 221A-02
TO-220AB

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.060
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTE
1. DIM. L & H APPLIES TO ALL LEADS.

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e. the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C. T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ ≤ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN 415)

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	–	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	–	700	μAdc
Collector Cutoff Current (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	– –	1.0 5.0	mAdc
Colltector Cutoff Current (V_{CB} = 70 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	– –	1.0 10	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	20 5.0	70 –	–
Collector-Emitter Saturation Voltage (1) (I_C = 4.0 Adc, I_B = 0.4 Adc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	– –	1.1 8.0	Vdc
Base-Emitter On Voltage (1) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 500 kHz)	f_T	2.0	–	MHz

(1) Pulse Test: Pulse Width≤300 μs, Duty Cycle≤2.0%.

FIGURE 2 – DC CURRENT GAIN

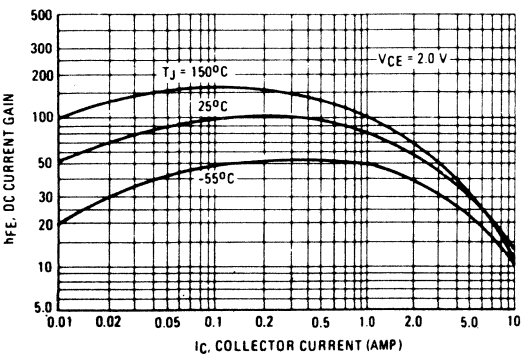
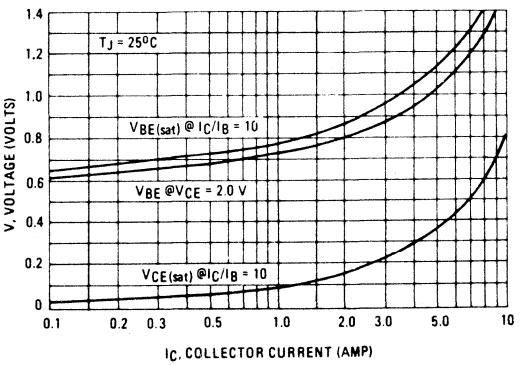


FIGURE 3 – "ON" VOLTAGES



MJE8500
MJE8501

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJE8500 and MJE8501 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times
- 300 ns Inductive Fall Time – 25°C (Typ)
- 500 ns Inductive Crossover Time – 25°C (Typ)
- 900 ns Inductive Storage Time – 25°C (Typ)

Operating Temperature Range –65 to +125°C

100°C Performance Specified for:
- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

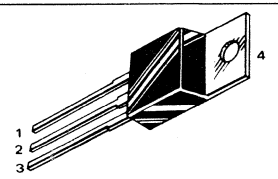
2.5 AMPERE

NPN SILICON POWER TRANSISTORS

700 and 800 VOLTS
65 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



3

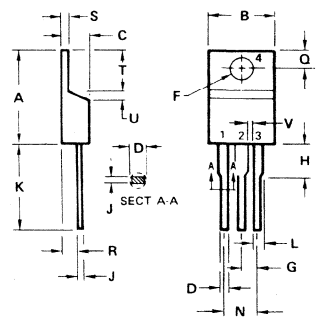
MAXIMUM RATINGS

Rating	Symbol	MJE8500	MJE8501	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	700	800	Vdc
Collector-Emitter Voltage	V_{CEV}	1200	1400	Vdc
Emitter Base Voltage	V_{EB}	8.0	8.0	Vdc
Collector Current – Continuous Peak (1)	I_C I_{CM}	2.5 5.0	2.5 5.0	Adc
Base Current – Continuous Peak (1)	I_B I_{BM}	2.0 4.0	2.0 4.0	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	65 17 0.65	65 17 0.65	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +125		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.54	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-02 TO-220

SWITCHMODE is a trademark of Motorola Inc.

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DS3383

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	MJE8500 MJE8501	$V_{CEO(sus)}$	700 800	– –	– –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	– –	– –	0.25 5.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	–	–	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	–	1.0	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 13			
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	7.5	–	–	–
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.33 Adc) (I_C = 2.5 Adc, I_B = 1.0 Adc) (I_C = 1.0 Adc, I_B = 0.33 Adc, T_C = 100°C)		$V_{CE(sat)}$	 – – –	 – – –	 2.0 5.0 3.0	Vdc
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.33 Adc) (I_C = 1.0 Adc, I_B = 0.33 Adc, TC = 100°C)		$V_{BE(sat)}$	 – –	 – –	 1.5 1.5	Vdc
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	50	–	250	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 500 Vdc, I_C = 1.0 A, I_{B1} = 0.33 A, $V_{BE(off)}$ = 5.0 Vdc, t_p = 50 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.045	0.20	μs
Rise Time		t_r	–	0.2	2.0	μs
Storage Time		t_s	–	1.0	4.0	μs
Fall Time		t_f	–	0.5	2.0	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 1.0 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 0.33 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	–	1.3	4.0	μs
Crossover Time		t_c	–	0.6	2.0	μs
Storage Time	(I_C = 1.0 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 0.33 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	–	0.9	–	μs
Crossover Time		t_c	–	0.5	–	μs
Fall Time		t_{fi}	–	0.3	–	μs

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤ 2%.

FIGURE 1 – DC CURRENT GAIN

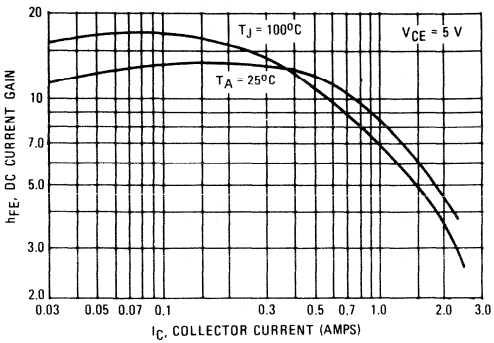

FIGURE 2 – COLLECTOR SATURATION REGION

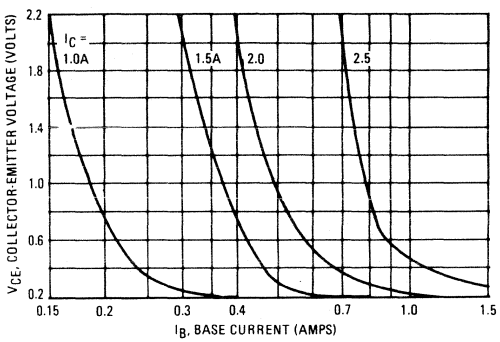

FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

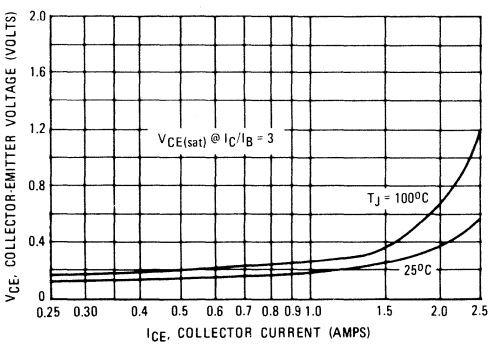

FIGURE 4 – BASE-EMITTER VOLTAGE

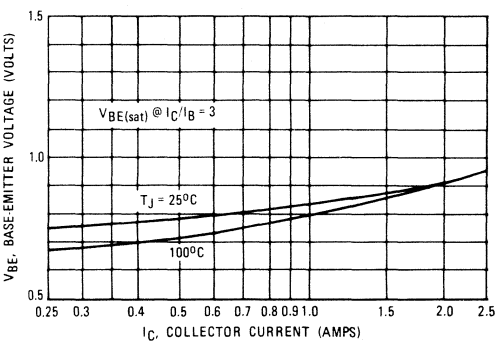

FIGURE 5 – COLLECTOR CUTOFF REGION

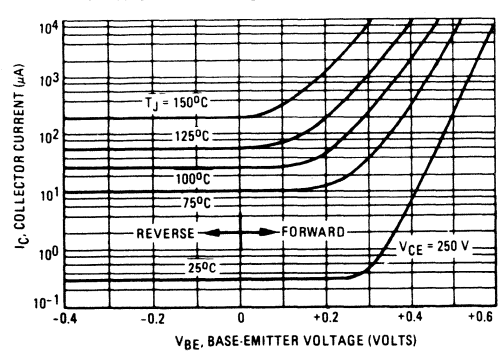

FIGURE 6 – CAPACITANCE

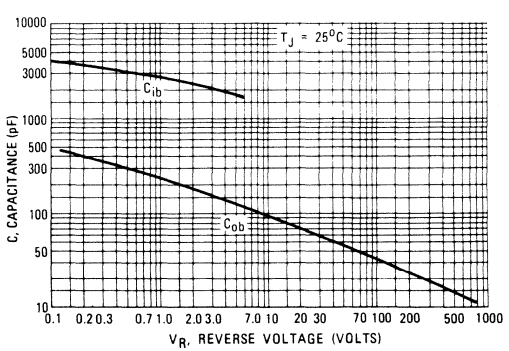

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FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

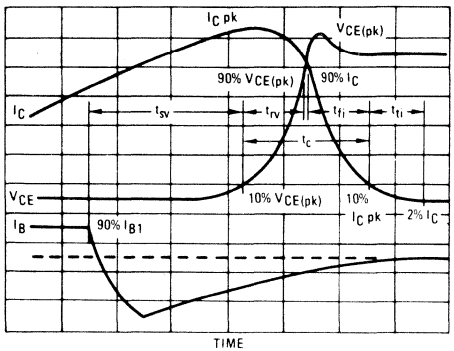
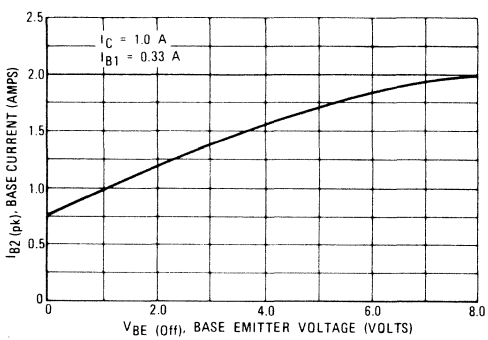


FIGURE 8 – PEAK REVERSE BASE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CE} (pk)
t_{rv} = Voltage Rise Time, 10–90% V_{CE} (pk)
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{CE} (pk) to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

TYPICAL RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 – TURN - ON SWITCHING TIMES

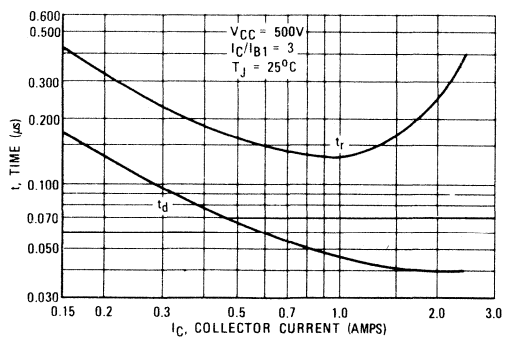


FIGURE 10 – TURN - OFF SWITCHING TIMES

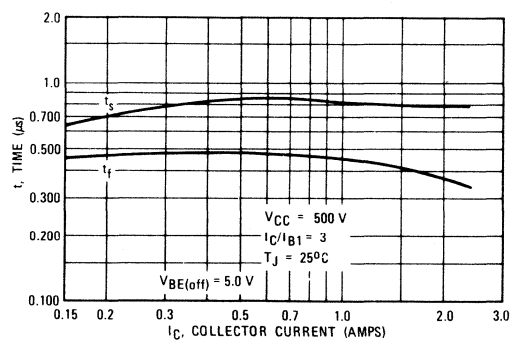
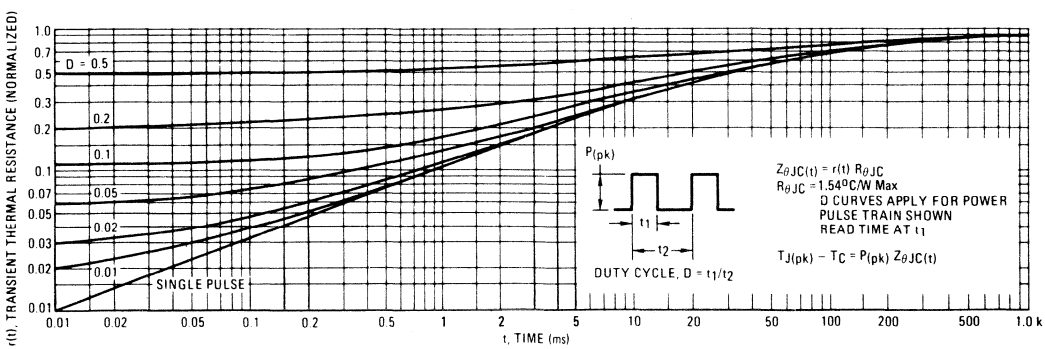


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	+10 V, 20, 0, 1, 2 PW Varied to Attain I_C = 100 mA	250 µF, 470 Ω 2 W, 47 Ω, R1, +15, 15 V, 0, 330 Ω, 5.1 Ω 5 W, R2, 50 Ω, 100 Ω, 430 Ω, 39 Ω, 250 µF, Adjust to obtain $V_{BE(off)}$ = 5.0 V All Diodes – 1N4934 All NPN – MJE200 All PNP – MJE210 Adjust R1 to obtain I_{B1} For switching and RB_{SOA}, R2 = 0 For $BV_{CEO(sus)}$, R2 = ∞	TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 500 V	V_{CC} = 500 V R_L = 500 Ω Pulse Width = 10 µs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT MR816, TUT, IN4934, MR816, IN4934, V_{clamp}, V_{CC}, 1, 2 OUTPUT WAVEFORMS I_C, $I_{C(pk)}$, t_f Clamped, t_1, t_f, t, V_{CE}, V_{CE} or V_{clamp}, Time, t_2 t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT MR816, TUT, IN4934, IN4934, R_L, V_{CC}, 1, 2

FIGURE 11 – THERMAL RESPONSE



SAFE OPERATING AREA INFORMATION

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

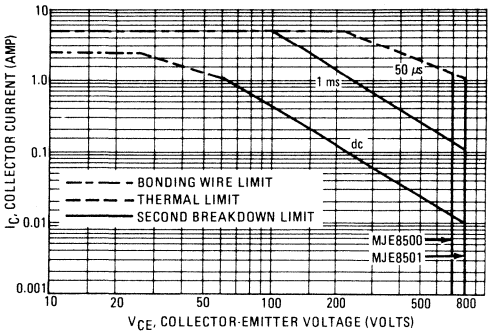
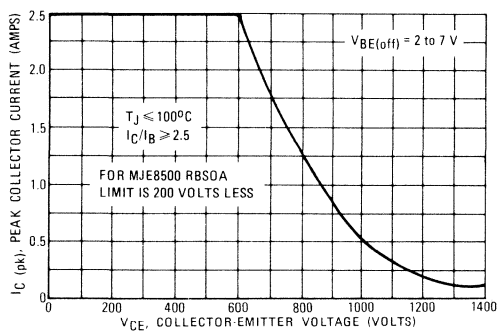


FIGURE 13 – RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA



FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

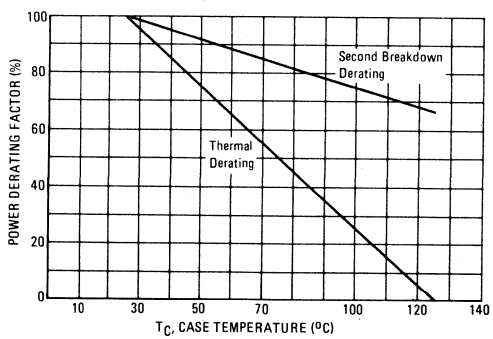
The data of Figure 12 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

FIGURE 14 – POWER DERATING



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MJE8502
MJE8503

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJE8502 and MJE8503 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times

150 ns Inductive Fall Time–25°C (Typ)

400 ns Inductive Crossover Time–25°C (Typ)

1200 ns Inductive Storage Time–25°C (Typ)

Operating Temperature Range –65 to +125°C

100°C Performance Specified for:

Reverse-Biased SOA with Inductive Loads

Switching Times with Inductive Loads

Saturation Voltages

Leakage Currents

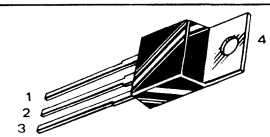
5.0 AMPERE

NPN SILICON POWER TRANSISTORS

700 and 800 VOLTS
80 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



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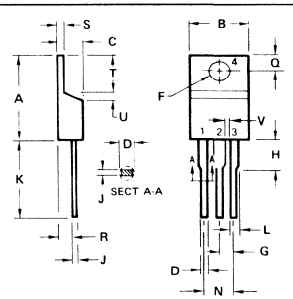
MAXIMUM RATINGS

Rating	Symbol	MJE8502	MJE8503	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	700	800	Vdc
Collector-Emitter Voltage	V_{CEV}	1200	1400	Vdc
Emitter Base Voltage	V_{EB}	8.0	8.0	Vdc
Collector Current – Continuous Peak (1)	I_C I_{CM}	5.0 10	5.0 10	Adc
Base Current – Continuous Peak (1)	I_B I_{BM}	4.0 8.0	4.0 8.0	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	80 21 0.80	80 21 0.80	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +125		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-02
TO-220

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DS3384

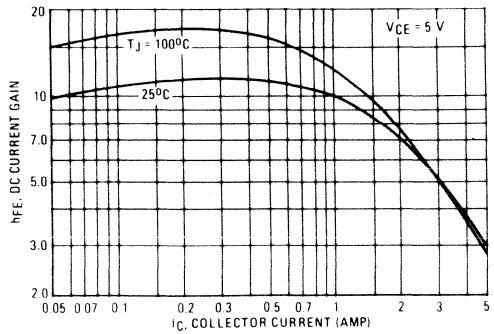
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	MJE8502 MJE8503	$V_{CEO(sus)}$	700 800	– –	– –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	 – –	 – –	 0.25 5.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	–	–	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	–	1.0	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 13			
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	7.5	–	–	–
Collector-Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 1.0 Adc) (I_C = 5.0 Adc, I_B = 2.0 Adc) (I_C = 2.5 Adc, I_B = 1.0 Adc, T_C = 100°C)		$V_{CE(sat)}$	 – – –	 – – –	 2.0 5.0 3.0	Vdc
Base-Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 1.0 Adc) (I_C = 2.5 Adc, I_B = 1.0 Adc, T_C = 100°C)		$V_{BE(sat)}$	 – –	 – –	 1.5 1.5	Vdc
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	60	–	300	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 500 Adc, IC = 2.5 A, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5.0 Vdc, t_p = 50 μs, Duty Cycle < 2.0%)	t_d	–	0.040	0.20	μs
Rise Time		t_r	–	0.125	2.0	μs
Storage Time		t_s	–	1.2	4.0	μs
Fall Time		t_f	–	0.65	2.0	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 2.5 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, TC = 100°C)	t_{sv}	–	1.6	5.0	μs
Crossover Time		t_c	–	0.60	2.0	μs
Storage Time	(I_C = 2.5 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	–	1.2	–	μs
Crossover Time		t_c	–	0.4	–	μs
Fall Time		t_{fi}	–	0.15	–	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN



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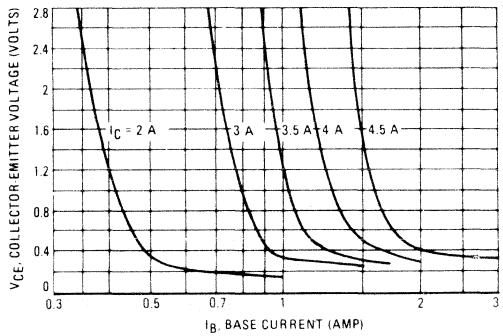


FIGURE 3 – COLLECTOR-EMITTER SATURATION REGION

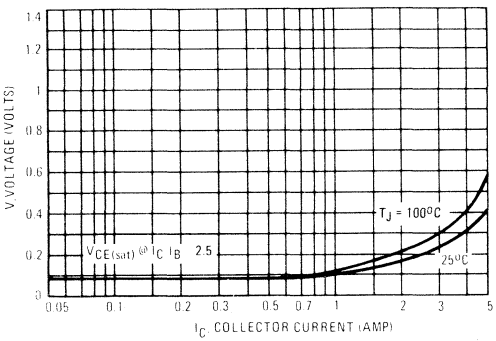


FIGURE 4 – BASE-EMITTER VOLTAGE

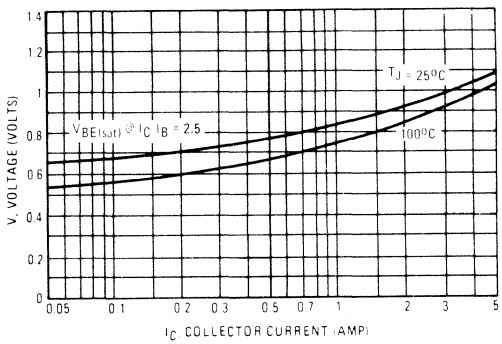
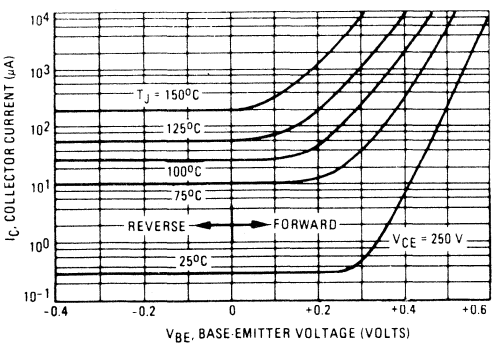


FIGURE 5 – COLLECTOR CUTOFF REGION



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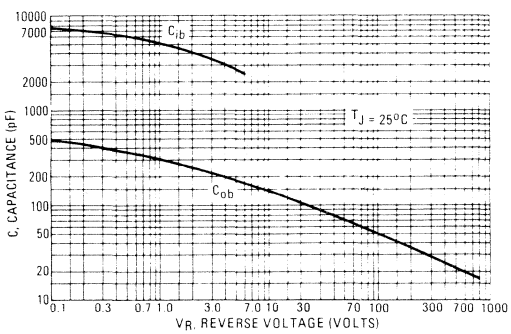

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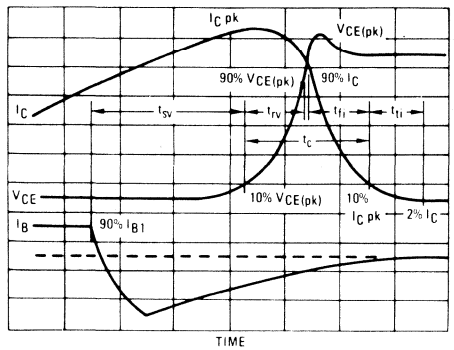

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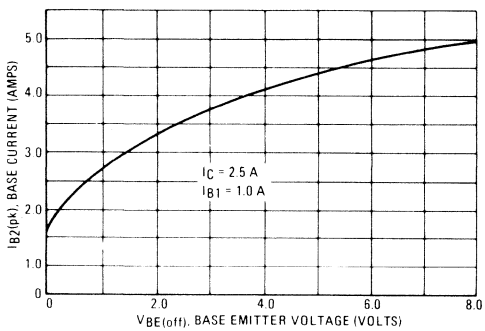

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t_{ti} = Current Tail, 10–2% I_C
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$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

TYPICAL RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 – TURN-ON SWITCHING TIMES

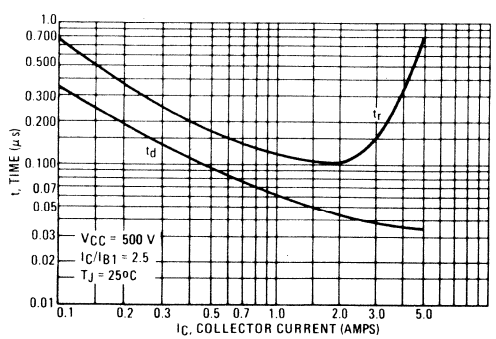


FIGURE 10 – TURN-OFF SWITCHING TIMES

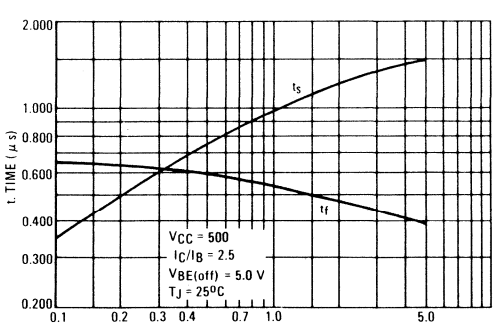
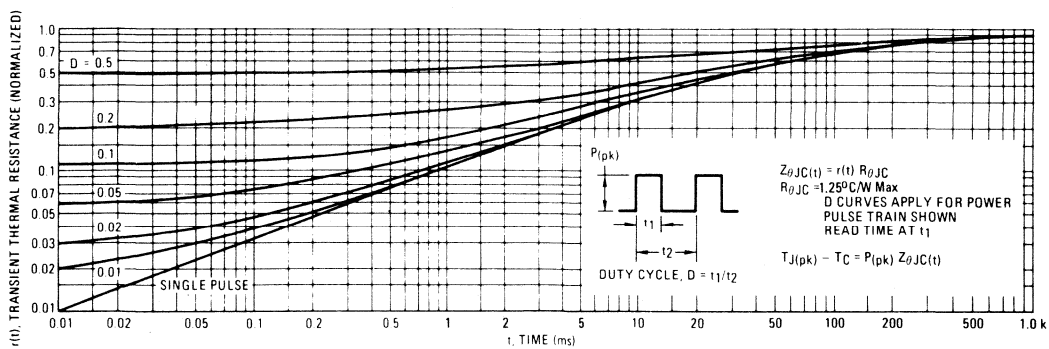


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	+10 V, 20, 0, 1, 2 PW Varied to Attain I_C = 100 mA	250 μF, 470 Ω 2 W, 47 Ω, R1, +15, 15 V, 0, 330 Ω, 5.1 Ω 5 W, R2, 50 Ω, 100 Ω, 430 Ω, 39 Ω, 250 μF, Adjust to obtain $V_{BE(off)}$ = 5.0 V All Diodes – 1N4934 All NPN – MJE200 All PNP – MJE210 Adjust R1 to obtain I_{B1} For switching and RB_{SOA}, R2 = 0 For $BV_{CEO(sus)}$, R2 = ∞	TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 500 V	V_{CC} = 500 V R_L = 200 Ω Pulse Width = 10 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT MR816, TUT, IN4934, MR816, IN4934, V_{clamp}, V_{CC}, 1, 2	OUTPUT WAVEFORMS I_C, $I_{C(pk)}$, t_f Clamped, t_1, t_f, t, V_{CE}, V_{CE} or V_{clamp}, Time, t_2 t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT MR816, TUT, IN4934, R_L, V_{CC}, 1, 2

FIGURE 11 – THERMAL RESPONSE



SAFE OPERATING AREA INFORMATION

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

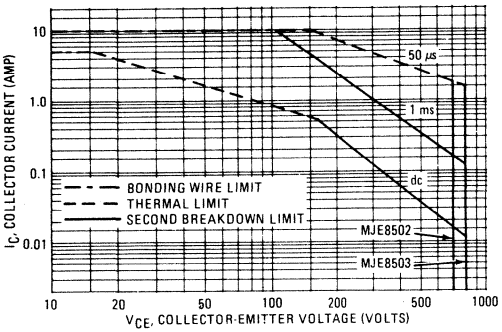
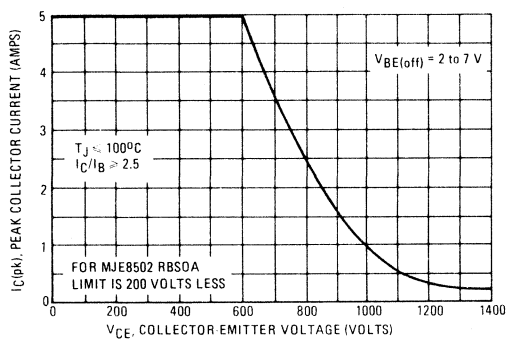


FIGURE 13 – RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA



FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

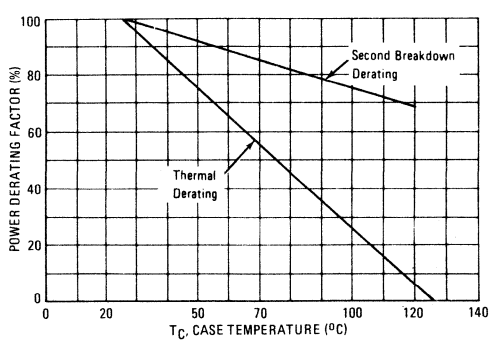
The data of Figure 12 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

FIGURE 14 – POWER DERATING



Motorola reserves the right to make changes to any products herein to improve reliability, function or design. Motorola does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights nor the rights of others.

NPN PNP

MJ15011 MJ15012

Advance Information

COMPLEMENTARY SILICON POWER TRANSISTORS

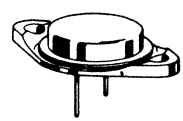
The MJ15011 and MJ15012 are Power Base power transistors designed for high-power audio, disk head positioners, and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc-to-dc converters or inverters.

- High Safe Operating Area (100% Tested)
  1.2 A @ 100 V
- Completely Characterized for Linear Operation
- High DC Current Gain and Low Saturation Voltage
  h_{FE} = 20 (Min) @ 2 A, 2 V
  $V_{CE(sat)}$ = 2.5 V (Max) @ I_C = 4 A, I_B = 0.4 A
- For Low Distortion Complementary Designs

10 AMPERE

COMPLEMENTARY POWER TRANSISTORS

250 VOLTS
200 WATTS



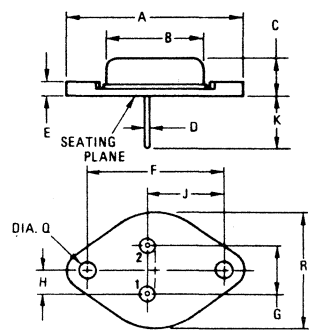
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	250	Vdc
Collector-Emitter Voltage	V_{CEX}	250	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	10 15	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 5	Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	12 20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.875	°C/W
Maximum Lead Temperature for Soldering Purposes	T_L	265	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
(TO-3)

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 100 mA)	$V_{CEO(sus)}$	250	–	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc)	I_{CEO}	–	1	mAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	–	500	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc)	I_{EBO}	–	500	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 2 Adc, V_{CE} = 2 Vdc) (I_C = 4 Adc, V_{CE} = 2 Vdc)	h_{FE}	 20 5	 100 –	–
Collector-Emitter Saturation Voltage (I_C = 2 Adc, I_B = 0.2 Adc) (I_C = 4 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$	 –	 0.8 2.5	Vdc
Base-Emitter On Voltage (I_C = 4 Adc, V_{CE} = 2 Vdc)	$V_{BE(on)}$	–	2	Vdc
DYNAMIC CHARACTERISTICS				
Output Capacitance (V_{CB} = 10 Vdc, f = 1 MHz)	C_{ob}	–	250	pF
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 50 Vdc, t = 0.5 s) (V_{CE} = 100 Vdc, t = 0.5 s)	$I_{S/b}$	 4 1.2	 – –	Adc

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

FIGURE 1 – DC CURRENT GAIN

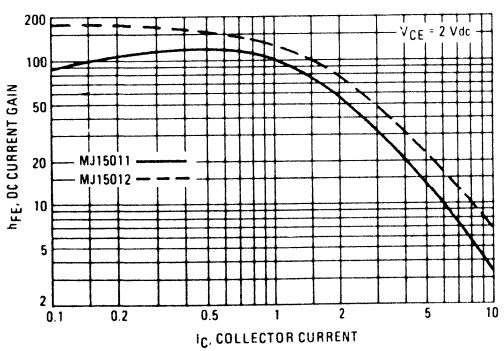
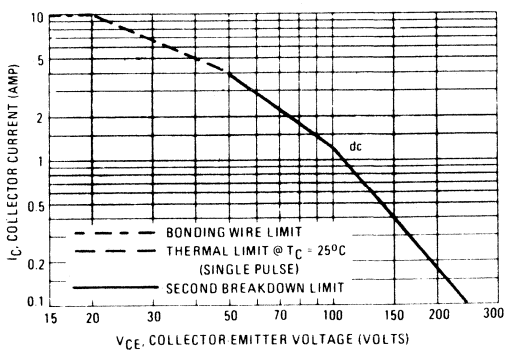


FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



NPN
MJ15022
MJ15024

SILICON POWER TRANSISTORS

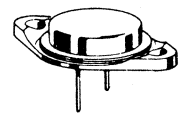
The MJ15022 and MJ15024 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) – 2 A @ 80 V
- High DC Current Gain – h_{FE} = 15 (Min) @ I_C = 8 Adc

16 AMPERE

SILICON POWER TRANSISTORS

200 and 250 VOLTS
250 WATTS



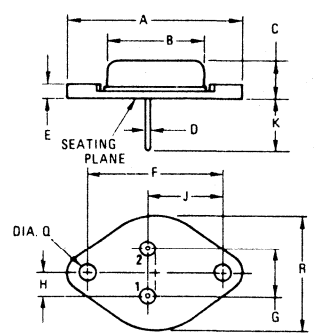
MAXIMUM RATINGS

Rating	Symbol	MJ15022	MJ15024	Unit
Collector-Emitter Voltage	V_{CEO}	200	250	Vdc
Collector-Base Voltage	V_{CBO}	350	400	Vdc
Emitter-Base Voltage	V_{EBO}	7		Vdc
Collector-Emitter Voltage	V_{CEX}	400		Vdc
Collector Current – Continuous Peak (1)	I_C	16 30		Adc
Base Current – Continuous	I_B	5		Adc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	250 1.43		Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.70	$^oC/W$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
(TO-3)

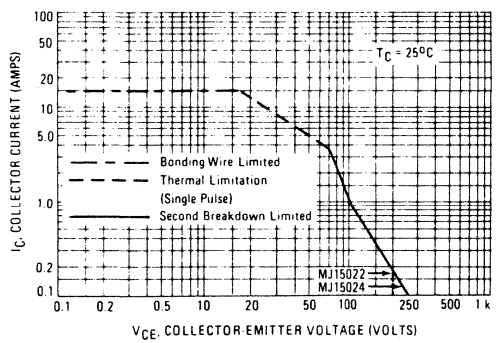
3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			
(I_C = 100 mAdc, I_B = 0)	MJ15022		200	–	
	MJ15024		250	–	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = 200 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	MJ15022		–	250	μAdc
(V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	MJ15024		–	250	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 150 Vdc, I_B = 0)	MJ15022		–	500	
(V_{CE} = 200 Vdc, I_B = 0)	MJ15024		–	500	
Emitter Cutoff Current		I_{EBO}	–	500	μAdc
(V_{CE} = 7 Vdc, I_B = 0)	Both				
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$			Adc
(V_{CE} = 50 Vdc, t = 0.5 s (non-repetitive))			5	–	
(V_{CE} = 80 Vdc, t = 0.5 s (non-repetitive))			2	–	
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 8 Adc, V_{CE} = 4 Vdc)			15	60	
(I_C = 16 Adc, V_{CE} = 4 Vdc)			5	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 8 Adc, I_B = 0.8 Adc)			–	1 4	
(I_C = 16 Adc, I_B = 3.2 Adc)			–	4.0	
Base-Emitter On Voltage		$V_{BE(on)}$	–	2.2	Vdc
(I_C = 8 Adc, V_{CE} = 4 Vdc)					
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product		f_T	4	–	MHz
(I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)					
Output Capacitance		C_{ob}	–	500	pF
(V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)					

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

FIGURE 2 – CAPACITANCES

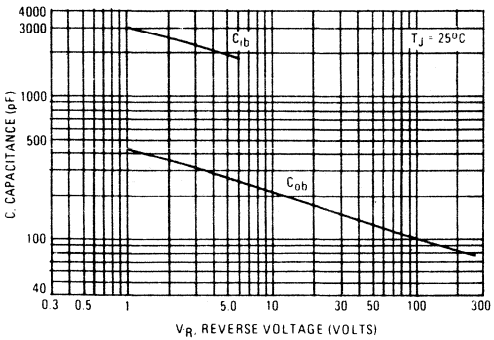


FIGURE 3 – CURRENT-GAIN–BANDWIDTH PRODUCT

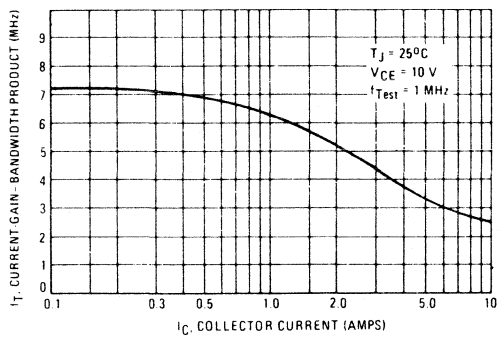


FIGURE 4 – DC CURRENT GAIN

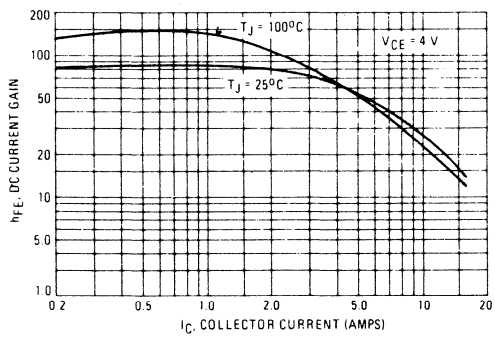


FIGURE 5 – "ON" VOLTAGE

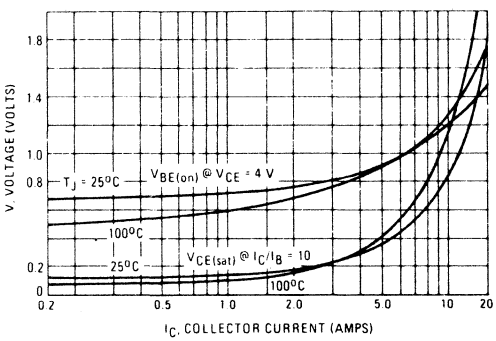
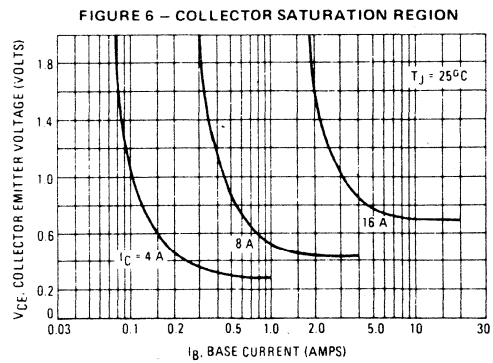


FIGURE 6 – COLLECTOR SATURATION REGION



3

PNP

MJ15023
MJ15025

SILICON POWER TRANSISTORS

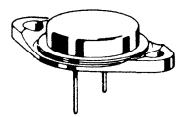
The MJ15023 and MJ15025 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) – 2 A @ 80 V
- High DC Current Gain – h_{FE} = 15 (Min) @ I_C = 8 Adc

16 AMPERE

SILICON POWER TRANSISTORS

200 and 250 VOLTS
250 WATTS



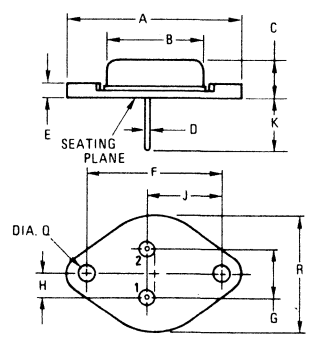
MAXIMUM RATINGS

Rating	Symbol	MJ15023	MJ15025	Unit
Collector-Emitter Voltage	V_{CEO}	200	250	Vdc
Collector-Base Voltage	V_{CBO}	350	400	Vdc
Emitter-Base Voltage	V_{EBO}	7		Vdc
Collector-Emitter Voltage	V_{CEX}	400		Vdc
Collector Current – Continuous Peak (1)	I_C	16 30		Adc
Base Current – Continuous	I_B	5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.70	°C/W

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

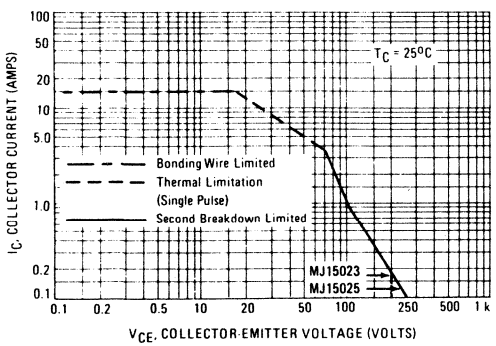
Collector connected to case.
'CASE 11-01
(TO-3)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			
(I_C = 100 mAdc, I_B = 0)	MJ15023		200	–	
	MJ15025		250	–	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = 200 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	MJ15023		–	250	μAdc
(V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	MJ15025		–	250	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 150 Vdc, I_B = 0)	MJ15023		–	500	
(V_{CE} = 200 Vdc, I_B = 0)	MJ15025		–	500	
Emitter Cutoff Current		I_{EBO}	–	500	μAdc
(V_{CE} = 7 Vdc, I_B = 0)	Both				
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$			Adc
(V_{CE} = 50 Vdc, t = 0.5 s (non-repetitive))			5	–	
(V_{CE} = 80 Vdc, t = 0.5 s (non-repetitive))			2	–	
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 8 Adc, V_{CE} = 4 Vdc)			15	60	
(I_C = 16 Adc, V_{CE} = 4 Vdc)			5	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 8 Adc, I_B = 0.8 Adc)			–	1.4	
(I_C = 16 Adc, I_B = 3.2 Adc)			–	4.0	
Base-Emitter On Voltage		$V_{BE(on)}$	–	2.2	Vdc
(I_C = 8 Adc, V_{CE} = 4 Vdc)					
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product		f_T	4	–	MHz
(I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)					
Output Capacitance		C_{ob}	–	500	pF
(V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)					

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

TYPICAL CHARACTERISTICS

FIGURE 2 – CAPACITANCES

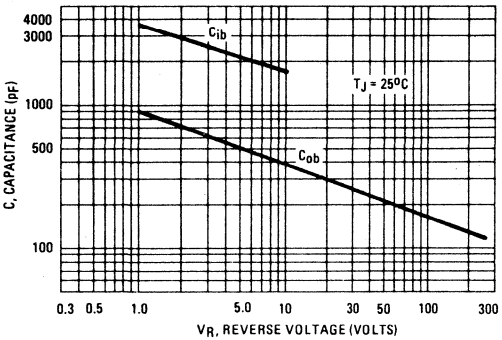


FIGURE 3 – CURRENT-GAIN–BANDWIDTH PRODUCT

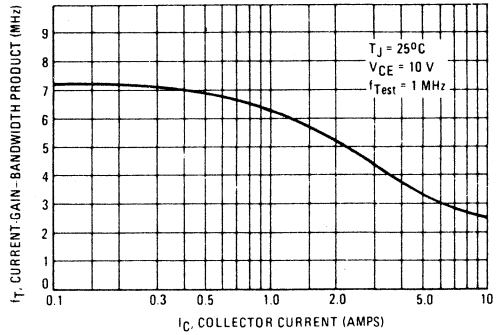


FIGURE 4 – DC CURRENT GAIN

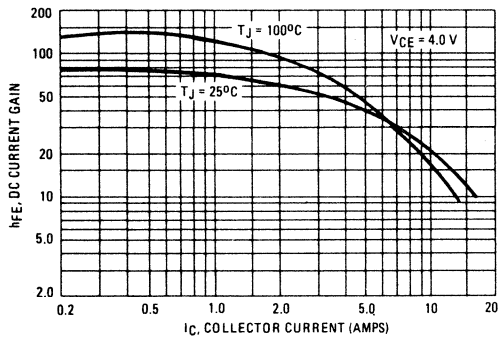
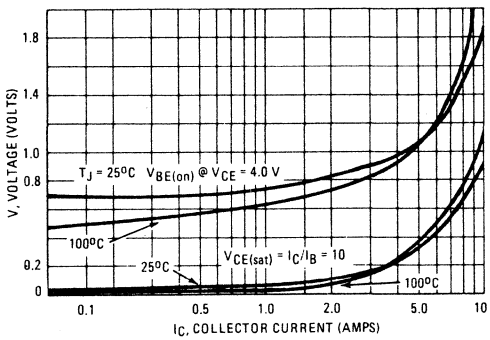


FIGURE 5 – "ON" VOLTAGE



NPN PNP

MJE15028 MJE15029
MJE15030 MJE15031

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

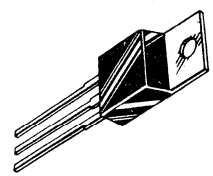
. . . designed for use as high-frequency drivers in audio amplifiers.

- DC Current Gain Specified to 4.0 Amperes
  h_{FE} = 40(Min) @ I_C = 3.0 Adc
  = 20(Min) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 120 Vdc (Min) – MJE15028, MJE15029
  = 150 Vdc (Min) – MJE15030, MJE15031
- High Current Gain – Bandwidth Product
  f_T = 30 MHz (Min) @ I_C = 500 mAdc
- TO-220AB Compact Package
- TO-66 Leadform Also Available

8 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

120–150 VOLTS
50 WATTS



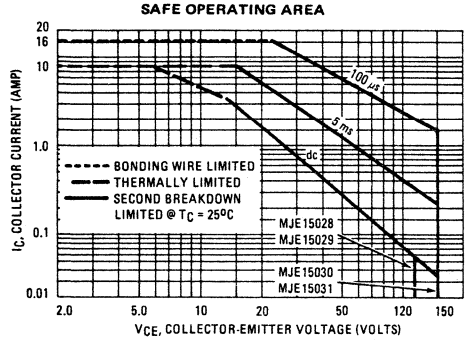
MAXIMUM RATINGS

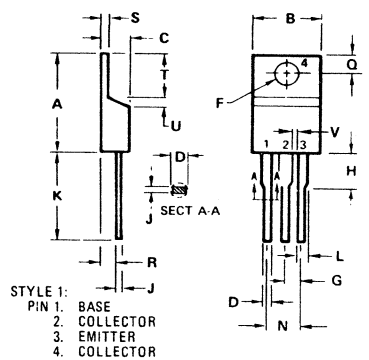
Rating	Symbol	MJE15028 MJE15029	MJE15030 MJE15031	Unit
Collector-Emitter Voltage	V_{CEO}	120	150	Vdc
Collector-Base Voltage	V_{CB}	120	150	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous – Peak	I_C	8.0 16		Adc
Base Current	I_B	2.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.40		Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

FIGURE 3 – FORWARD BIAS SAFE OPERATING AREA





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

CASE 221A-02
TO-220AB

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 10 mAdc, I_B = 0)	MJE15028, MJE15029		120	–	
	MJE15030, MJE15031		150	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 120 Vdc, I_B = 0)	MJE15028, MJE15029		–	0.1	
(V_{CE} = 150 Vdc, I_B = 0)	MJE15030, MJE15031		–	0.1	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 120 Vdc, I_E = 0)	MJE15028, MJE15029		–	10	
(V_{CB} = 150 Vdc, I_E = 0)	MJE15030, MJE15031		–	10	
Emitter Cutoff Current		I_{EBO}	–	10	μAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 0.1 Adc, V_{CE} = 2.0 Vdc)			40	–	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)			40	–	
(I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)			40	–	
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)			20	–	
DC Current Gain Linearity		h_{FE}	Typ		
(V_{CE} From 2.0V to 20V, I_C From 0.1A to 3A)			2		
(NPN TO PNP)			3		
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	–	0.5	Vdc
(I_C = 1.0 Adc, I_B = 0.1 Adc)					
Base-Emitter On Voltage		$V_{BE(on)}$	–	1.0	Vdc
(I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (2)		f_T	30	–	MHz
(I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)					

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2)$f_T = |h_{fe}| \bullet f_{test}$

MTM474, MTM475
MTP474, MTP475

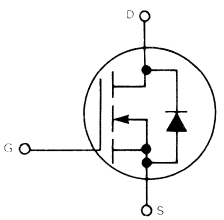
Designers Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designers Data — I_{DSS}, $V_{DS(on)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)}$ 4.0 Volts (max)

TMOS™

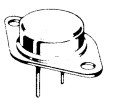


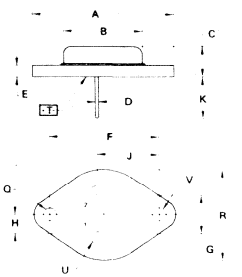
4 AMPERE

N-CHANNEL TMOS POWER FET

450 and 500 VOLTS

MTM474
MTM475



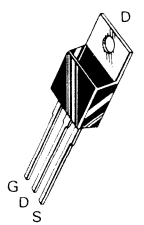


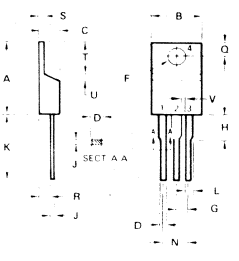
STYLE 3
PIN 1. GATE
2. SOURCE
3. DRAIN

CASE 1-05
TO-3 TYPE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A		39.37		1.550
B		21.08		0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R		26.67		1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

MTP474
MTP475





STYLE 5
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 221A-02
TO-220AB

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14		0.045	

MAXIMUM RATINGS

Rating	Symbol	MTM474 MTP474	MTM475 MTP475	Unit
Drain — Source Voltage	V_{DSS}	450	500	Vdc
Drain — Gate Voltage	V_{DGO}	450	500	Vdc
Gate — Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 4.0 8.0		Adc
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

TMOS is a trademark of Motorola Inc.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 mA)	MTM564/MTP564 MTM565/MTP565	$V_{(BR)DSS}$	 350 400	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 BV_{DSS}, V_{GS} = 0) T_J = 100°C		I_{DSS}	 — —	 0.25 2.5	mAdc
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	1.5	4.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 2.5 Adc) (I_D = 5.0 Adc) (I_D = 2.5 Adc, T_J = 100°C)		$V_{DS(on)}$	 — — —	 3.75 8.0 6.0	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2.5 Adc)		$r_{DS(on)}$	—	1.5	Ohms
Forward Transconductance (V_{DS} = 15 V, I_D = 2.5 A)		g_{fs}	2.0	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)		C_{iss}	—	1200	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)		C_{oss}	—	300	pF
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)		C_{rss}	—	80	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time (V_{DS} = 25 V, I_D = 2.5 A, R_{gen} = 50 ohms)		$t_{d(on)}$	—	50	ns
Rise Time (V_{DS} = 25 V, I_D = 2.5 A, R_{gen} 50 ohms)		t_r	—	100	ns
Turn-Off Delay Time (V_{DS} = 25 V, I_D = 2.5 A, R_{gen} = 50 ohms)		$t_{d(off)}$	—	200	ns
Fall Time (V_{DS} = 25 V, I_D = 2.5 A, R_{gen} = 50 ohms)		t_f	—	100	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = 5.0 A	V_{SD}	1.1	Vdc
Forward Turn-On Time	V_{GS} = 0	t_{on}	250	ns
Reverse Recovery Time	See Figures 17 and 18	t_{rr}	420	ns

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

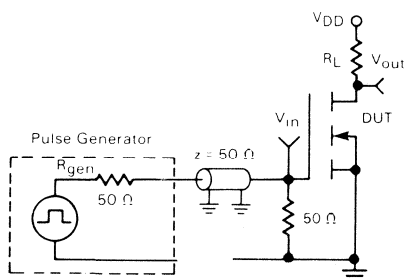
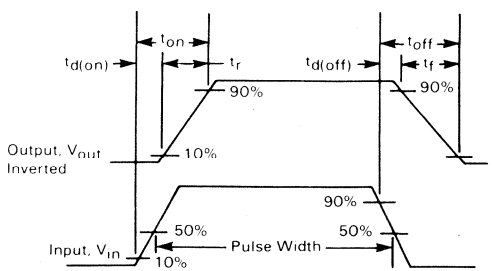


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

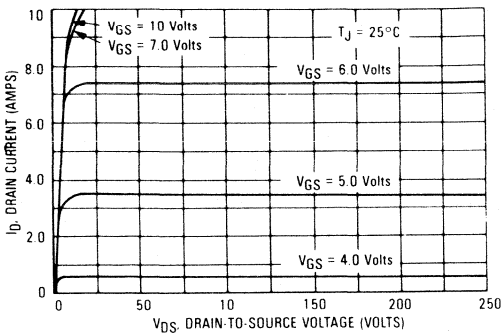


FIGURE 4 — ON-REGION CHARACTERISITCS

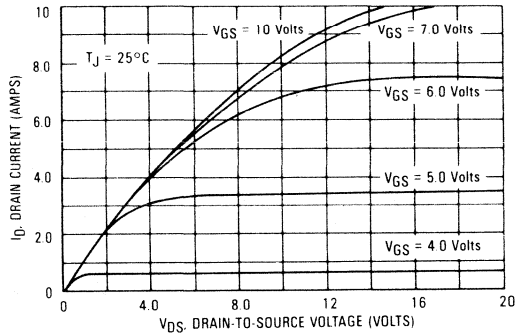


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

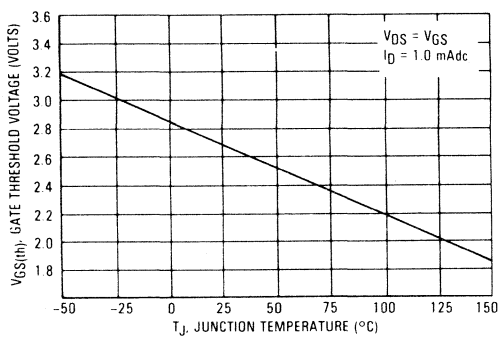


FIGURE 6 — TRANSFER CHARACTERISTICS

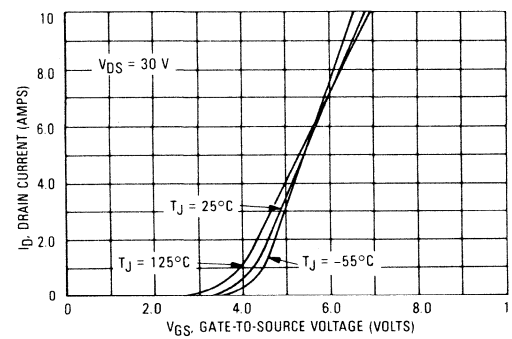


FIGURE 7 — ON-VOLTAGE versus TEMPERATURE

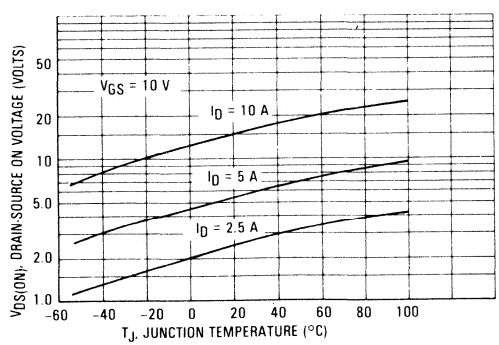
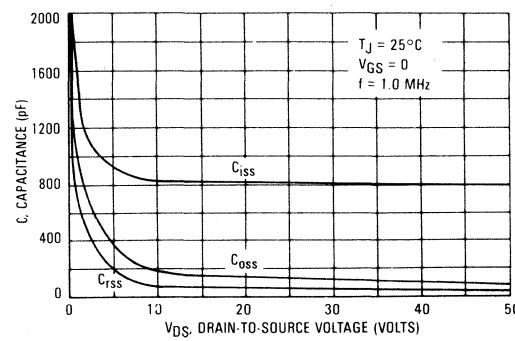


FIGURE 8 — CAPACITANCE VARIATION



3

TYPICAL CHARACTERISTICS

FIGURE 9 — ON-RESISTANCE versus DRAIN CURRENT

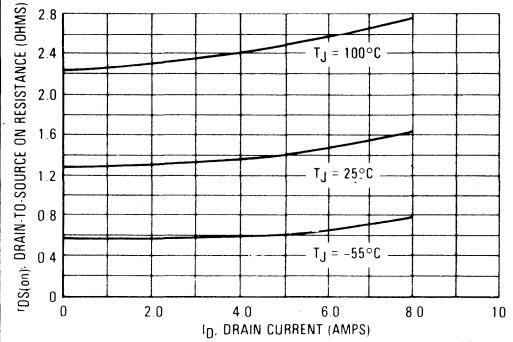
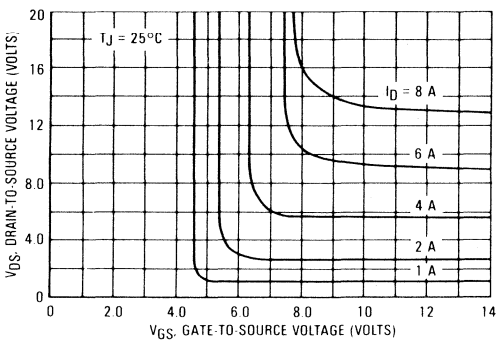


FIGURE 10 — ON-VOLTAGE VARIATION



THERMAL RESPONSE

FIGURE 11 — MTM474/MTM475

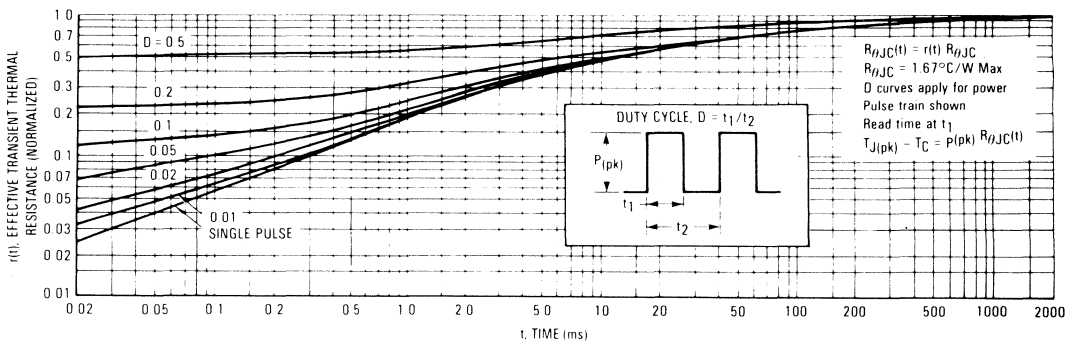
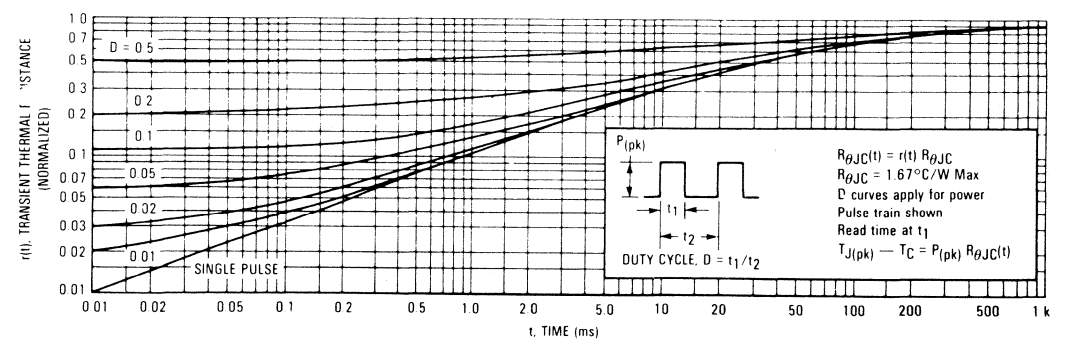


FIGURE 12 — MTP474/MTP475



SAFE OPERATING AREA INFORMATION

FIGURE 13 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

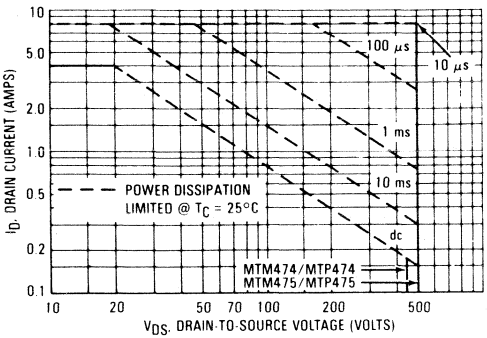
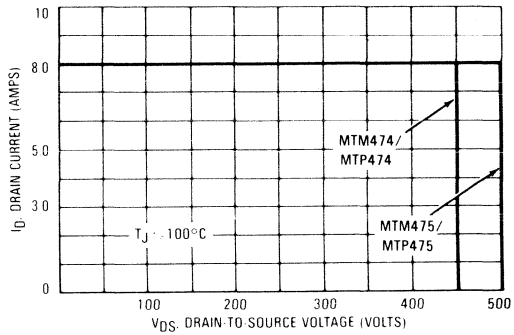


FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED

The data of Figure 13 is based on T_C = 25°C; $T_{J(pk)}$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 13 may be calculated for any case temperature with the aid of the following equation:

$$I_{D(T_C)} = I_{D(25°C)} \left[1 - \frac{T_C - 25°C}{P_D R_{\theta JC}} \right]$$

where

$I_{D(T_C)}$ = the maximum allowable current at a case temperature, T_C.

$I_{D(25°C)}$ = the maximum allowable current at a given voltage from Figure 13.

P_D = the rated power dissipation at T_C = 25°C.

$R_{\theta JC}$ = the rated steady state thermal resistance

For various pulse widths and duty cycles, substitute $R_{\theta JC(t)}$ determined from Figures 11 and 12 for $R_{\theta JC}$.

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The switching safe operating area (SOA) of Figure 14, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

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Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

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TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 15. Reversal of the drain voltage will cause current flow in the reverse direction. This diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 15 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

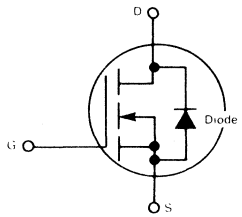


FIGURE 16 — DIODE TURN-ON TEST CIRCUIT

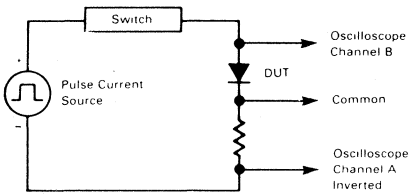


FIGURE 17 — DIODE TURN-ON WAVEFORMS

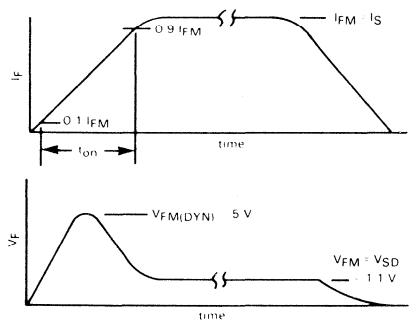


FIGURE 18 — REVERSE RECOVERY CHARACTERISTIC

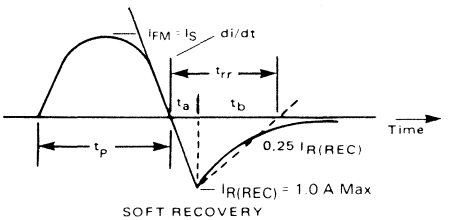
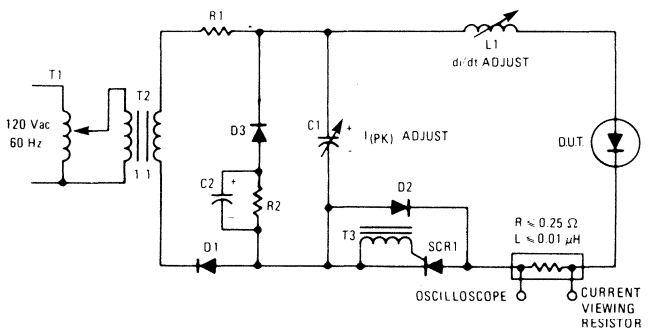


FIGURE 19 — JEDEC REVERSE RECOVERY CIRCUIT



R1 = 50 Ohms
R2 = 250 Ohms
D1 = 1N4723
D2 = 1N4001
D3 = 1N4933
SCR1 = MCR729-10
C1 = 0.5 to 50 μF
C2 ≈ 4000 μF
L1 = 1.0 - 27 μH
T1 = Variac Adjusts I(PK) and di/dt
T2 = 1:1
T3 = 1:1 (to trigger circuit)

Motorola reserves the right to make changes to any products herein to improve reliability, function or design. Motorola does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights nor the rights of others.

MTM564, MTM565
MTP564, MTP565

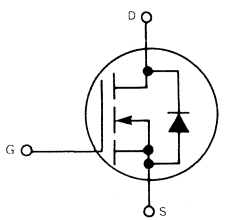
Designers Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designers Data — I_{DSS}, $V_{DS(on)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)}$ = 4.0 Volts (max)

TMOS™

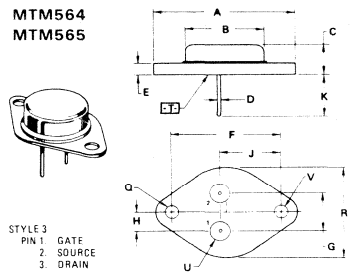


5 AMPERE

N-CHANNEL TMOS POWER FET

350 and 400 VOLTS

MTM564
MTM565

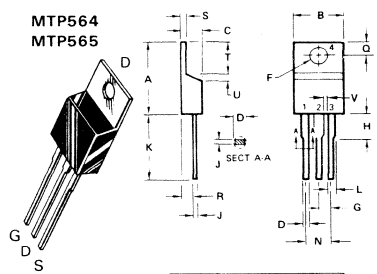


STYLE 3
PIN 1. GATE
2. SOURCE
3. DRAIN

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-3 TYPE

MTP564
MTP565



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM564 MTP564	MTM565 MTP565	Unit
Drain — Source Voltage	V_{DSS}	350	400	Vdc
Drain — Gate Voltage	V_{DGO}	350	400	Vdc
Gate — Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 5.0 10		Adc
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

TMOS is a trademark of Motorola Inc.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 mA)	MTM474/MTP474 MTM475/MTP475	$V_{(BR)DSS}$	450 500	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 BV_{DSS}, V_{GS} = 0) T_C = 100°C		I_{DSS}	— —	0.25 2.5	mAdc
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	1.5	4.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 2.0 Adc) (I_D = 4.0 Adc) (I_D = 2.0 Adc, T_J = 100°C)		$V_{DS(on)}$	— — —	4.5 9.0 8.0	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2.0 Adc)		$r_{DS(on)}$	—	2.25	Ohms
Forward Transconductance (V_{DS} = 15 V, I_D = 2.0 A)		g_{fs}	1.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)		C_{iss}	—	1200	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)		C_{oss}	—	300	pF
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)		C_{rss}	—	80	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time (V_{DS} = 25 V, I_D = 2.5 A, R_{gen} = 50 ohms)		$t_{d(on)}$	—	50	ns
Rise Time (V_{DS} = 25 V, I_D = 2.5 A, R_{gen} 50 ohms)		t_r	—	100	ns
Turn-Off Delay Time (V_{DS} = 25 V, I_D = 2.5 A, R_{gen} = 50 ohms)		$t_{d(off)}$	—	200	ns
Fall Time (V_{DS} = 25 V, I_D = 2.5 A, R_{gen} = 50 ohms)		t_f	—	100	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = 4.0 A	V_{SD}	1.1	Vdc
Forward Turn-On Time	V_{GS} = 0	t_{on}	250	ns
Reverse Recovery Time	See Figures 17 and 18	t_{rr}	420	ns

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

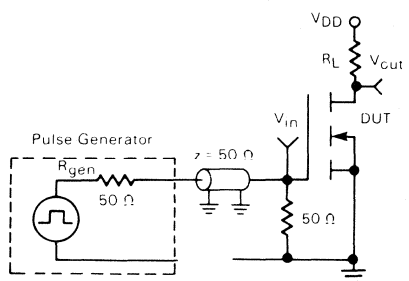
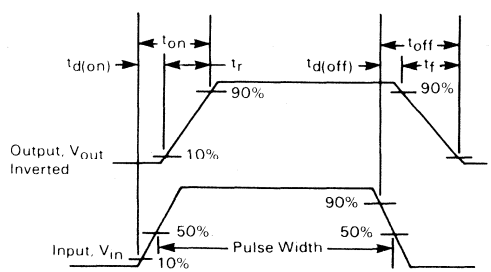


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

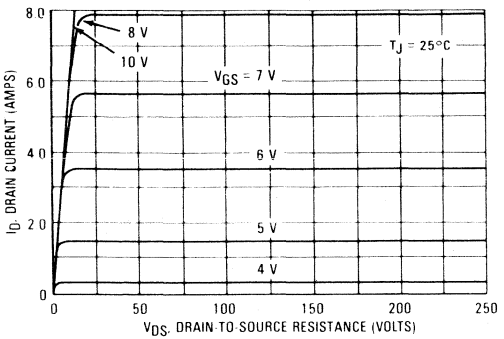


FIGURE 4 — ON-REGION CHARACTERISITCS

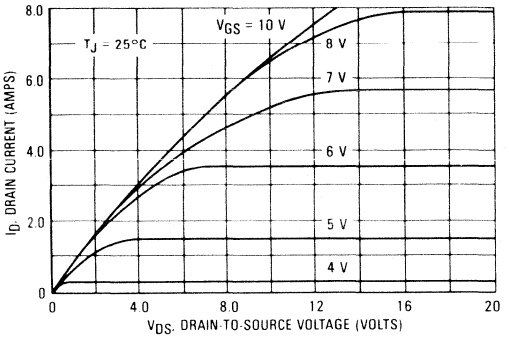


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

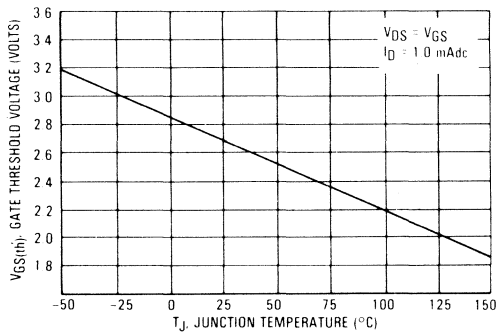


FIGURE 6 — TRANSFER CHARACTERISTICS

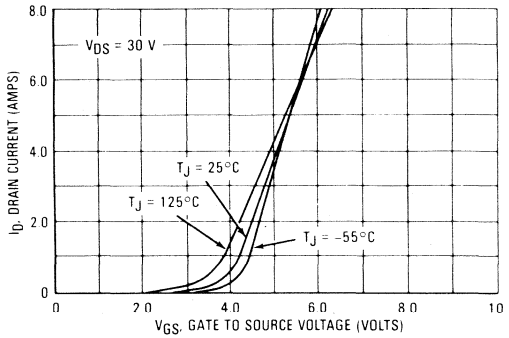


FIGURE 7 — ON-VOLTAGE versus TEMPERATURE

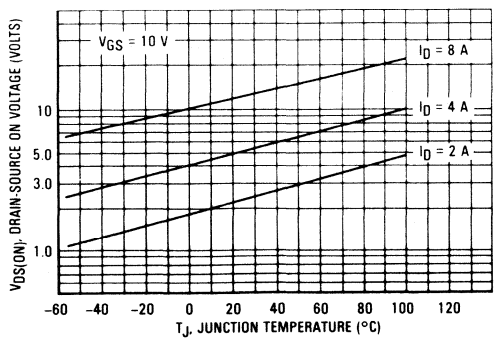
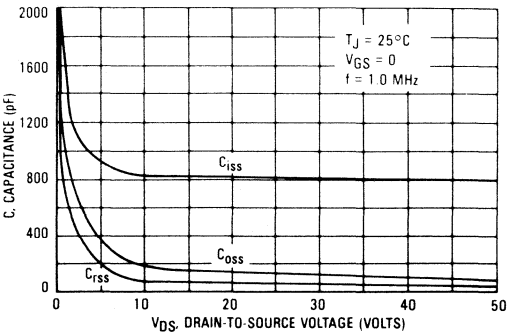


FIGURE 8 — CAPACITANCE VARIATION



3

TYPICAL CHARACTERISTICS

FIGURE 9 — ON-RESISTANCE versus DRAIN CURRENT

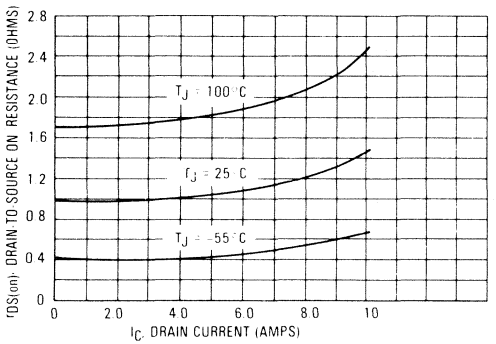
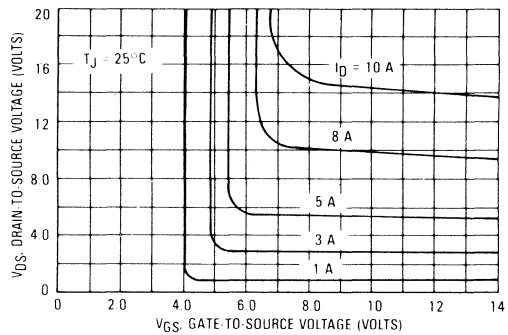


FIGURE 10 — ON-VOLTAGE VARIATION



THERMAL RESPONSE

FIGURE 11 — MTM564/MTM565

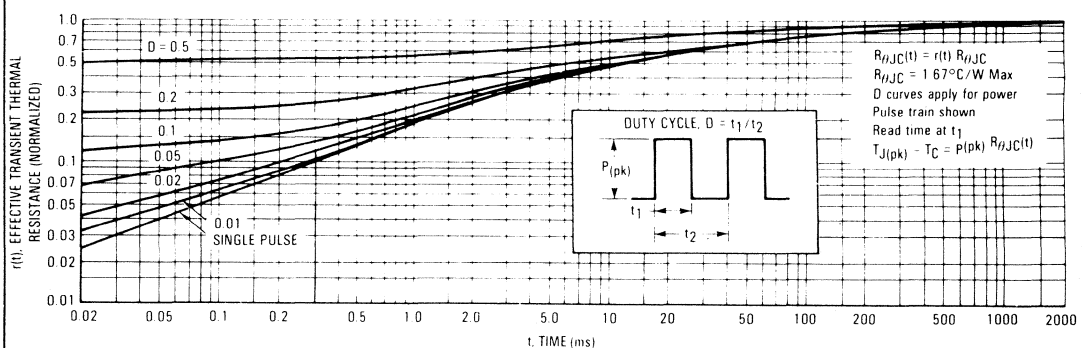
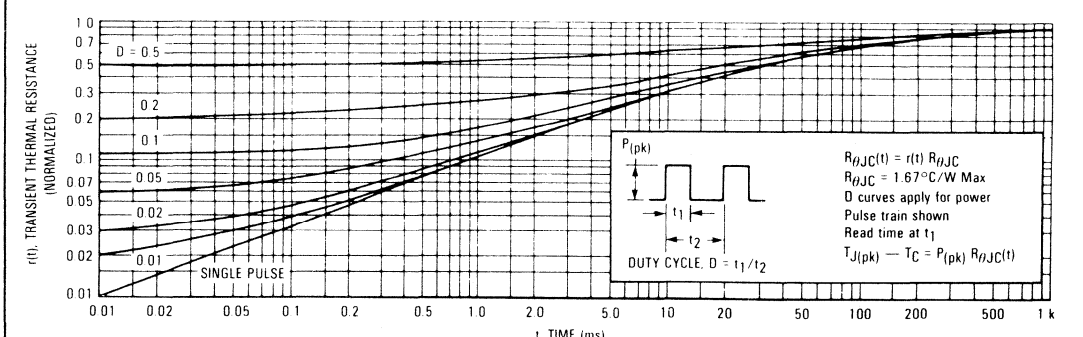


FIGURE 12 — MTP564/MTP565



SAFE OPERATING AREA INFORMATION

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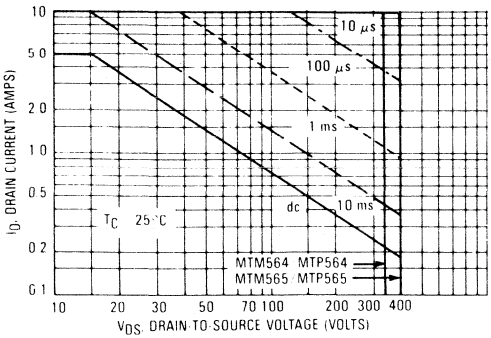

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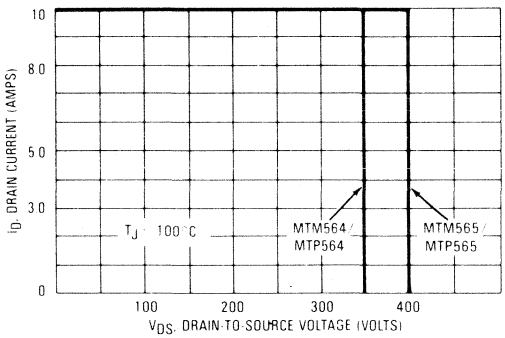

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$$I_{D(T_C)} \quad I_{D(25°C)} \left[1 - \frac{T_C - 25°C}{P_D R_{\theta JC}} \right]$$

where

$I_{D(T_C)}$ — the maximum allowable current at a case temperature, T_C.

$I_{D(25°C)}$ — the maximum allowable current at a given voltage from Figure 13.

P_D — the rated power dissipation at T_C = 25°C.

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For various pulse widths and duty cycles, substitute $R_{\theta JC(t)}$ determined from Figures 11 and 12 for $R_{\theta JC}$.

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3

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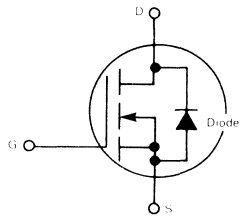


FIGURE 16 — DIODE TURN-ON TEST CIRCUIT

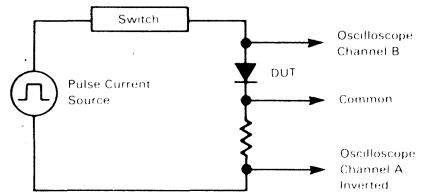


FIGURE 17 — DIODE TURN-ON WAVEFORMS

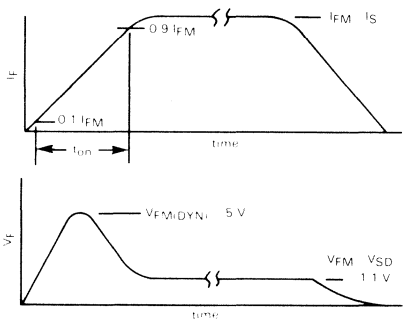


FIGURE 18 — REVERSE RECOVERY CHARACTERISTIC

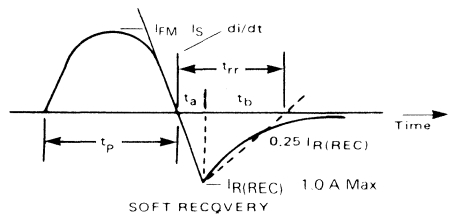
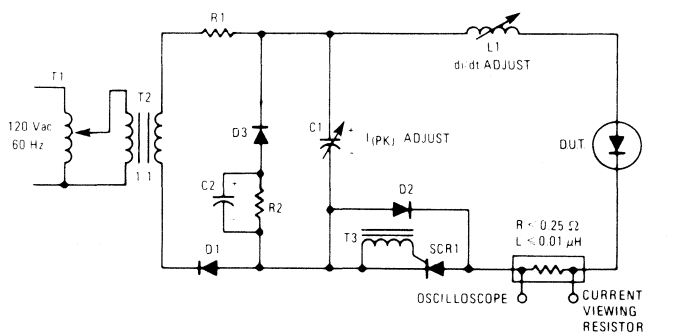


FIGURE 19 — JEDEC REVERSE RECOVERY CIRCUIT



R1 = 50 Ohms
R2 = 250 Ohms
D1 = 1N4723
D2 = 1N4001
D3 = 1N4933
SCR1 = MCR729-10
C1 = 0.5 to 50 μF
C2 = 4000 μF
L1 = 1.0 - 27 μH
T1 = Variac Adjusts I(PK) and di/dt
T2 = 1:1
T3 = 1:1 (to trigger circuit)

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MTM1224, MTM1225
MTP1224, MTP1225

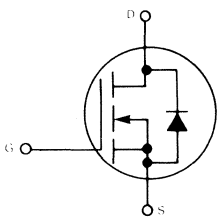
Designers Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds – Switching Times Specified at 100°C
- Designers Data – I_{DSS}, $V_{DS(on)}$ and SOA Specified at Elevated Temperature
- Rugged – SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)}$ 4.0 Volts (max)

TMOS™

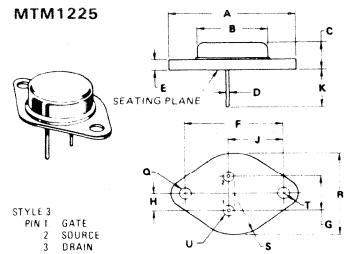


12 AMPERE

N-CHANNEL TMOS POWER FET

60 and 100 VOLTS

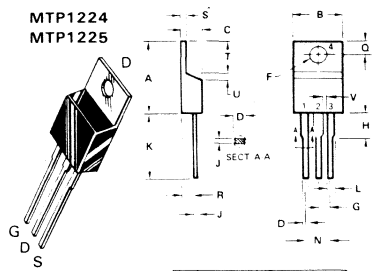
MTM1224
MTM1225



CASE 1-04
TO-3 TYPE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120

MTP1224
MTP1225



CASE 221A-02
TO-220AB

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14		0.045	

MAXIMUM RATINGS

Rating	Symbol	MTM1224 MTP1224	MTM1225 MTP1225	Unit
Drain – Source Voltage	V_{DSS}	60	100	Vdc
Drain – Gate Voltage	V_{DGO}	60	100	Vdc
Gate – Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 12 30		Adc
Gate Current – Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.

TMOS is a trademark of Motorola Inc.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 mA)	MTM1224/MTP1224 MTM1225/MTP1225	$V_{(BR)DSS}$	 60 100	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 BV_{DSS}, V_{GS} = 0) T_C = 100°C		I_{DSS}	 — —	 0.25 2.5	mAdc
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	1.5	4.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 6.0 Adc) (I_D = 12 Adc) (I_D = 6.0 Adc, T_C = 100°C)		$V_{DS(on)}$	 — — —	 1.5 3.0 2.5	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 6.0 Adc)		$r_{DS(on)}$	—	0.25	Ohms
Forward Transconductance (V_{DS} = 10 V, I_D = 6.0 A)		g_{fs}	3.0	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)		C_{iss}	—	1200	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)		C_{oss}	—	500	pF
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)		C_{rss}	—	120	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time (V_{DS} = 25 V, I_D = 2.5 A, R_{gen} = 50 ohms)		$t_{d(on)}$	—	50	ns
Rise Time (V_{DS} = 25 V, I_D = 2.5 A, R_{gen} 50 ohms)		t_r	—	100	ns
Turn-Off Delay Time (V_{DS} = 25 V, I_D = 2.5 A, R_{gen} = 50 ohms)		$t_{d(off)}$	—	200	ns
Fall Time (V_{DS} = 25 V, I_D = 2.5 A, R_{gen} = 50 ohms)		t_f	—	100	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = 12 A	V_{SD}	1.3	Vdc
Forward Turn-On Time	V_{GS} = 0	t_{on}	250	ns
Reverse Recovery Time	See Figures 17 and 18	t_{rr}	325	ns

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

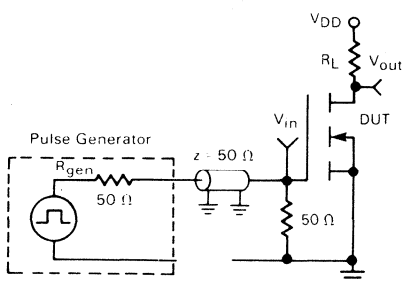
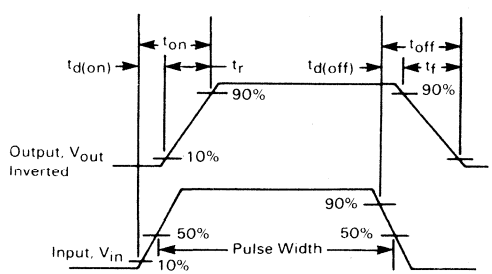


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

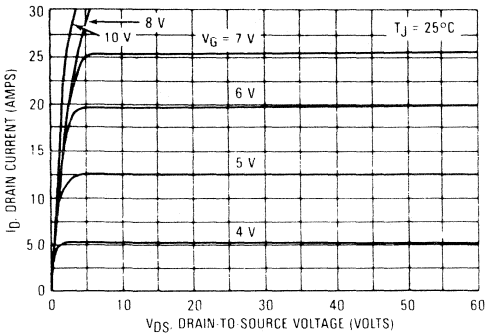


FIGURE 4 — ON-REGION CHARACTERISITCS

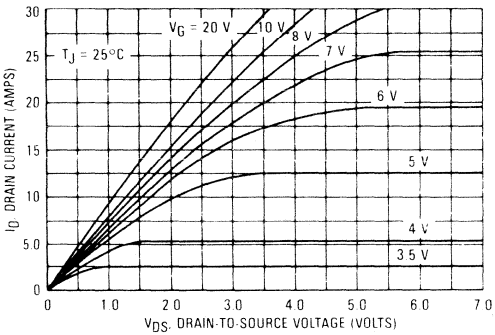


FIGURE 5 — GATE THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

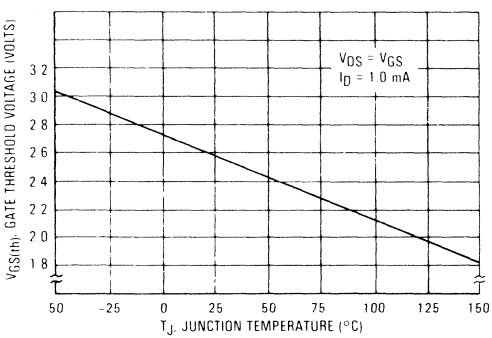


FIGURE 6 — TRANSFER CHARACTERISTICS

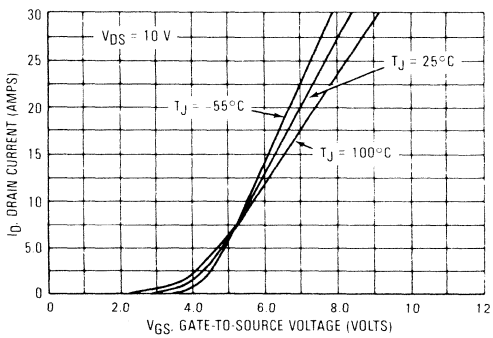


FIGURE 7 — ON-VOLTAGE versus TEMPERATURE

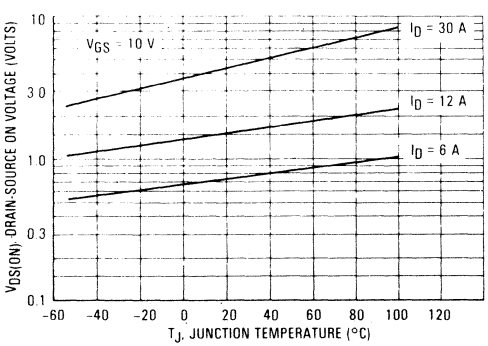
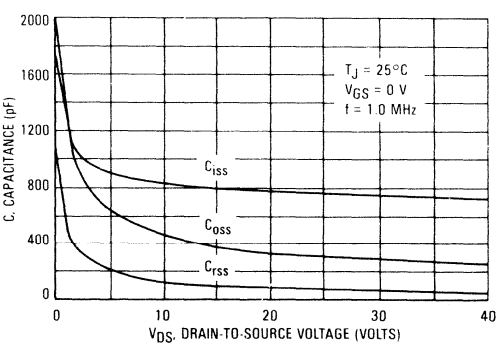


FIGURE 8 — CAPACITANCE VARIATION



3

TYPICAL CHARACTERISTICS

FIGURE 9 — ON-RESISTANCE versus DRAIN CURRENT

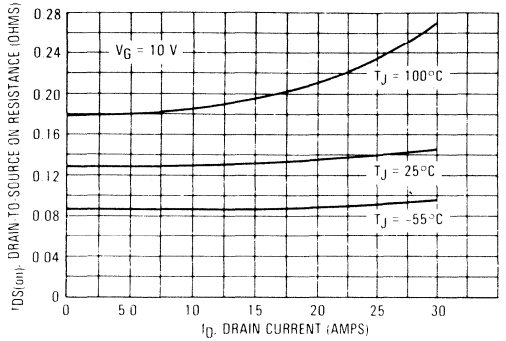
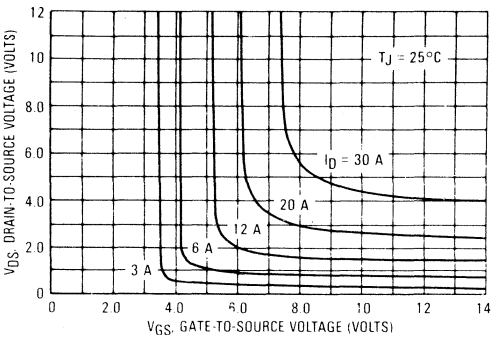


FIGURE 10 — ON-VOLTAGE VARIATION



THERMAL RESPONSE

FIGURE 11 — MTM1224/MTM1225

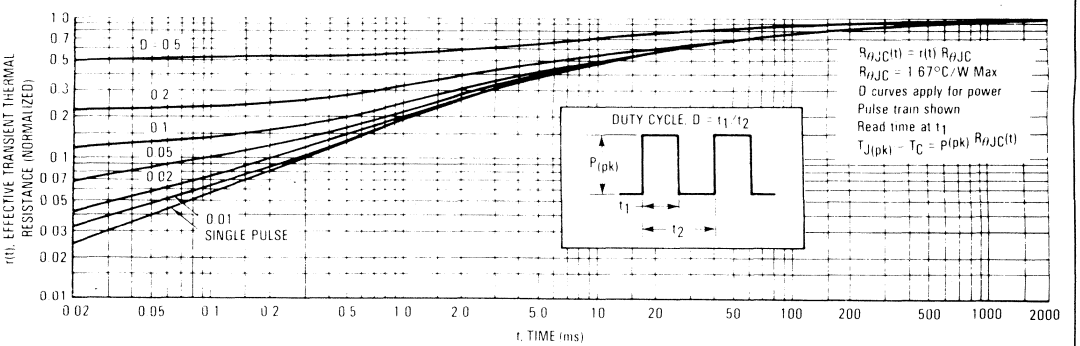
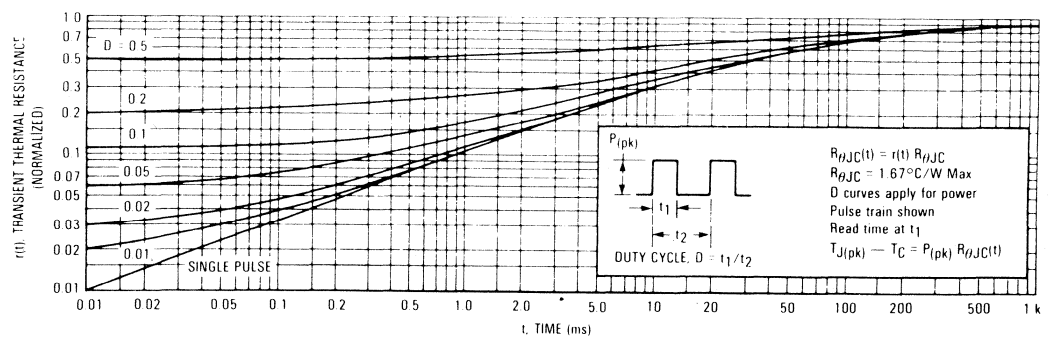


FIGURE 12 — MTP1224/MTP1225



SAFE OPERATING AREA INFORMATION

FIGURE 13 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

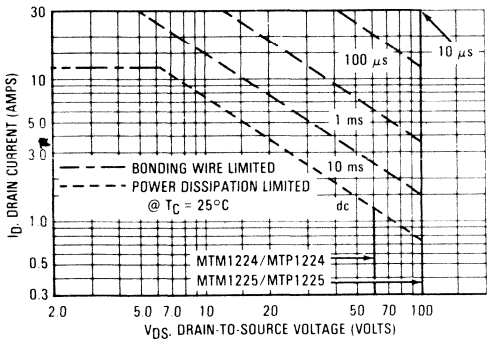
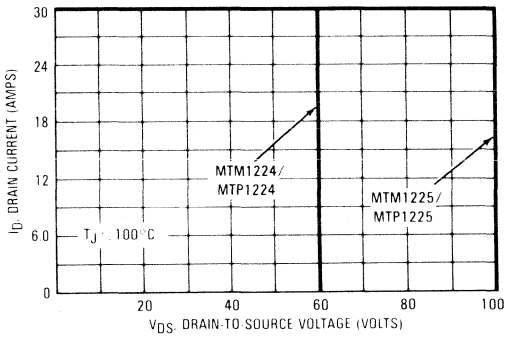


FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED

The data of Figure 13 is based on $T_C = 25°C$; $T_{J(pk)}$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 13 may be calculated for any case temperature with the aid of the following equation.

$$I_{D(T_C)} = I_{D(25°C)} \left[1 - \frac{T_C - 25°C}{P_D R_{\theta JC}} \right]$$

where

$I_{D(T_C)}$ = the maximum allowable current at a case temperature, T_C

$I_{D(25°C)}$ = the maximum allowable current at a given voltage from Figure 13

P_D = the rated power dissipation at $T_C = 25°C$

$R_{\theta JC}$ = the rated steady state thermal resistance

For various pulse widths and duty cycles, substitute $R_{\theta JC(t)}$ determined from Figures 11 and 12 for $R_{\theta JC}$.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 14, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 500 mA. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ±20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

3

TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 15. Reversal of the drain voltage will cause current flow in the reverse direction. This diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 15 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

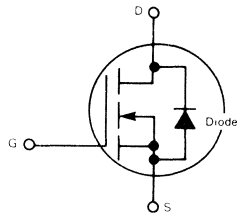


FIGURE 16 — DIODE TURN-ON TEST CIRCUIT

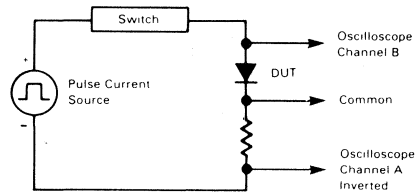


FIGURE 17 — DIODE TURN-ON WAVEFORMS

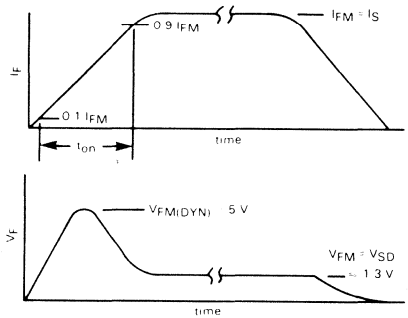


FIGURE 18 — REVERSE RECOVERY CHARACTERISTIC

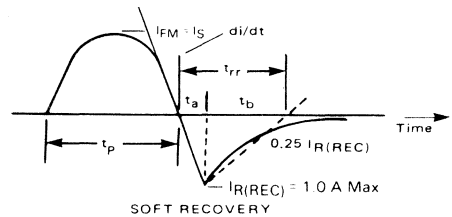
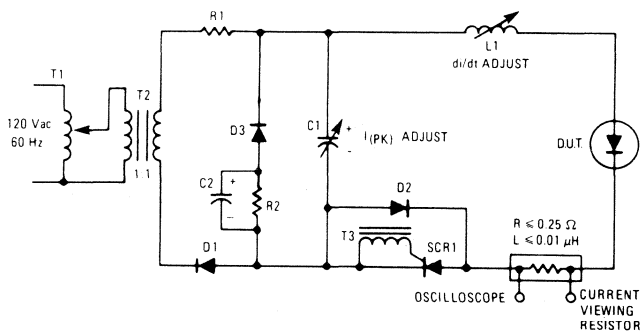


FIGURE 19 — JEDEC REVERSE RECOVERY CIRCUIT



R1 = 50 Ohms
R2 = 250 Ohms
D1 = 1N4723
D2 = 1N4001
D3 = 1N4933
SCR1 = MCR729-10
C1 = 0.5 to 50 μF
C2 ≈ 4000 μF
L1 = 1.0 - 27 μH
T1 = Variac Adjusts I(PK) and di/dt
T2 = 1:1
T3 = 1:1 (to trigger circuit)

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TIP47 TIP48
TIP49 TIP50

HIGH VOLTAGE NPN SILICON POWER TRANSISTORS

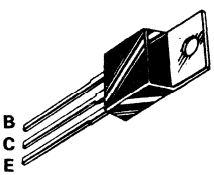
. . . designed for line operated audio output amplifier, Switchmode[1] power supply drivers and other switching applications.

- 250 V to 400 V (Min) – $V_{CEO(sus)}$
- 1 A Rated Collector Current
- Popular TO-220 Plastic Package
- TO-66 Leadform Available

1.0 AMPERE

POWER TRANSISTORS NPN SILICON

250-300-350-400 VOLTS
40 WATTS



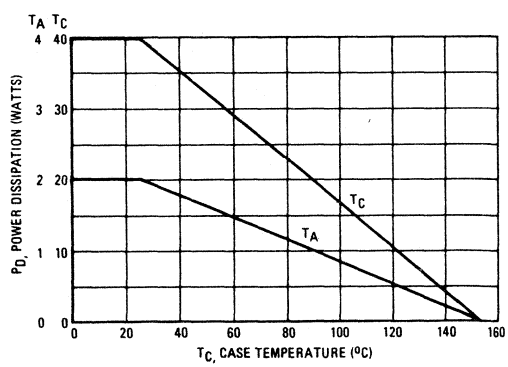
MAXIMUM RATINGS

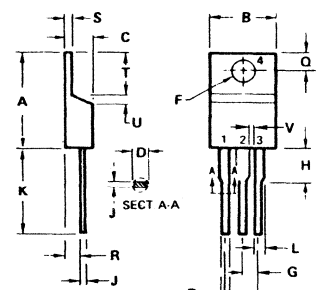
Rating	Symbol	TIP47	TIP48	TIP49	TIP50	Unit
Collector-Emitter Voltage	V_{CEO}	250	300	350	400	Vdc
Collector-Base Voltage	V_{CB}	350	400	450	500	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →				Vdc
Collector Current – Continuous Peak	I_C	← 1.0 → ← 2.0 →				Adc
Base Current	I_B	← 0.6 →				Adc
Total Power Dissipation @ T_C = 25° C Derate above 25° C	P_D	← 40 → ← 0.32 →				Watts W/°C
Total Power Dissipation @ T_A = 25° C Derate above 25° C	P_D	← 2.0 → ← 0.016 →				Watts W/°C
Unclamped Inducting Load Energy (See Figure 8)	E	← 20 →				mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	TIP47	$V_{CEO(sus)}$	250	–	Vdc
	TIP48		300	–	
	TIP49		350	–	
	TIP50		400	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 150 Vdc, I_B = 0)	TIP47		–	1.0	
(V_{CE} = 200 Vdc, I_B = 0)	TIP48		–	1.0	
(V_{CE} = 250 Vdc, I_B = 0)	TIP49		–	1.0	
(V_{CE} = 300 Vdc, I_B = 0)	TIP50		–	1.0	
Collector Cutoff Current		I_{CES}			mAdc
(V_{CE} = 350 Vdc, V_{BE} = 0)	TIP47		–	1.0	
(V_{CE} = 400 Vdc, V_{BE} = 0)	TIP48		–	1.0	
(V_{CE} = 450 Vdc, V_{BE} = 0)	TIP49		–	1.0	
(V_{CE} = 500 Vdc, V_{BE} = 0)	TIP50		–	1.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 0.3 Adc, V_{CE} = 10 Vdc)			30	150	
(I_C = 1.0 Adc, V_{CE} = 10 Vdc)			10	–	
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc)		$V_{CE(sat)}$	–	1.0	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 2.0 MHz)		f_T	10	–	MHz
Small-Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	–	–

(1) Pulse Test: Pulsewidth ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – SWITCHING TIME EQUIVALENT CIRCUIT

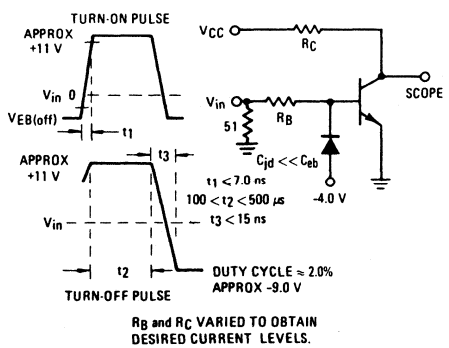


FIGURE 3 – TURN-ON TIME

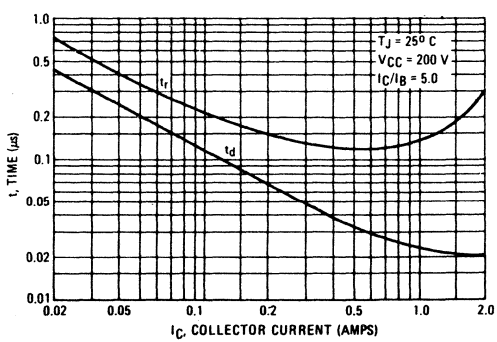


FIGURE 4 – THERMAL RESPONSE

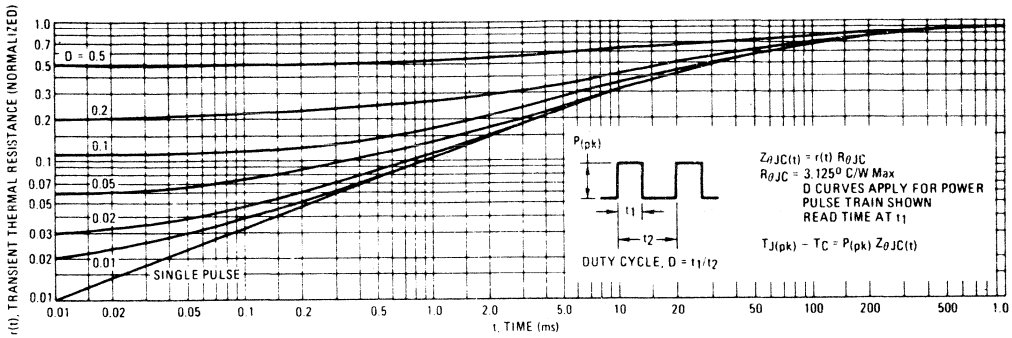
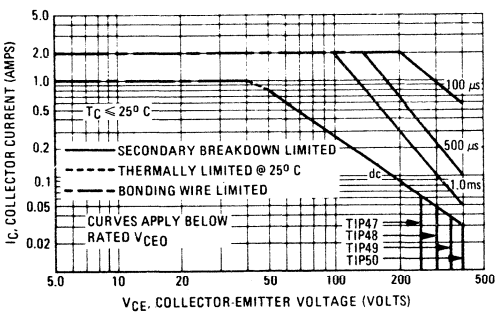


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

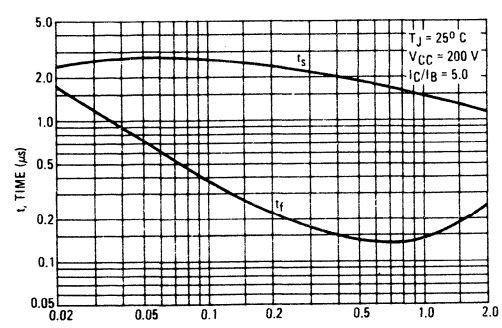
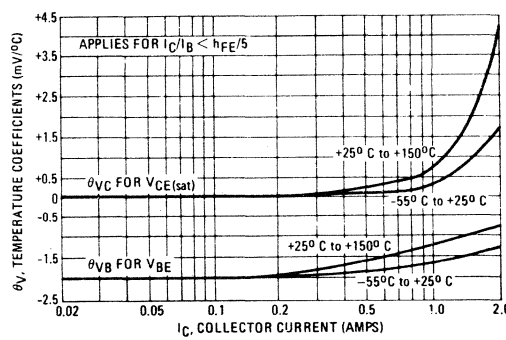


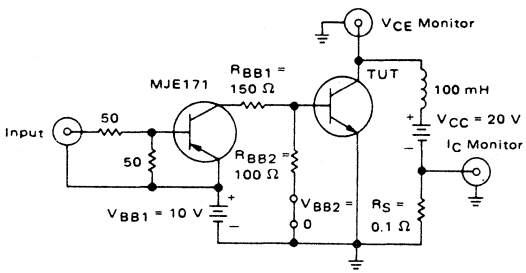
FIGURE 7 – TEMPERATURE COEFFICIENTS



3

FIGURE 8 – INDUCTIVE LOAD SWITCHING

Test Circuit



Note A: Input pulse width is increased until I_{CM} = 0.63 A.

Voltage and Current Waveforms

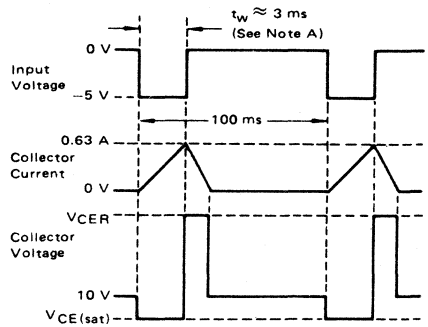


FIGURE 9 – DC CURRENT GAIN

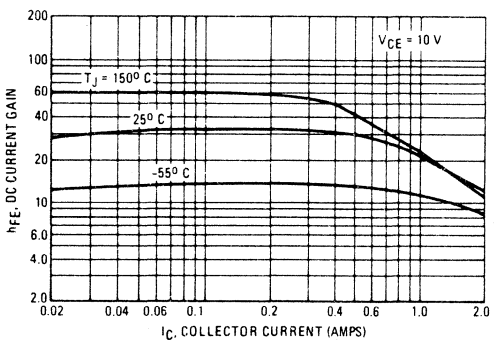
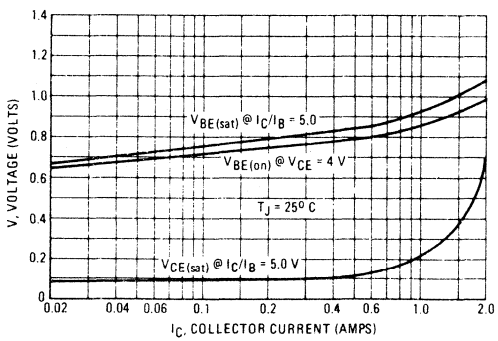


FIGURE 10 – "ON" VOLTAGES



2N3773 (NPN)
2N6609 (PNP)

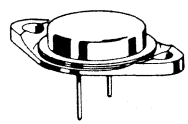
COMPLEMENTARY SILICON POWER TRANSISTORS

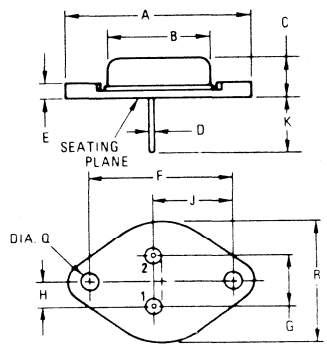
The 2N3773 and 2N6609 are EPI-BASE▲ power transistors designed for high power audio, disk head positioners and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc to dc converters or inverters.

- High Safe Operating Area (100% Tested)
  150 W @ 100 V
- Completely Characterized for Linear Operation
- High DC Current Gain and Low Saturation Voltage
  h_{fe} = 15 (Min) @ 8 A, 4 V
  $V_{CE(sat)}$ = 1.4 V (Max) @ I_C = 8 A, I_B = 0.8 A
- For Low Distortion Complementary Designs

16 AMPERE
COMPLEMENTARY
POWER TRANSISTORS

140 VOLTS
150 WATTS





STYLE 1
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-03
TO-3

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector Emitter Voltage	V_{CEO}	140	Vdc
Collector-Emitter Voltage	V_{CEX}	160	Vdc
Collector-Base Voltage	V_{CBO}	160	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector Current – Continuous – Peak (1)	I_C	16 30	Adc
Base Current – Continuous – Peak (1)	I_B	4 15	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.855	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)				
*Collector-Emitter Breakdown Voltage (I_C = 0.2 Adc, I_B = 0)	$V_{CEO(sus)}$	140	–	Vdc
*Collector-Emitter Sustaining Voltage (I_C = 0.1 Adc, $V_{BE(off)}$ = 1.5 Vdc, R_{BE} = 100 Ohms)	$V_{CEX(sus)}$	160	–	Vdc
Collector-Emitter Sustaining Voltage (I_C = 0.2 Adc, R_{BE} = 100 Ohms)	$V_{CER(sus)}$	150	–	Vdc
*Collector Cutoff Current (V_{CE} = 120 Vdc, I_B = 0)	I_{CEO}	–	10	mAdc
*Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	– –	2 10	mAdc
Collector Cutoff Current (V_{CB} = 140 Vdc, I_E = 0)	I_{CBO}	–	2	mAdc
*Emitter Cutoff Current (V_{BE} = 7 Vdc, I_C = 0)	I_{EBO}	–	5	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain *(I_C = 8 Adc, V_{CE} = 4 Vdc) (I_C = 16 Adc, V_{CE} = 4 Vdc)	h_{FE}	 15 5	 60	–
Collector-Emitter Saturation Voltage *(I_C = 8 Adc, I_B = 800 mAdc) (I_C = 16 Adc, I_B = 3.2 Adc)	$V_{CE(sat)}$	 – –	 1.4 4	Vdc
*Base-Emitter On Voltage (I_C = 8 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	–	2.2	Vdc
DYNAMIC CHARACTERISTICS				
Magnitude of Common-Emitter Small-Signal, Short-Circuit, Forward Current Transfer Ratio (I_C = 1 A, f = 50 kHz)	$\|h_{fe}\|$	4	–	–
*Small-Signal Current Gain (I_C = 1 Adc, V_{CE} = 4 Vdc, f = 1 kHz)	h_{fe}	40	–	–
SWITCHING CHARACTERISTICS				
Second Breakdown Collector Current with Base Forward Biased t = 1 s (non-repetitive), V_{CE} = 100 V, See Figure 12	$I_{S/b}$	1.5	–	Adc

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

*Indicates JEDEC Registered Data

NPN

FIGURE 1 – DC CURRENT GAIN

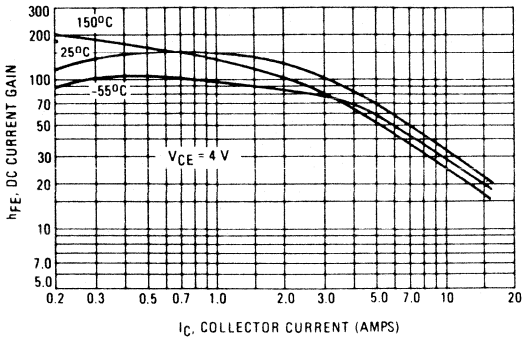


FIGURE 3 – COLLECTOR SATURATION REGION

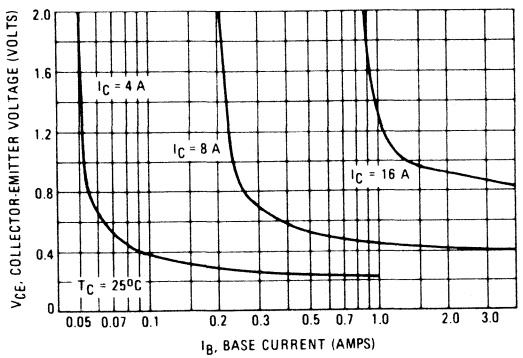
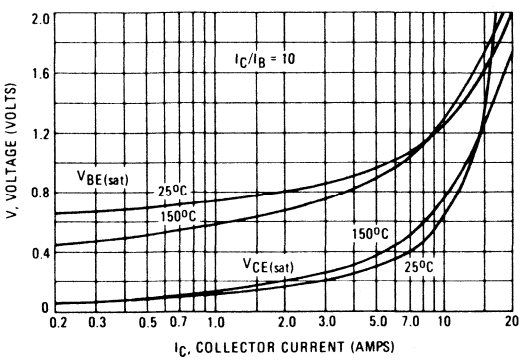


FIGURE 5 – "ON" VOLTAGE



PNP

FIGURE 2 – DC CURRENT GAIN

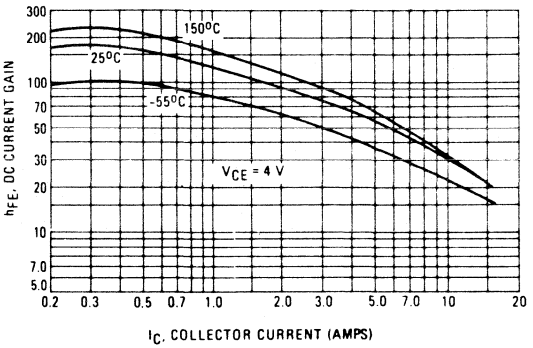


FIGURE 4 – COLLECTOR SATURATION REGION

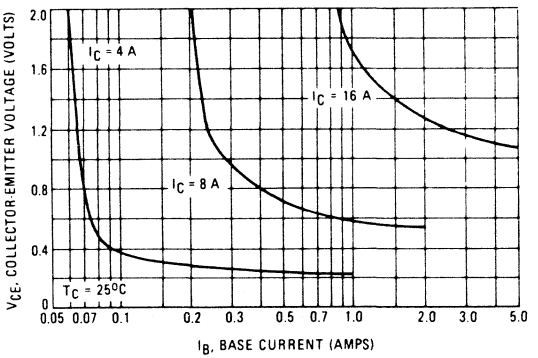
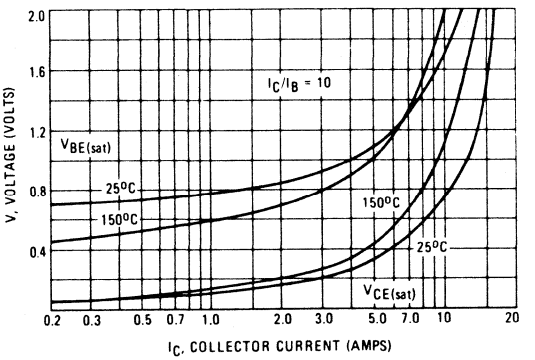


FIGURE 6 – "ON" VOLTAGE



3

FIGURE 7 – TURN-ON SWITCHING TIMES – 2N3773, 2N6609

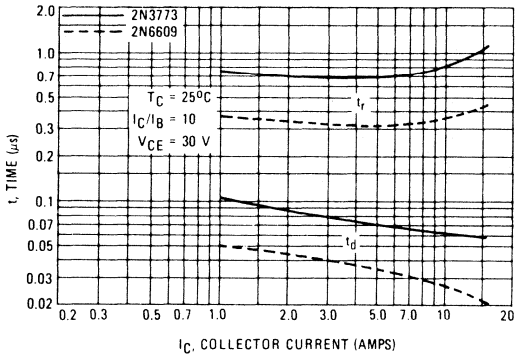


FIGURE 8 – TURN-OFF SWITCHING TIMES – 2N3773, 2N6609

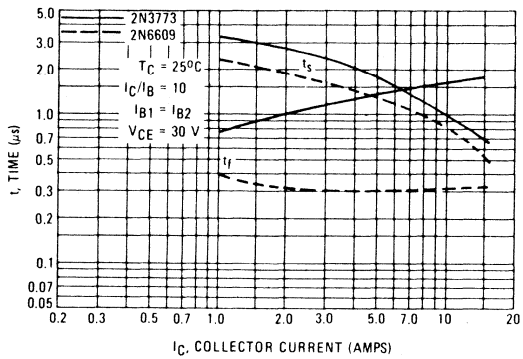


FIGURE 9 – CURRENT-GAIN – BANDWIDTH PRODUCT – 2N3773, 2N6609

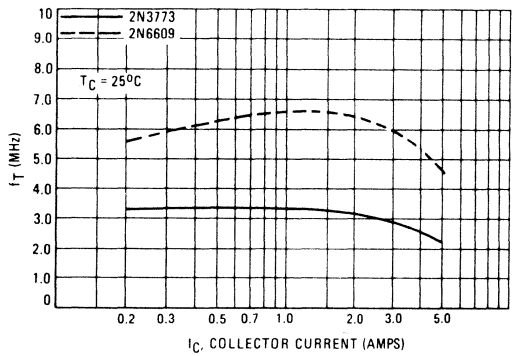


FIGURE 10 – CAPACITANCES – 2N3773, 2N6609

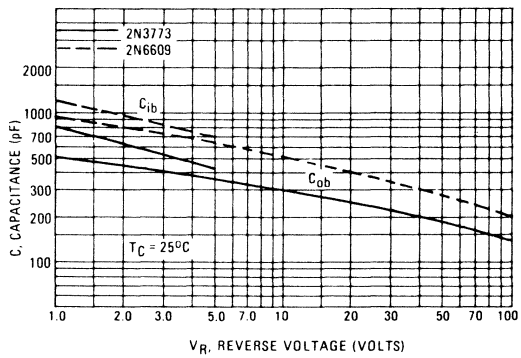


FIGURE 11 – THERMAL RESPONSE – 2N3773, 2N6609

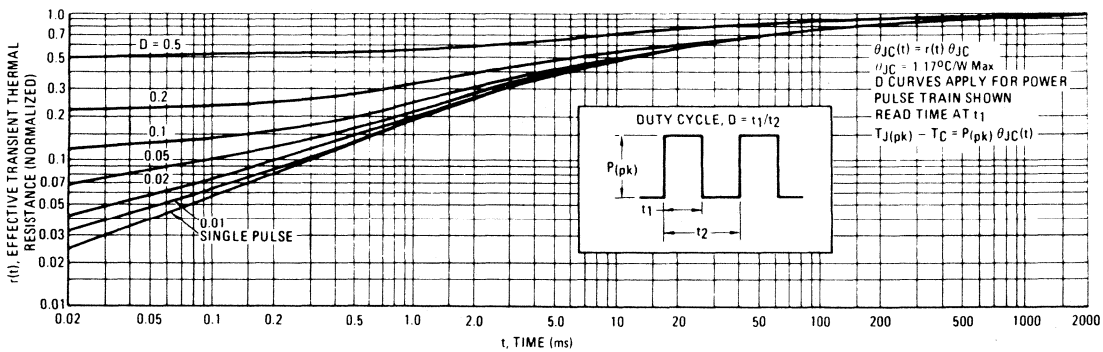
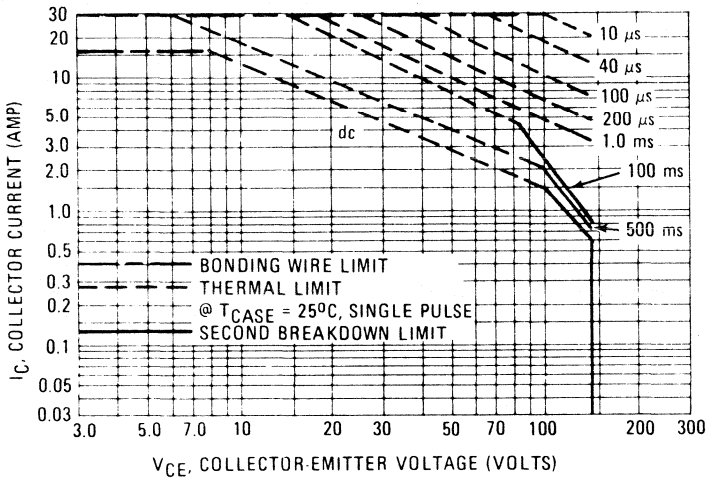


FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

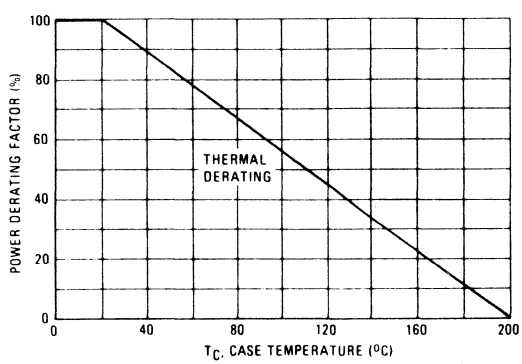


There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^{\circ}C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown (see AN-415A).

3

FIGURE 13 – POWER DERATING



NPN	PNP
2N6486	**2N6489**
2N6487	**2N6490**
2N6488	**2N6491**

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

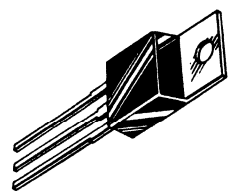
. . . designed for use in general-purpose amplifier and switching applications.

- DC Current Gain Specified to 15 Amperes
  h_{FE} = 20–150 @ I_C = 5.0 Adc
  = 5.0 (Min) @ I_C = 15 Adc
- Collector-Emitter Sustaining Voltage –
  $V_{CEO\ (sus)}$ = 40 Vdc (Min) – 2N6486, 2N6489
  = 60 Vdc (Min) – 2N6487, 2N6490
  = 80 Vdc (Min) – 2N6488, 2N6491
- High Current Gain – Bandwidth Product
  f_T = 5.0 MHz (Min) @ I_C = 1.0 Adc
- TO-220AB Compact Package
- TO-66 Leadform Also Available

15 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

40-60-80 VOLTS
75 WATTS



*MAXIMUM RATINGS

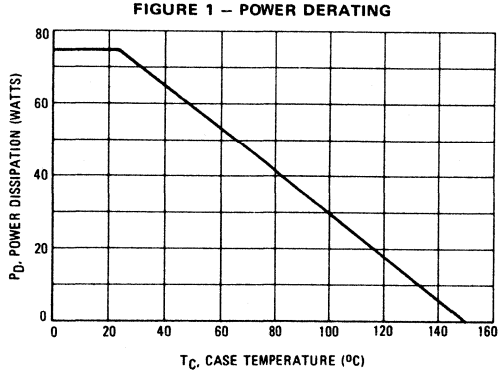
Rating	Symbol	2N6486 2N6489	2N6487 2N6490	2N6488 2N6491	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	50	70	90	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current – Continuous	I_C	15			Adc
Base Current	I_B	5.0			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			°C

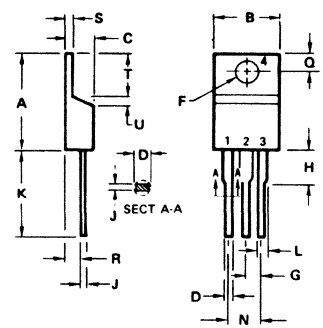
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

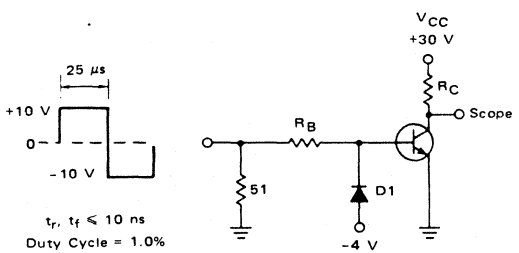
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N6486, 2N6489		40	–	
	2N6487, 2N6490		60	–	
	2N6588, 2N6491		80	–	
Collector-Emitter Sustaining Voltage (1)		V_{CEX}			Vdc
(I_C = 200 mAdc, V_{BE} = 1.5 Vdc)	2N6486, 2N6489		50	–	
	2N6487, 2N6490		70	–	
	2N6488, 2N6491		90	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 20 Vdc, I_B = 0)	2N6486, 2N6489		–	1.0	
(V_{CE} = 30 Vdc, I_B = 0)	2N6487, 2N6490		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N6488, 2N6491		–	1.0	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = 45 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6486, 2N6489		–	500	
(V_{CE} = 65 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6487, 2N6490		–	500	
(V_{CE} = 85 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6488, 2N6491		–	500	
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6486, 2N6489		–	5.0	mAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6487, 2N6490		–	5.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6488, 2N6491		–	5.0	
Emitter Cutoff Current		I_{EBO}	–	1.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)			20	150	
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)			5.0	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 0.5 Adc)			–	1.3	
(I_C = 15 Adc, I_B = 5.0 Adc)			–	3.5	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)			–	1.3	
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)			–	3.5	
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (2)		f_T	5.0	–	MHz
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 1.0 MHz)					
Small-Signal Current Gain		h_{fe}	25	–	–
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)					

*Indicates JEDEC Registered Data.

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2)$f_T = |h_{fe}| \bullet f_{test}$.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

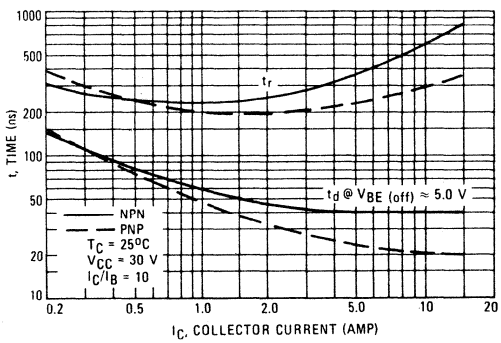


t_r, t_f ≤ 10 ns
Duty Cycle = 1.0%

R_B and R_C varied to obtain desired current levels.
For PNP reverse all polarities.

D1 must be fast recovery type, e.g.;
MBD5300 used above I_B ≈ 100 mA
MSD6100 used below I_B ≈ 100 mA

FIGURE 3 – TURN-ON TIME



3

FIGURE 4 – THERMAL RESPONSE

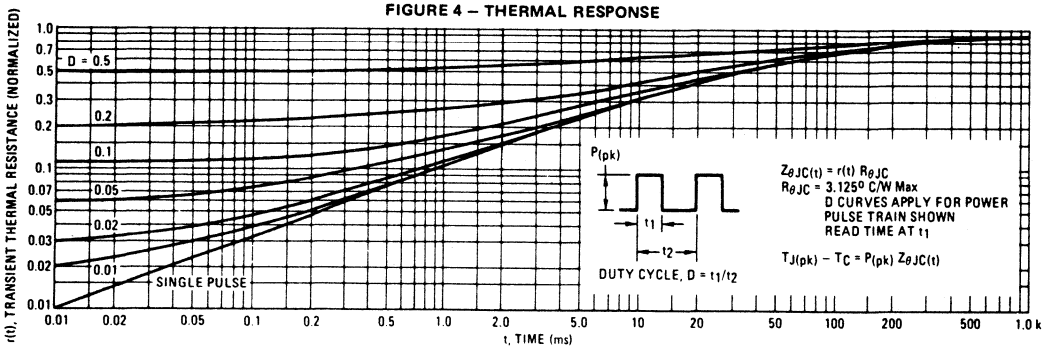
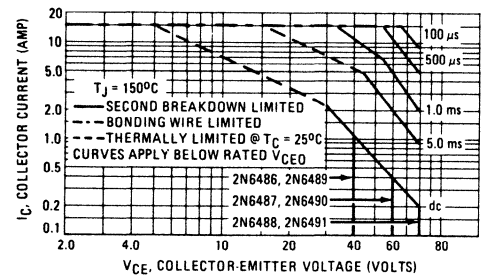


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{o}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^{o}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown (see AN-415A).

FIGURE 6 – TURN-OFF TIME

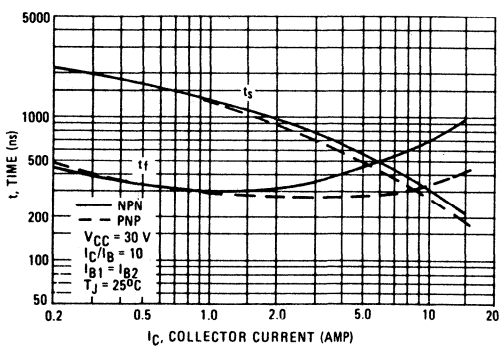
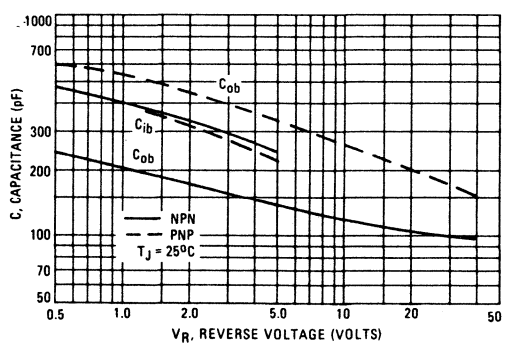


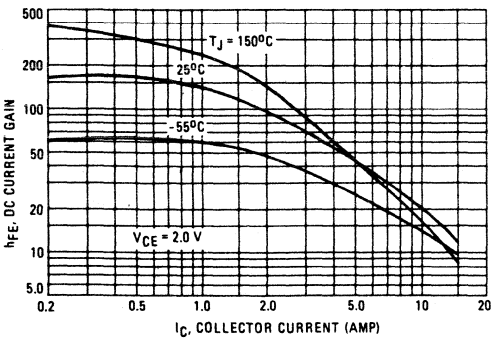
FIGURE 7 – CAPACITANCES



NPN
2N6486, 2N6487, 2N6488

PNP
2N6489, 2N6490, 2N6491

FIGURE 8 – DC CURRENT GAIN



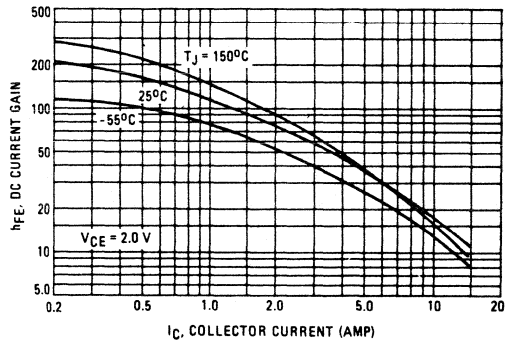
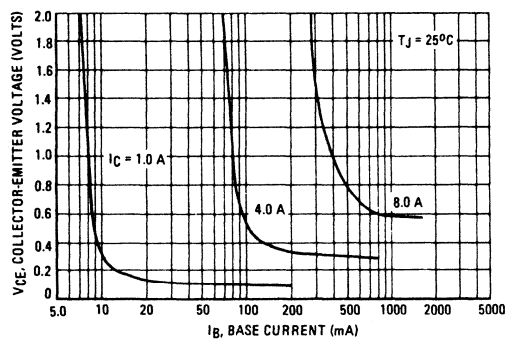


FIGURE 9 – COLLECTOR SATURATION REGION



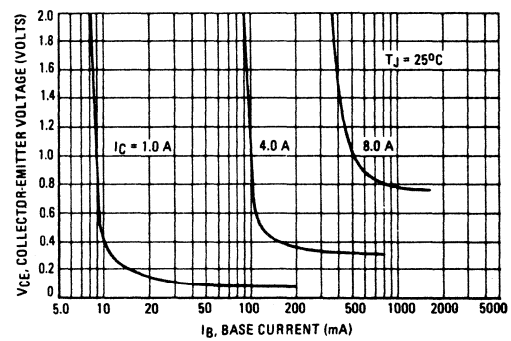
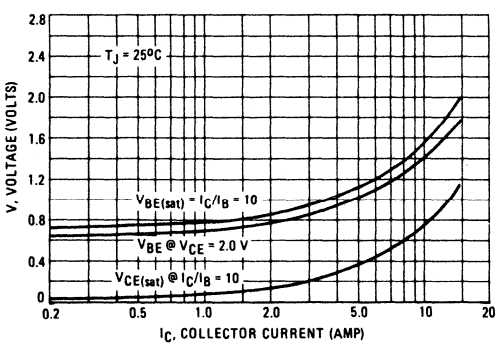
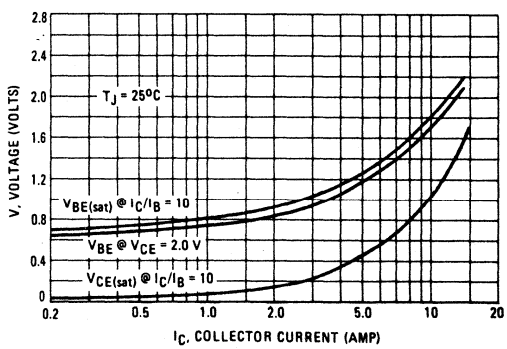


FIGURE 10 – "ON" VOLTAGES



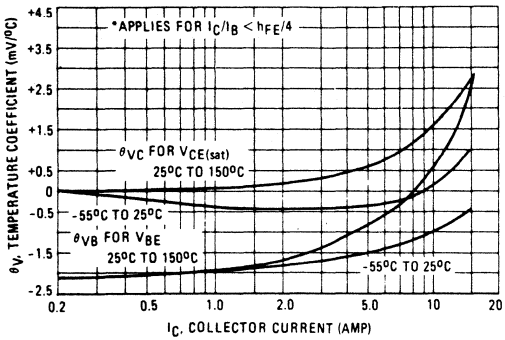


3

NPN
2N6486, 2N6487, 2N6488

PNP
2N6489, 2N6490, 2N6491

FIGURE 11 – TEMPERATURE COEFFICIENTS



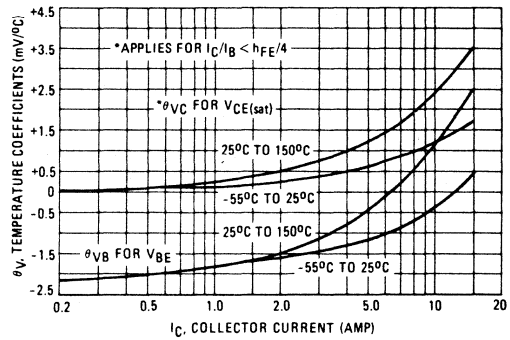
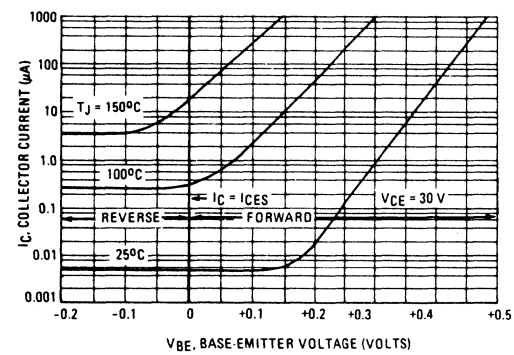


FIGURE 12 – COLLECTOR CUTOFF REGION



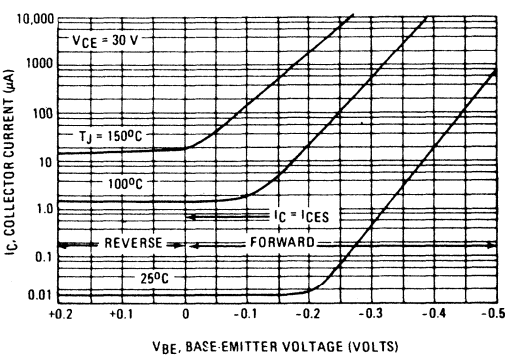
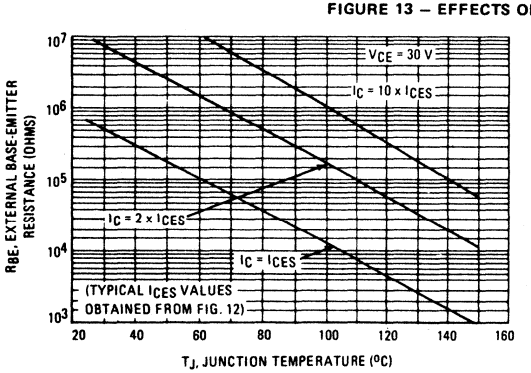
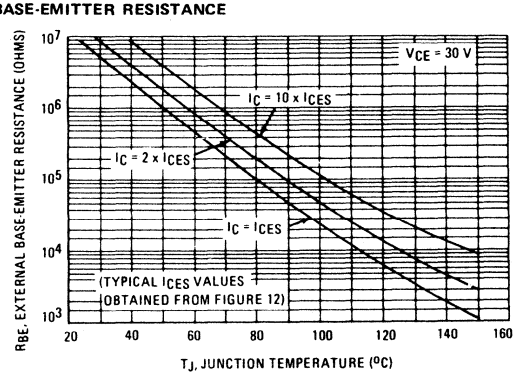


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE

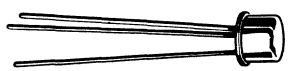




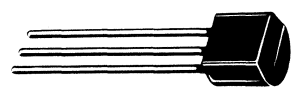
SECTION 4
SMALL SIGNAL BIPOLAR TRANSISTORS

- **Metal and plastic encapsulated transistors for general purpose applications and applications requiring:**
  - **low noise/high H_{FE} linearity;**
  - **high frequency;**
  - **high voltage;**
  - **high current.**

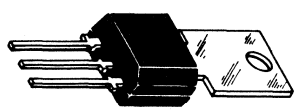
Section 4—Packages



TO 39



TO 92



Case 306.04

4 SMALL SIGNAL BIPOLAR TRANSISTORS

General Purpose Transistors

Device	Designation	H_{FE} @ (min.)	I_C mA	V_{CE} V	I_C (cont.) mA	BV_{CEO} V	Polarity	Package	Page
BC237, 238, 239	Complementary Transistors	120-380	2	5	100	20-45	NPN	TO-92	4-3
BC307, 308, 309			2	5	100	20-45	PNP	TO-92	4-7
BC546, 547, 548	Complimentary Transistors	120-420	2	5	100	30-65	NPN	TO-92	4-50
BC556, 557, 558			2	5	100	30-65	PNP	TO-92	4-63
BF257, 258, 259	Video O/P Transistors	25	30	10	100	160-300	NPN	TO-39	4-92
MPS A13, A14	Darlington Transistors	10K-20K	100	5	300	30	NPN	TO-92	4-116
MPS A16, A17	Switching Transistors	200	5	10	100	40	NPN	TO-92	4-119
MPS A62, A63, A64	Darlington Transistors	10K-20K	100	5	300	20-30	PNP	TO-92	4-121
MPS L01	High Voltage Transistor	50	10	5	150	120	NPN	TO-92	4-125

Low Noise/Good H_{FE} Linearity Transistors

Device	Designation	H_{FE} @ (min.)	I_C mA	V_{CE} V	I_C (cont.) mA	BV_{CEO} V	Polarity	Package	Page
BC413, 414	Amplifier Transistors	180-380	2	5	100	30-45	NPN	TO-92	4-20
BC415, 416	Amplifier Transistors	180-380	2	5	100	30-45	PNP	TO-92	4-27
BC549, 550	Amplifier Transistors	180-380	2	5	100	30-45	NPN	TO-92	4-56
BC559, 560	Amplifier Transistors	100-380	2	5	100	30-45	PNP	TO-92	4-69
BC650,S – 651,S	Amplifier Transistors	380-680	2	5	200	30-45	NPN	TO-92	4-76

High Frequency Transistors

Device	Designation	H_{FE} @ (min.)	I_C mA	V_{CE} V	I_C (cont.) mA	BV_{CEO} V	Polarity	Package	Page
BF199	TV/IF Amplifier Transistor	40	7	10	100	25	NPN	TO-92	4-82
BF240, 241	AM/FM Amplifier Transistors	36-67	1	10	25	40	NPN	TO-92	4-85
BF254, 255	AM/FM Amplifier Transistors	35-100	1	10	100	20	NPN	TO-92	4-89
BF491, 492, 493	High Voltage Video Transistors	40	10	10	500	200-300	PNP	TO-92	4-94
BF506	VHF Oscillator/Mixer Transistor	20	3	10	50	35	PNP	TO-92	4-97
BF509	VHF Amplifier Transistor	20	3	10	50	35	PNP	TO-92	4-100
BF959	SAW Filter Transistor	40	20	10	50	20	NPN	TO-92	4-107

High Voltage Transistors

Device	Designation	H_{FE} @ (min.)	I_C mA	V_{CE} V	I_C (cont.) mA	BV_{CEO} V	Polarity	Package	Page
BC372, 373	Darlington Transistors	10K-25K	100	5	1000	80-100	NPN	TO-92	4-17
BC445, 447, 449	Driver/Output Transistors	50-180	2	5	300	60-100	NPN	TO-92	4-34
BC446, 448, 450	Driver/Output Transistors	50-180	2	5	300	60-100	PNP	TO-92	4-38
BC485, 487, 489	Driver/Output Transistors	60-160	100	2	1000	45-80	NPN	TO-92	4-42
BC486, 488, 490	Driver/Output Transistors	60-160	100	2	1000	45-80	PNP	TO-92	4-46
BF257, 258, 259	Video O/P Transistors	25	30	10	100	160-300	NPN	TO-39	4-92
BF491, 492, 493	Video Transistors	40	10	10	500	200-300	PNP	TO-92	4-94
BF787, 789, 791	Video O/P Transistors	50	25	20	100	250-350	NPN	306-04	4-104
BF788, 790, 792		50	25	20	100	250-350	PNP	306-04	4-104
MPS A05, A06	Comp. Driver Transistors	50	10	1	500	60-80	NPN	TO-92	4-110
MPS A55, A56		50	10	1	500	60-80	PNP	TO-92	4-110
MPS L01	Amplifier Transistor	50	10	5	150	120	NPN	TO-92	4-125

High Current Transistors

Device	Designation	H_{FE} @ (min.)	I_C mA	V_{CE} V	I_C (cont.) mA	BV_{CEO} V	Polarity	Package	Page
BC327, 328	Compl. Driver OP Transistors	100-160	100	1	800	25-45	PNP	TO-92	4-11
BC337, 338		100-160	100	1	800	25-45	NPN	TO-92	4-11
BC372, 373	Darlington Transistors	10K-25K	100	5	1000	80-100	NPN	TO-92	4-17
BC485, 487, 489	Driver/Output Transistors	60-160	100	2	1000	45-80	NPN	TO-92	4-42
BC486, 488, 490	Driver/Output Transistors	60-160	100	2	1000	45-80	PNP	TO-92	4-46
BF491, 492, 493	Video Transistors	40	10	10	500	200-300	PNP	TO-92	4-94
MPS A05, A06	Compl. Driver Transistors	50	10	1	500	60-80	NPN	TO-92	4-110
MPS A55, A56		50	10	1	500	60-80	PNP	TO-92	4-110

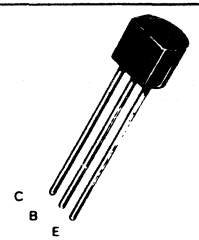
BC 237
BC 238
BC 239

NPN SILICON ANNULAR TRANSISTORS

. . . designed for general-purpose use in audio, radio, and television applications.

- High Breakdown Voltage—
  BV_{CEO} = 45, 20, 45 Vdc (Min) @ I_C = 2.0 mAdc
- Low Collector-Emitter Saturation Voltage—
  $V_{CE(sat)}$ = 0.6 Vdc (Max) @ I_C = 100 mAdc
- Low Collector-Base capacitance
  C_{cbo} = 4.5 pf (Max) @ V_{CB} = 10 Vdc
- Complementary to PNP BC 307, BC 308, BC 309
- One-Piece, Injection-Molded Unibloc † Package

NPN SILICON AMPLIFIER TRANSISTORS



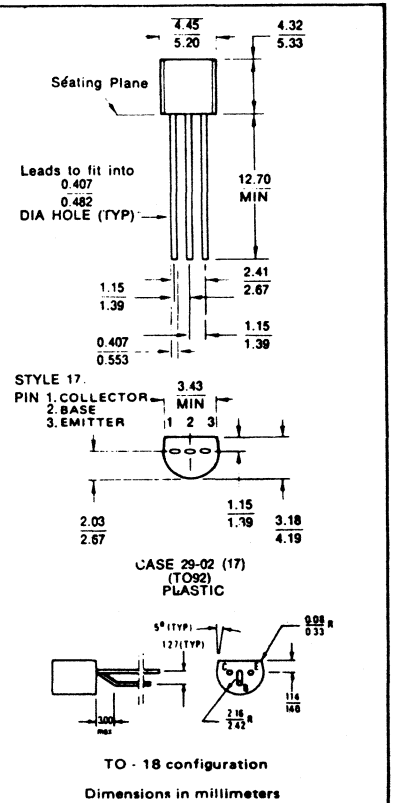
For standard package order BC 237 / 238 / 239
For TO - 18 configuration order BC 237 - 18 / 238 - 18 / 239 - 18
For TO - 5 configuration order BC 237 - 5 / 238 - 5 / 239 - 5

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BC 237 BC 238 BC 239	45 20 45	Vdc
Collector-Emitter Voltage	V_{CES}	BC 237 BC 238 BC 239	50 30 50	Vdc
Emitter-Base Voltage	V_{EB}		5.0	Vdc
Collector Current—Continuous Peak	I_C		0.10 0.20	Adc
Base Current—Continuous	I_B		0.05	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D		350 2.81	mW mW/°C
Operating and Storage Junction Temperature range	T_J, T_{stg}		−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}		0.357	°C/mW



TO - 18 configuration

Dimensions in millimeters

* Annular Semiconductors Patented by Motorola Inc.

† Trademark of Motorola Inc.

4

ELECTRICAL CHARACTERISTICS (T_A 25° C unless otherwise noted)

Characteristic	Type	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 2.0 mAdc, I_B = 0)	BC 237 BC 238 BC 239	BV_{CEO}	45 20 45			Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BC 237 BC 238 BC 239	BV_{EBO}	6 5 5			Vdc
Collector Cutoff Current						
(V_{CE} = 30Vdc, V_{BE} = 0)	BC 238	I_{CES}		0.20	15	
(V_{CE} = 50 Vdc, V_{BE} = 0)	BC 239 BC 237			0.20 0.20	15 15	ηAdc
(V_{CE} = 30 Vdc, V_{BE} = 0) T_A = 125 C	BC 238			0.20	4	
(V_{CE} = 50 Vdc, V_{BE} = 0) T_A = 125 C	BC 239 BC 237			0.20 0.20	4 4	μAdc
ON CHARACTERISTICS						
DC Current Gain						
(I_C = 10 μAdc, V_{CE} = 5 Vdc)		h_{FE}				
	BC 237A/238A			90		
	BC 237B/238B/239B			150		
	BC 237C/238C/239C			270		
(I_C = 2mAdc, V_{CE} = 5Vdc)						
	BC 237		120		800	
	BC 238		120		800	
	BC 239		180		800	
	BC 237A/238A		120	170	220	
	BC 237B/238B/239B		180	290	460	
	BC 237C/238C/239C		380	500	800	
(I_C = 100 mAdc, V_{CE} = 5 Vdc)						
	BC 237A/238A			120		
	BC 237B/238B/239B			180		
	BC 237C/238C/239C			300		
Collector-Emitter On Voltage						
(I_C = 100 μAdc, I_B = 5 μAdc)	BC 237/BC 238/BC 239	$V_{CE(sat)}$		0.07	0.20	Vdc
(I_C = 100 mAdc, I_B = 5 mAdc)	BC 237/BC 239			0.20	0.60	
	BC 238			0.20	–	
Base-Emitter Saturation Voltage						
(I_C = 100 μAdc, I_B = 5 μAdc)		$V_{BE(sat)}$		0.60	0.83	Vdc
(I_C = 100 mAdc, I_B = 5 mAdc)				1.05		
Base-Emitter On Voltage		$V_{BE(on)}$				Vdc
(I_C = 100 μAdc, V_{CE} = 5 Vdc)				0.50		
(I_C = 2 mAdc, V_{CE} = 5 Vdc)			0.55	0.62	0.70	
(I_C = 100 mAdc, V_{CE} = 5 Vdc)				0.83		

DYNAMIC CHARACTERISTICS, SMALL SIGNAL CHARACTERISTICS

Characteristic	Type	Symbol	Min	Typ	Max	Unit
Current-Gain-Bandwidth Product		f_T				MHz
(I_C = 0.5 mAdc, V_{CE} = 3 Vdc, f = 100 MHz)						
	BC 237			100		
	BC 238			120		
	BC 239			140		
(I_C = 10 mAdc, V_{CE} = 5 Vdc, f = 100 MHz)						
	BC 237		150	200		
	BC 238		150	240		
	BC 239		150	280		
Collector-Base Capacitance		C_{cb}				pF
(V_{CB} = 10 Vdc, I_C = 0, f = 1 MHz)					4.50	
Emitter-Base Capacitance		C_{eb}				pF
(V_{BE} = 0.5 Vdc, I_C = 0, f = 1 MHz)				8.0		
Input Impedance		h_{ie}(h11e)				K ohm
(I_C = 2 mAdc, V_{CE} = 5 Vdc, f = 1 KHz)						
	BC 237A/238A		1.6	2.2	4.5	
	BC 237B/238B/239B		3.2	6.0	8.5	
	BC 237C/238C/239C		6.0	8.7	15.0	
Voltage Feedback Ratio		h_{re}(h12e)				X10 $^{-4}$
(I_C = 2 mAdc, V_{CE} = 5 Vdc, f = 1 KHz)						
	BC 237A/238A			1.5		
	BC 237B/238B/239B			2.0		
	BC 237C/238C/239C			3.0		
Small-Signal Current Gain		h_{fe}(h21e)				
(I_C = 2 mAdc, V_{CE} = 5 Vdc, f = 1 KHz)						
	BC 237A/238A		125	220	260	
	BC 237B/238B/239B		240	330	500	
	BC 237C/238C/239C		450	600	900	
Output Admittance		h_{oe}(h22e)				μ mhos
(I_C = 2 mAdc, V_{CE} = 5 Vdc, f = 1 KHz)						
	BC 237A/238A			8	25	
	BC 237B/238B/239B			10	35	
	BC 237C/238C/239C			12	50	
Noise Figure		NF				dB
(I_C = 0.2 mAdc, V_{CE} = 5 Vdc, R_S = 2 Kohms, f = 30 Hz to 15 KHz)	BC 239			2	4	
(I_C = 0,2 mAdc, V_{CE} = 5 Vdc, R_S = 2 Kohms, f = 1 KHz, Δf = 200 Hz)	BC 237			2	10	
	BC 238			2	10	
	BC 239			2	4	

4

FIGURE 1 NORMALIZED DC CURRENT GAIN

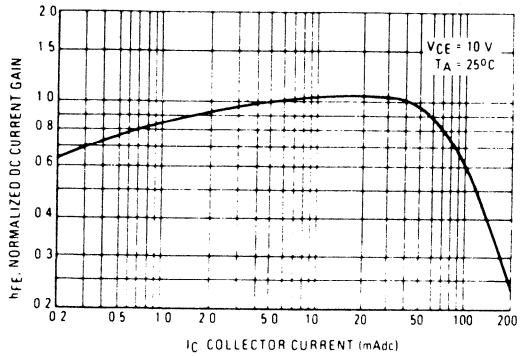


FIGURE 2 - "SATURATION" AND "ON" VOLTAGES

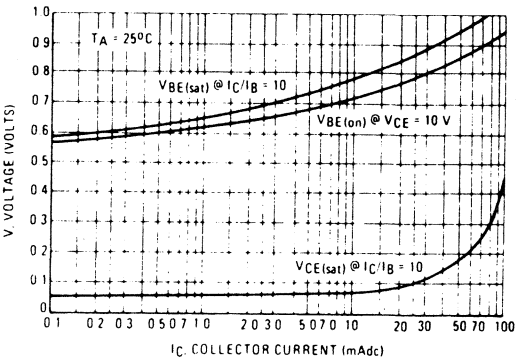


FIGURE 3 - CURRENT GAIN-BANDWIDTH PRODUCT

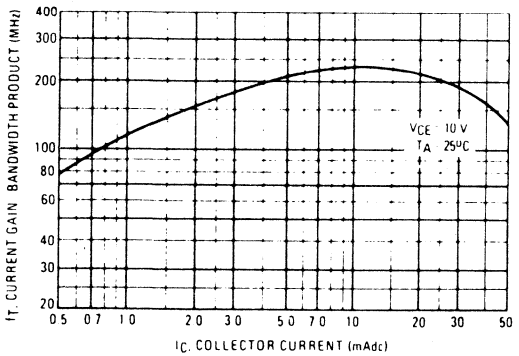


FIGURE 4 - CAPACITANCES

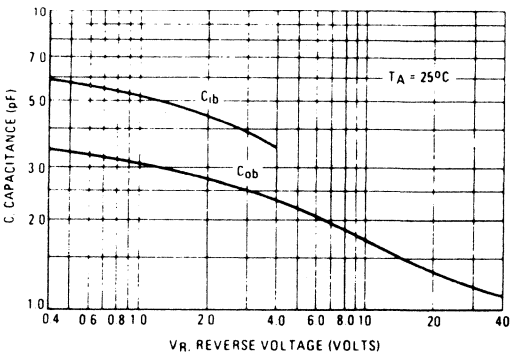


FIGURE 5 – OUTPUT ADMITTANCE

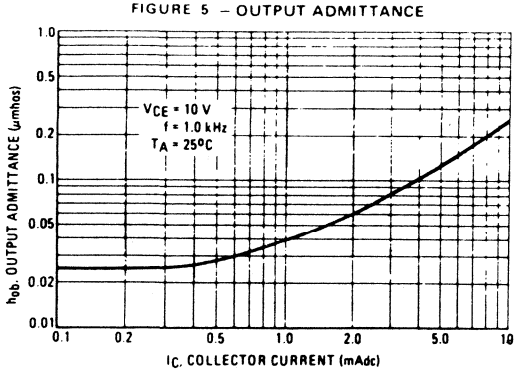
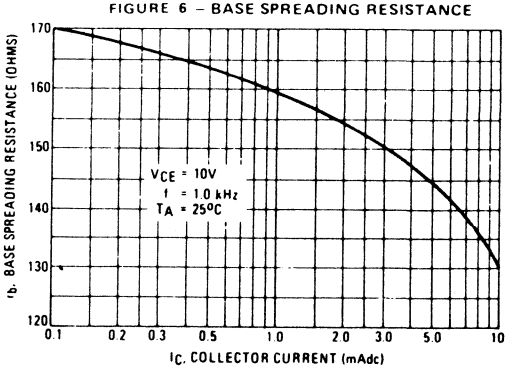


FIGURE 6 – BASE SPREADING RESISTANCE



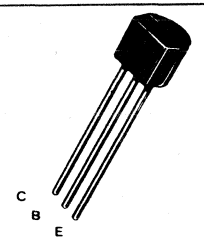
BC307
BC308 • BC309

PNP SILICON ANNULAR* TRANSISTORS

. . . designed for general purpose use in audio, radio, and television applications.

- High Breakdown Voltage—
  BV_{CEO} = 20, 25, 45 Vdc (Min) @ I_C = 2.0 mAdc
- Low Collector-Emitter Saturation Voltage—
  $V_{CE\ (sat)}$ = 0.35 Vdc (Typ) @ I_C = 100 mAdc
- Low Collector - Base capacitance
  C_{cbo} = 6.0 pF (Max) @ V_{CB} = 10 Vdc
- Complementary to NPN BC 237, BC 238, BC 239
- One-Piece, Injection-Molded Unibloc† Package

PNP SILICON AMPLIFIER TRANSISTORS



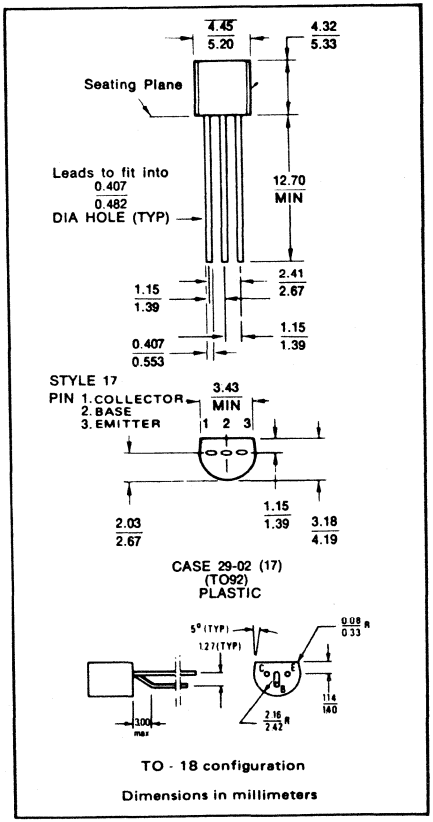
For standard package order BC 307 / 308 / 309
For TO - 18 configuration order BC 307 - 18 / 308 - 18 / 309 - 18
For TO - 5 configuration order BC 307 - 5 / 308 - 5 / 309 - 5

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BC 307 BC 308 BC 309	45 25 45	Vdc
Collector-Emitter Voltage	V_{CES}	BC 307 BC 308 BC 309	50 30 50	Vdc
Emitter-Base Voltage	V_{EB}	all	5.0	Vdc
Collector Current - Continuous Peak	I_C I_{CM}	all	0.10 0.20	A
Base Current - Continuous	I_B	all	0.05	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	all	0.30 2.40	Watts mW/°C
Operating and Storage Junction Temperature range	T_J, T_{stg}	all	-55 to + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}		0.416	°C/mW



* Annular Semiconductors Patented by Motorola Inc.
† Trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Type	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 2.0 mAdc, I_B = 0)	BC 307	BV_{CEO}	45	–	–	Vdc
	BC 308		25	–	–	
	BC 309		45	–	–	
Emitter-Base Breakdown Voltage (I_E = 100μAdc, I_C = 0)	BC 307	BV_{EBO}	5	–	–	Vdc
	BC 308		5	–	–	
	BC 309		5	–	–	
Collector-Emitter Leakage Current (V_{CES} = 20 V)	BC 307	I_{CES}	–	2	100	nA
	BC 308		–	2	100	
	BC 309		–	2	100	
(V_{CES} = 20 V, T_A = 125°C)	BC 307		–	–	4	μA
	BC 308		–	–	4	
	BC 309		–	–	4	
ON CHARACTERISTICS						
DC Current Gain (I_C = 10 μ Adc, V_{CE} = 5 Vdc)	BC 307A/308A/309A	h_{FE}	–	90	–	
	BC 307B/308B/309B		–	150	–	
	BC 307C/308C/309C		–	270	–	
(I_C = 2 mAdc, V_{CE} = 5 Vdc)	BC 307		120	–	800	
	BC 308		120	–	800	
	BC 309		120	–	800	
	BC 307A/308A/309A		120	170	220	
	BC 307B/308B/309B		180	290	460	
	BC 307C/308C/309C		380	500	800	
(I_C = 100 mAdc, V_{CE} = 5 Vdc)	BC 307A/308A/309A		–	120	–	
	BC 307B/308B/309B		–	180	–	
	BC 307C/308C/309C		–	300	–	
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 0,5 mAdc)		V_{CE} (sat)	–	0.10	–	Vdc
(I_C = 10 mAdc, I_B = see Note 1)			–	0.30	0.60	
(I_C = 100 mAdc, I_B = 5 mAdc)			–	0.25	–	
Base-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 0.5 mAdc)		V_{BE} (sat)	–	0.70	–	Vdc
(I_C = 100 mAdc, I_B = 5 mAdc)			–	1.00	–	
Base-Emitter on Voltage (I_C = 2 mAdc, V_{CE} = 5 Vdc)		V_{BE} (on)	0.55	0.62	0.70	Vdc

Note 1 : I_C = 10 mAdc on the constant base current characteristic, which yields the point I_C = 11 mAdc, V_{CE} = 1 V

DYNAMIC CHARACTERISTICS / SMALL SIGNAL CHARACTERISTICS

Characteristic	Type	Symbol	Min	Typ	Max	Unit
Current-Gain – Bandwidth Product (I_C= 10 mAdc, V_{CE}= 5 Vdc, f = 50 MHz)		f_T				MHz
	BC 307		–	280	–	
	BC 308		–	320	–	
	BC 309		–	360	–	
Collector-Base Capacitance (V_{CB}= 10 Vdc, I_C= 0, f = 1 MHz)		C_{cbo}	–	–	6.0	pF
Noise Figure		NF				dB
(I_C= 0.2 mAdc, V_{CE}= 5 Vdc, R_S= 2 Kohms, f = 30 Hz to 15 KHz)	BC 309		–	2	4	
(I_C= 0,2 mAdc, V_{CE}= 5 Vdc, R_S= 2 Kohms, f = 1 KHz, f = 200 Hz)	BC 307		–	2	10	
	BC 308		–	2	10	
	BC 309		–	2	4	
Input Impedance (I_C= 2 mAdc, V_{CE}= 5 Vdc, f = 1 KHz)		$h_{ie}(h_{11e})$				kΩ
	BC 307A/308A/309A		1.2	2.7	4.5	
	BC 307B/308B/309B		3.0	4.5	8.0	
	BC 307C/308C/309C		5.0	8.0	14.0	
Voltage Feedback Ratio (I_C= 2 mAdc, V_{CE}= 5 Vdc, f = 1 KHz)		$h_{re}(h_{12e})$				10^{-4}
	BC 307A/308A/309A		–	3.0	–	
	BC 307B/308B/309B		–	3.5	–	
	BC 307C/308C/309C		–	4.0	–	
Small Signal Current Gain (I_C= 2 mAdc, V_{CE}= 5 Vdc f = 1 KHz)		$h_{fe}(h_{21e})$				–
	BC 307A/308A/309A		125	220	260	
	BC 307B/308B/309B		240	330	500	
	BC 307C/308C/309C		450	600	900	
Output Admittance (I_C= 2 mAdc, V_{CE}= 5 Vdc, f= 1 KHz)		$h_{oe}(h_{22e})$				μmhos
	BC 307A/308A/309A		–	25	50	
	BC 307B/308B/309B		–	30	70	
	BC 307C/308C/309C		–	60	110	

4

FIGURE 1 – NORMALIZED DC CURRENT GAIN

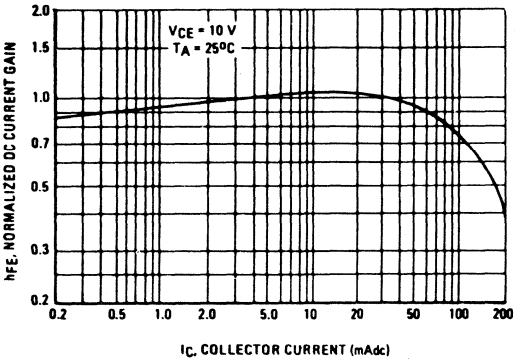


FIGURE 2 – "SATURATION" AND "ON" VOLTAGES

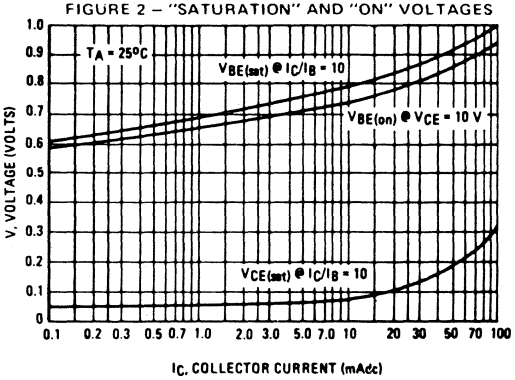


FIGURE 3 – CURRENT-GAIN–BANDWIDTH PRODUCT

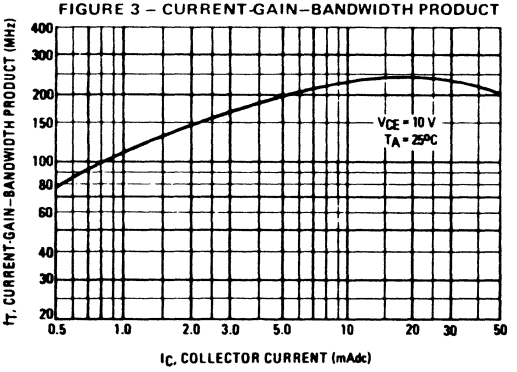


FIGURE 4 – CAPACITANCES

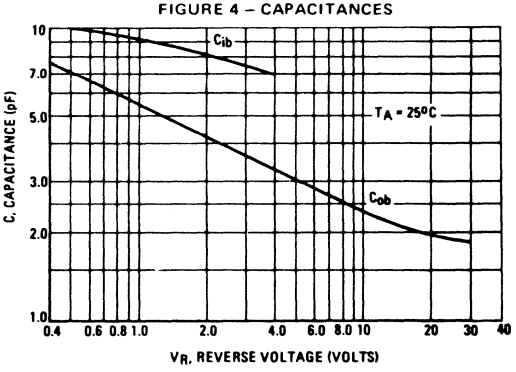


FIGURE 5 – OUTPUT ADMITTANCE

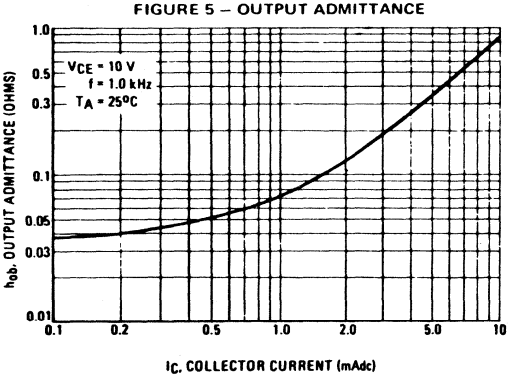
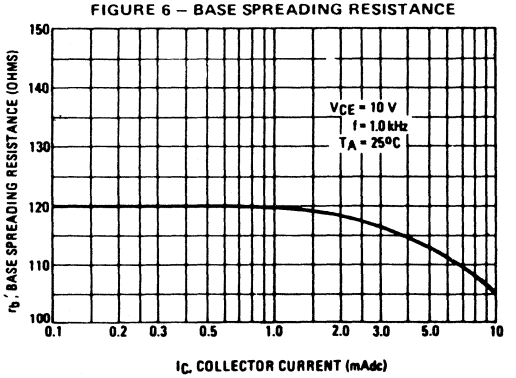


FIGURE 6 – BASE SPREADING RESISTANCE



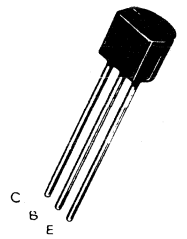
BC327
BC328

PNP SILICON ANNULAR♦ TRANSISTORS

... designed for complementary driver and output stages where the following features are important.

- High Peak Current of 1 Amp
- High Gain, h_{FE} = 40 min at I_C = 300 mA
- Low Saturation Voltage, $V_{CE\ sat}$ = 0.7 Volts max. at I_C = 500 mA
- High Power Dissipation[1], P_D = 1.5 Watt
- One-Piece, Injection-Molded Unibloc Package
- Complementary to NPN BC337, BC338
- Available in -16 and -25 gain groups

PNP SILICON AMPLIFIER TRANSISTORS



For standard package order BC327/BC328
For TO - 18 configuration order BC327 - 16/328 - 16
For TO - 5 configuration order BC327 - 5/328 - 5

T Case ≤ 25 °C.

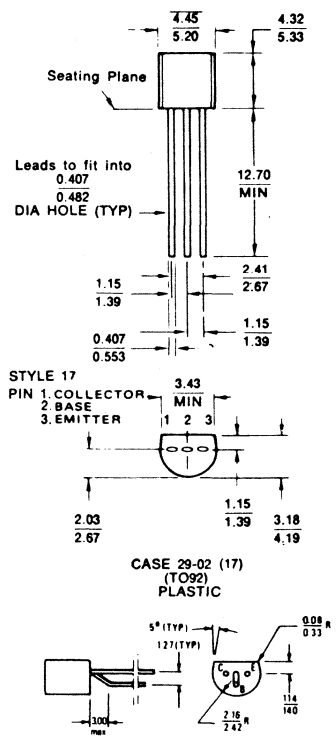
MAXIMUM RATINGS

Rating	Symbol	BC327	BC328	Unit
Collector-Emitter Voltage	V_{CEO}	45	25	Vdc
Collector-Base Voltage	V_{CB}	50	30	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Total Device Dissipation @ T_A = 25° C Derate above 25° C	P_D	625 5.0		mW mW/° C
Total Device Dissipation @ T_C = 25° C Derate above 25° C	P_D	1.5 12.0		Watt mW/° C
DC Collector Current	I_C	800		mA
Collector Current (10 μsec pulse)	I_C	1.0		A
DC Base Current	I_B	100		mA
Base Current (10 μsec pulse)	I_B	200		mA
Operating and Storage Junction Temperature Range	T_J, T_{stg}	— 55 to + 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	83.3	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	200	°C/W

♦ Annular Semiconductors patented by Motorola Inc.



TO-18 configuration
Dimensions in millimeters

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Characteristics & Conditions	Symbol	Type	Min.	Typ.	Max.	Unit
Collector-Emitter Breakdown Voltage I_C = 10mA, I_B = 0	BV_{CEO}	BC327 BC328	45 25			Vdc
Collector-Base Breakdown Voltage I_C = 10μA, I_E = 0	BV_{CBO}	BC327 BC328	50 30			Vdc
Emitter-Base Breakdown Voltage I_E = 10μA, I_C = 0	BV_{EBO}		5			Vdc
Collector Cutoff Current BC327 — V_{CB} = 30V I_E = 0 BC328 — V_{CB} = 20V I_E = 0	I_{CBO}				100	nAdc
Emitter Cutoff Current V_{EB} = 4V, I_C = 0	I_{EBO}				100	nAdc
DC Current Gain I_C = 100mA, V_{CE} = 1V BC327/BC328 BC327-16/BC328-16 BC327-25/BC328-25 I_C = 300mA, V_{CE} = 1V	h_{FE}		100 100 160 40		600 250 400	
Base-Emitter On Voltage I_C = 300mA, V_{CE} = 1V	$V_{BE(on)}$				1.2	Vdc
Collector-Emitter Saturation Voltage I_C = 500mA, I_B = 50mA	$V_{CE(sat)}$				0.7	Vdc
Output Capacitance V_{CB} = 10V, I_E = 0 f = 1MHz	C_{ob}			5		pF
Current-Gain-Bandwidth Product I_C = 10mA, V_{CE} = 5V	f_T			260		MHz

FIGURE 1 – THERMAL RESPONSE

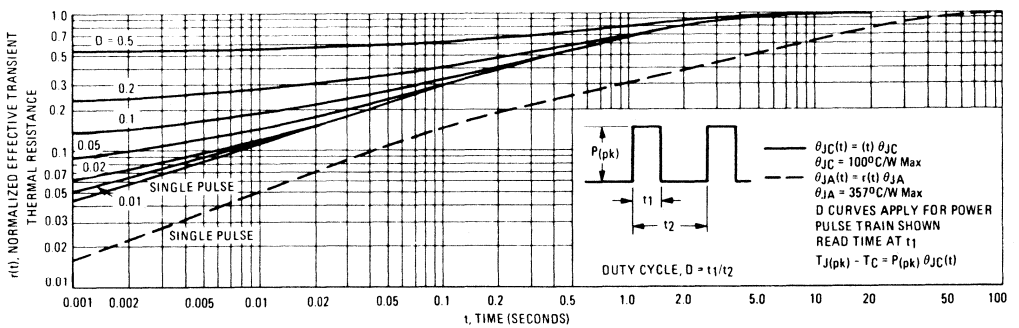


FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

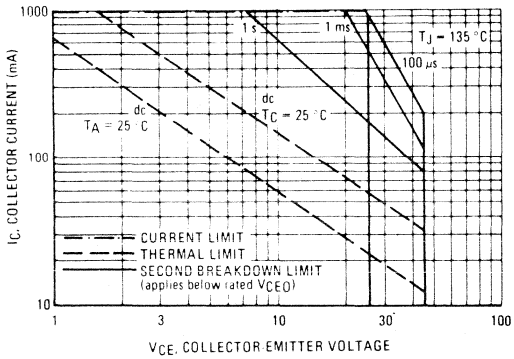


FIGURE 3 – DC CURRENT GAIN

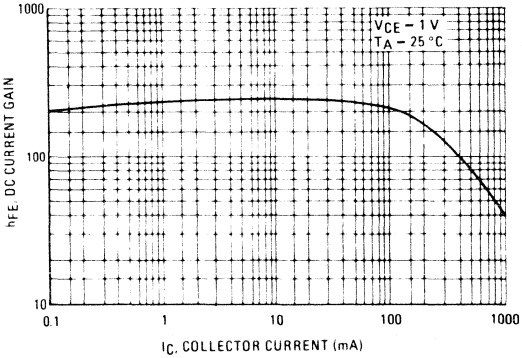


FIGURE 4 – SATURATION REGION

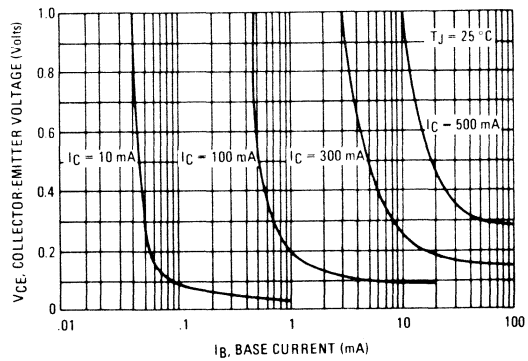


FIGURE 5 – "ON" VOLTAGES

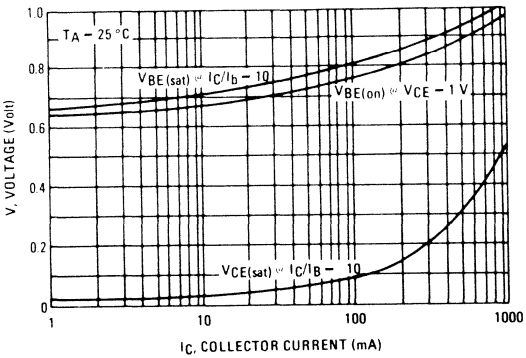


FIGURE 6 – TEMPERATURE COEFFICIENTS

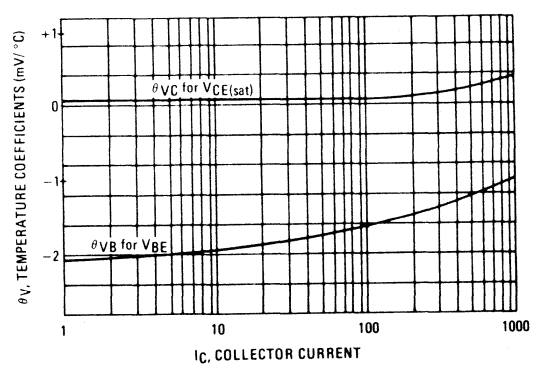
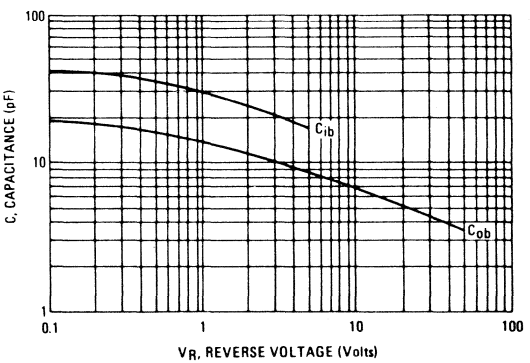


FIGURE 7 – CAPACITANCES



4

BC337
BC338

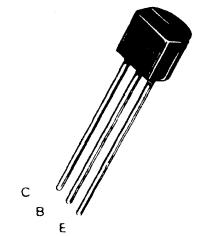
NPN SILICON ANNULAR♦ TRANSISTORS

. . . designed for complementary driver and output stages where the following features are important.

- High Peak Current of 1 Amp
- High Gain, h_{FE} = 60 min at I_C = 300 mA
- Low Saturation Voltage, V_{CEsat} = 0.7 Volts max. at I_C = 500 mA
- High Power Dissipation[1], P_D = 1.5 Watt
- One-Piece, Injection-Molded Unibloc Package
- Complementary to PNP BC327, BC328
- Available in -16, -25 and -40 gain groups

[1] T Case ≤ 25 °C.

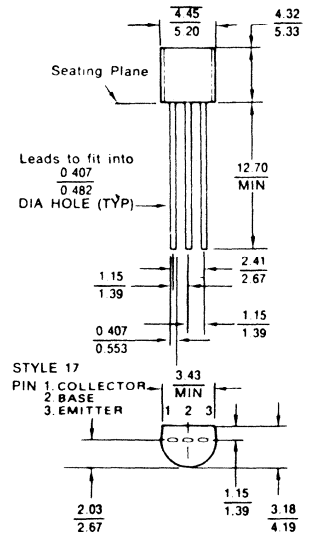
NPN SILICON AMPLIFIER TRANSISTORS



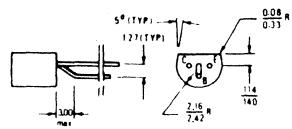
For standard package order BC 337 / BC 338
For TO-18 configuration order BC 337-16 / 338-16
For TO-5 configuration order BC 337-5 / 338-5

MAXIMUM RATINGS

Rating	Symbol	BC337	BC338	Unit
Collector-Emitter Voltage	V_{CEO}	45	25	Vdc
Collector-Base Voltage	V_{CB}	50	30	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Total Device Dissipation @ T_A = 25° C Derate above 25° C	P_D	625 5.0		mW mW/°C
Total Device Dissipation @ T_C = 25° C Derate above 25° C	P_D	1.5 12.0		Watt mW/°C
DC Collector Current	I_C	800		mA
Collector Current (10 μsec pulse)	I_C	1.0		A
DC Base Current	I_B	100		mA
Base Current (10 μsec pulse)	I_B	200		mA
Operating and Storage Junction Temperature Range	T_J, T_{stg}	— 55 to + 150		°C



CASE 29-02 (17)
(TO92)
PLASTIC



TO-18 configuration
Dimensions in millimeters

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	83.3	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	200	°C/W

♦ Annular Semiconductors patented by Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Characteristics & Conditions	Symbol	Type	Min.	Typ.	Max.	Unit
Collector-Emitter Breakdown Voltage I_C = 10mA, I_B = 0	BV_{CEO}	BC337 BC338	45 25			Vdc
Collector-Base Breakdown Voltage I_C = 10μA, I_E = 0	BV_{CBO}	BC337 BC338	50 30			Vdc
Emitter-Base Breakdown Voltage I_E = 10μA, I_C = 0	BV_{EBO}		5			Vdc
Collector Cutoff Current BC337 — V_{CB} = 30V I_E = 0 BC338 — V_{CB} = 20V I_E = 0	I_{CBO}				100	nAdc
Emitter Cutoff Current V_{EB} = 4V, I_C = 0	I_{EBO}				100	nAdc
DC Current Gain I_C = 100mA, V_{CE} = 1V BC337/BC338 BC337-16/BC338-16 BC337-25/BC338-25 BC337-40/BC338-40 I_C = 300mA, V_{CE} = 1V	h_{FE}		 100 100 160 250 60		 600 250 400 600	
Base-Emitter On Voltage I_C = 300mA, V_{CE} = 1V	$V_{BE(on)}$				1.2	Vdc
Collector-Emitter Saturation Voltage I_C = 500mA, I_B = 50mA	$V_{CE(sat)}$				0.7	Vdc
Output Capacitance V_{CB} = 10V, I_E = 0 f = 1MHz	C_{ob}			4		pF
Current-Gain-Bandwidth Product I_C = 10mA, V_{CE} = 5V	f_T			210		MHz

4

FIGURE 1 – THERMAL RESPONSE

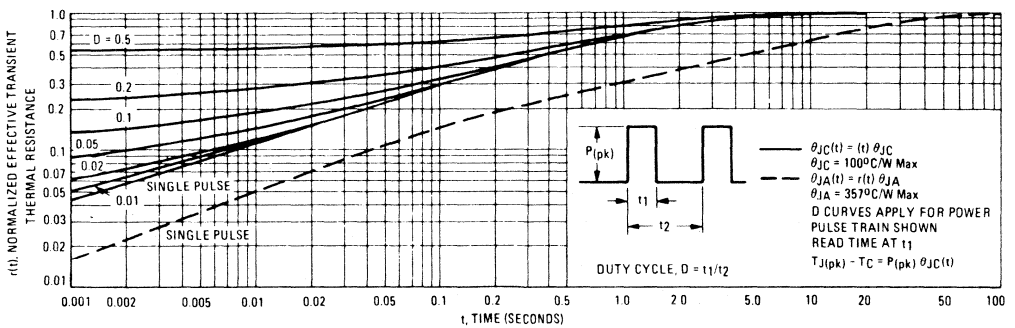


FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

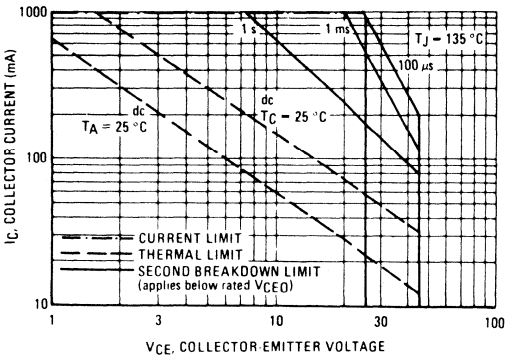


FIGURE 3 – DC CURRENT GAIN

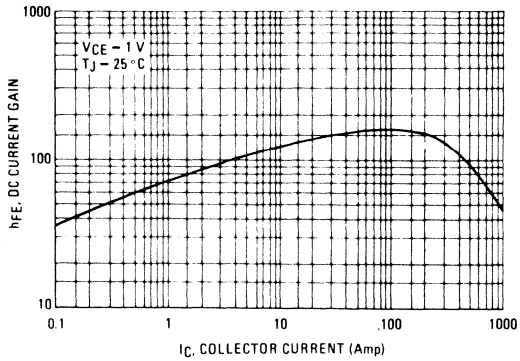


FIGURE 4 – SATURATION REGION

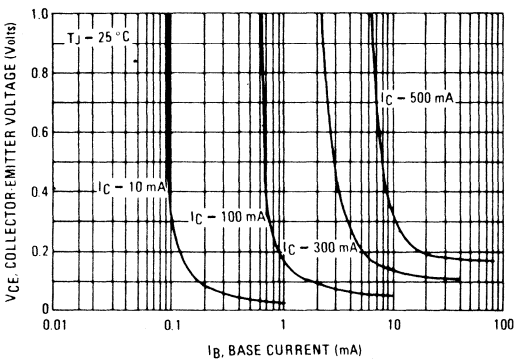


FIGURE 5 – "ON" VOLTAGES

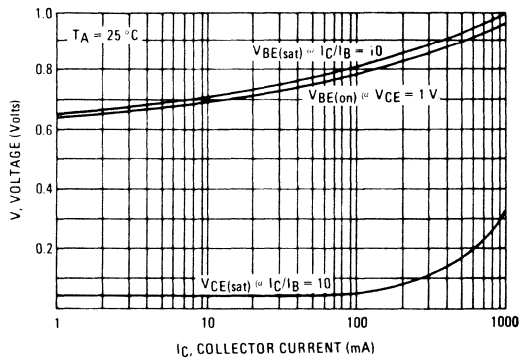


FIGURE 6 – TEMPERATURE COEFFICIENTS

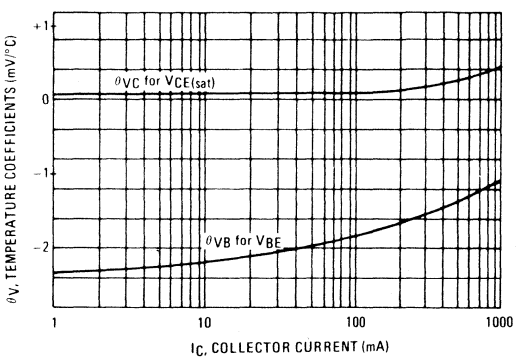
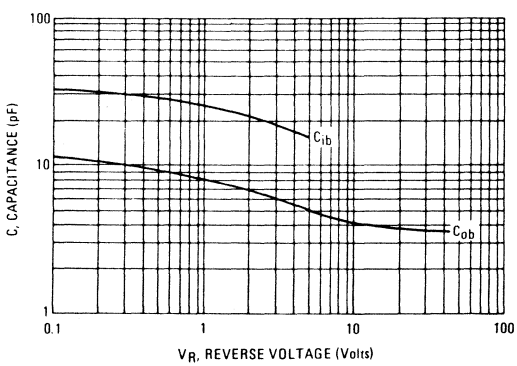


FIGURE 7 – CAPACITANCES



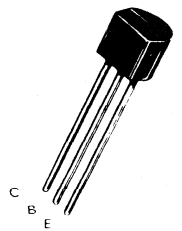
BC372
BC373

NPN SILICON HIGH VOLTAGE DARLINGTON

. . . designed for use relay driver and all inductive load applications.

- High Collector-Emitter Breakdown Voltage
  BV_{CES} – 100 V at 100 μA for BC372
  – 80 V at 100 μA for BC373
- High Current gain
  I_C – 100/mAdc, V_{CE} – 5 Vdc (min, 10000, max. 600000).
- Available in standardized gain groups (–16, –25, –40).

NPN SILICON DARLINGTON TRANSISTORS



For standard package order BC372, BC373
For TO - 18 configuration order
BC372-18, BC373-18
For TO - 5 configuration order
BC372-5, BC373-5.

MAXIMUM RATINGS

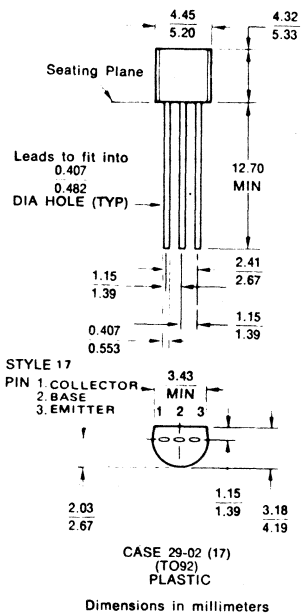
Rating	Symbol	BC372	BC373	Unit
Collector-Emitter Voltage	V_{CEO}	100	80	Vdc
Collector-Base Voltage	V_{CB}	100	80	Vdc
Emitter-Base Voltage	V_{EB}	12		Vdc
Collector-Current-Continuous	I_C	1.0		Adc
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	625 5.0		mW mW/°C
Total Device Dissipation T_C = 25 C Derate above 25 C	P_D	1.5 12.0		W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal resistance, Junction to case	Θ_{JC}	0.083	°C/mW
Thermal resistance, Junction to Ambient	Θ_{JA}	0.20	°C/mW

* Annular Semiconductors patented by Motorola Inc

[1] Due to the monolithic construction of this device breakdown voltages of both transistors are identical BV_{CES} is tested in lieu of BV_{CEO} in order to avoid errors caused by boise pickup. The voltage measured during the BV_{CES} test is the BV_{CEO} of the output transistor.



CASE 29-02 (17)
(TO92)
PLASTIC

Dimensions in millimeters

4

ELECTRICAL CHARACTERISTICS (T_A = 25°C unlessotherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage* (I_C = 100 μAdc, I_B = 0) BC372 BC373	BV_{CES}	 100 80			Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0) BC372 BC373	BV_{CBO}	 100 80			Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	12			Vdc
Collector cutoff current V_{CB} = 80 Vdc – I_E = 0 BC372 V_{CB} = 60 Vdc – I_E = 0 BC373	I_{CBO}			 100 100	nAdc
Emitter cutoff current V_{BE} = 10 V, I_C = 0	I_{EBO}			100	nAdc
ON CHARACTERISTICS*					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5 Vdc) plein range –16 –25 –40 (I_C = 250 mAdc, V_{CE} = 5 Vdc) plein range –16 –25 –40	h_{FE}	 10 K 10 K 25 K 60 K 8 K 8 K 20 K 40 K		 600 K 60 K 160 K 600 K	
Collector Emitter Saturation Voltage (I_C = 250 mAdc – I_B = 0,25 mAdc	$V_{CE\ (sat)}$		0.8	1	Vdc
Base Emitter Saturation Voltage (I_C = 250 mAdc, I_B = 0,25 mAdc)	$V_{BE\ (sat)}$		1.4	2	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (I_C = 100 mAdc, V_{CE} = 5.0 Vdc, f = 20 MHz)	f_T	100	200		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}		10	25	pF
Noise Figure (I_C = 1 mAdc, V_{CE} = 5 Vdc, R_g = 100 Kohm, F = 1 KHz	N_F		2.0		dB

*Pulse test – Pulse width = 300 μs – Duty cycle 2%.

FIGURE 1 – DC CURRENT GAIN

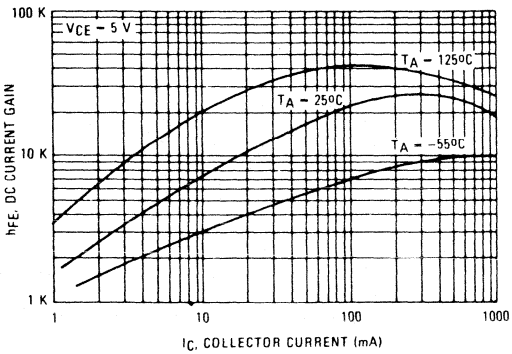


FIGURE 2 – "SATURATION" AND "ON" VOLTAGES

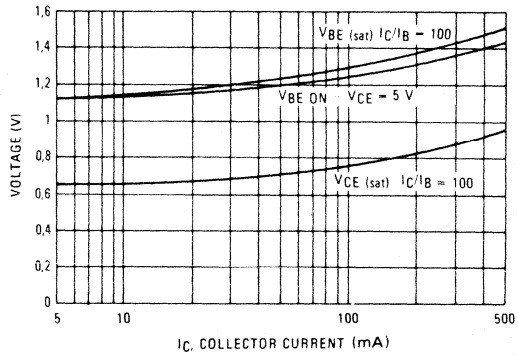


FIGURE 3 – CURRENT GAIN BANDWIDTH PRODUCT

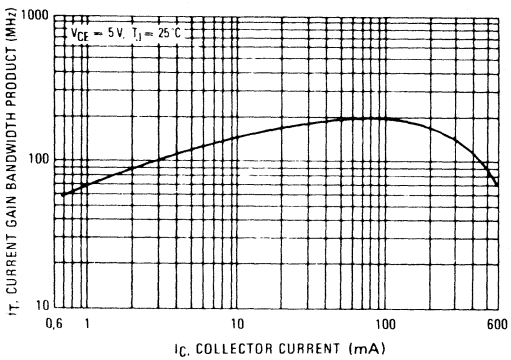
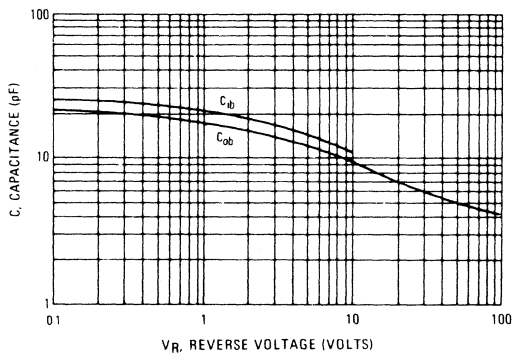


FIGURE 4 – CAPACITANCES



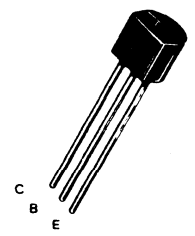
4

BC413
BC414

NPN SILICON ANNULAR♦
LOW NOISE, HIGH GAIN AMPLIFIER TRANSISTOR

- Low Wideband Noise Figure
  NF = 2.5dB max (30Hz-15KHz)
- Low Noise At Low Frequency
  V_T = 12nV/$\sqrt{Hz}$ max (120Hz)
- High Gain in 2 Ranges
  B range: 180 – 460
  C range: 380 – 800
  (2mA/5V)
- Full Applications Information

NPN SILICON
LOW NOISE
TRANSISTOR



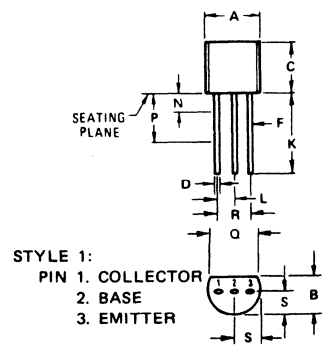
MAXIMUM RATINGS

Rating	Symbol	Value BC413	Value BC414	Unit
Collector-Emitter Voltage	V_{CEO}	30	45	Vdc
Collector-Base Voltage	V_{CBO}	45	50	Vdc
Emitter-Base Voltage	V_{EBO}	5		Vdc
Collector Current Continuous Peak	I_C	0.1 0.2		Adc Adc
Base-Current-Continuous	I_B	0.05		Adc
Total Device Dissipation at T_A = 25 °C Derate above 25 °C	P_D	350 2.81		mW mW/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	357	°C/W

♦ Annular Semiconductors Patented by Motorola Inc.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

ELECTRICAL CHARACTERISTICS (T_A = 25°C Unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Collector-Emitter Breakdown Voltage (I_C = 10mAdc, I_B = 0) BC413	BV_{CEO}	30			Vdc
BC414		45			
Collector-Base Breakdown Voltage (I_C = 10μAdc, I_E = 0) BC413	BV_{CBO}	45			Vdc
BC414		50			
Emitter-Base Breakdown Voltage (I_C = 10μAdc, I_C = 0)	BV_{EBO}	5			Vdc
Collector Cutoff Current (V_{CB} = 30Vdc, I_E = 0)	I_{CBO}			15	nAdc
(V_{CB} = 30Vdc, I_E = 0, T_A = + 125 °C)				5	μAdc
Emitter Cutoff Current (V_{EB} = 4Vdc, I_C = 0)	I_{EBO}			15	nAdc
On Characteristics					
DC Current Gain (I_C = 10μAdc, V_{CE} = 5Vdc) BC413B/BC414B	h_{FE}	100	150		
BC413C/BC414C		100	270		
(I_C = 2mAdc, V_{CE} = 5Vdc) BC413B/BC414B		180	290	460	
BC413C/BC414C		380	500	800	
Collector-Emitter Saturation Voltage	$V_{CE(S)}$				Vdc
(I_C = 10mAdc, I_B = 0.5mAdc)			0.075	0.25	
(I_C = 10mAdc, I_B = see note 1)			0.3	0.6	
(I_C = 100mAdc, I_B = 5mAdc, see note 2)			0.25	0.6	
Base-Emitter Saturation Voltage (I_C = 100mAdc, I_B = 5mAdc)	$V_{BE(S)}$		1.1		Vdc
Base-Emitter On Voltage	$V_{BE(ON)}$				Vdc
(I_C = 10μAdc, V_{CE} = 5 Vdc)			0.52		
(I_C = 100μAdc, V_{CE} = 5Vdc)			0.55		
(I_C = 2mAdc, V_{CE} = 5Vdc)		0.55	0.62	0.75	

Note 1: I_B is value for which I_C = 11mA at V_{CE} = 1V
Note 2: Pulse test = 300μs —— Duty Cycle = 2%

4

Characteristic	Symbol	Min	Typ	Max	Unit

Dynamic Characteristics

Current-Gain-Bandwidth Product (I_C = 10mAdc, V_{CE} = 5Vdc, f = 100MHz)	f_T		250		MHz
Collector-Base Capacitance (V_{CE} = 10Vdc, I_E = 0, f = 1MHz)	Ccbo		2.5		pF

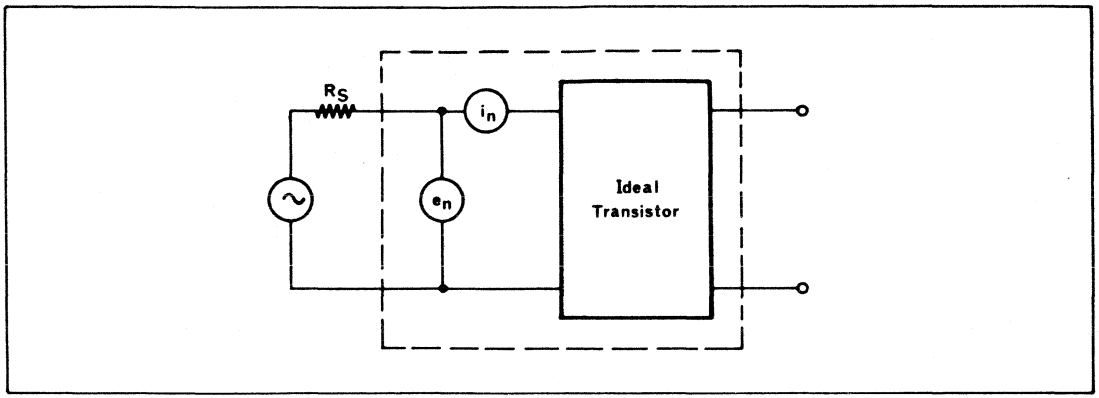
h-Parameters (I_C = 2mAdc, V_{CE} = 5Vdc, f = 1KHz)

Input Impedance	h_{ie}				KΩ
BC413B/BC414B	(h_{11e})	3.2	6.0	8.5	
BC413C/BC414C		6.0	8.7	15.0	
Voltage Feedback Ratio	h_{re}				10^{-4}
BC413B/BC414B	(h_{12e})		2.		
BC413C/BC414C			3.		
Small Signal Current Gain	h_{fe}				
BC413B/BC414B	(h_{21e})	240	330	500	
BC413C/BC414C		450	600	900	
Output Admittance	h_{oe}				μ mhos
BC413B/BC414B	(h_{22e})		10	60	
BC413C/BC414C			12	110	

Noise Performance

Noise Figure (I_C = 200μAdc, V_{CE} = 5Vdc, R_S = 2KΩ, f = 30Hz – 15KHz)	NF		0.6	2.5	dB
Equivalent Input Noise Voltage (I_C = 200μAdc, V_{CE} = 5V, R_S = 2KΩ, f = 120Hz) See Application note, Section I	V_T		8.0	12	$nV/\sqrt{Hz}$
Equivalent Input Noise Voltage (I_C = 200μAdc, V_{CE} = 5V, R_S = 2KΩ, f = 10Hz – 50Hz) See Application note, Section II	V_T		74	135	$nV/\sqrt{Hz}$

FIGURE 1. – TRANSISTOR NOISE MODEL.



NOISE APPLICATION NOTE

I. NOISE FIGURE RELATED TO V_T, e_n, and i_n

For a transistor, total noise at the input may be expressed as:

$$V_T = \left[e_n^2 + 4\,KT\,R_S + i_n^2 R_S^2\right]^{1/2} \qquad (1)$$

Where:

V_T = total noise voltage at the transistor input (Volts/$\sqrt{Hz}$)
e_n = noise voltage of the transistor referred to the input (figures 2 & 3)
i_n = noise current of the transistor referred to the input (figure 4)
K = Boltzmann's constant (1.38×10^{-23}j/°K)
T = Temperature of the source resistance (°K)
R_S = Source resistance (Ohms)

Example:
Find the total noise at the input of a BC414 for a collector current of 1mA and a source impedance of 1KΩ at a frequency of 120Hz and a temperature of 25 °C.

1. V_T is calculated from e_n, i_n

Read e_n = 4.5nV/$\sqrt{Hz}$ from figure 2 or figure 3 (Note that this is for a one cycle bandwidth)
Read i_n = 5.8pA/$\sqrt{Hz}$ from figure 4

$$V_T = [(3.5 \times 10^{-9})2 + (4).(1.38 \times 10^{-23}).(300).(1 \times 10^{3}) + (5.8 \times 10^{-12})2.(1 \times 10^{3})2]^{1/2}$$

Thus: $\boxed{V_T = 8.2nV}$

This checks with the value of 8nV shown in figure 6.

2. Noise figure is calculated from V_T

Noise figure is defined as:

$$NF = 20 \log_{10} \frac{\text{total noise voltage}}{\text{noise voltage contributed by source resistance}}$$

or

$$NF = 20 \log_{10} \left[\frac{V_T^2}{4\,KT\,R_S}\right]^{1/2}$$

Noise figure can be calculated for the above example as follows:

$$NF = 20 \log_{10} \left[\frac{(8 \times 10^{-9})2}{16.6 \times 10^{-18}}\right]^{1/2}$$

Thus: $\boxed{NF = 5.9\ dB}$

This checks with the values of 6 dB read from figure 7;

To minimize noise in a transistor stage, one might use figure 7 and deduce that noise is minimized when Noise Figure is minimum. This is not necessarily true as shown by figure 6 where the total noise voltage is a minimum at small values of source impedance.
This can be seen from equation (1) which shows that total noise is a direct function of source resistance.

4

II. NOISE VARIATION WITH FREQUENCY

Noise over a frequency band can be handled in one of two ways depending upon whether total transistor noise is constant or variable over the bandwidth of interest:

1. For constant transistor noise, multiply, V_T by the square root of bandwidth. i.e., $V_T = V_T . f.^{1/2}$
2. For variable transistor noise integrate the spectral density V_T (where $\Delta f = 1Hz$), over the bandwidth of interest.

Example: Low Frequency Noise

Find the total noise at the input in the bandwidth $f_1 = 10Hz$, $f_2 = 50Hz$ at $I_C = 200\mu A$ and $R_S = 2K\Omega$

This example corresponds to the popular "FLICKER NOISE" test shown on many data sheets.

$$V_T^2 = \int_{-\infty}^{+\infty} V_T(f) \times [G(f)]^2 \, df$$
$$(f_1 - f_2)$$

where:

$$V_{T(f)}^2 = e_{n(f)}^2 + 4KT\,R_S + i_{n(f)}^2\,R_S^2$$

$e_{n(f)}$ and 4 KT R_S are constant in the bandwidth

$$i_{n(f)} = \frac{i_n^2\ (1\ Hz)}{f}\ \text{(1/f noise spectrum density)}$$

G(f) bandpass filter

$= 1$ for $f \in (f_1, f_2)$

$= 0$ for $f \notin (f_1, f_2)$

after integration:

$$V_{T(f_1-f_2)}^2 = (e_{n(f1)}^2 + 4\,KT\,R_S) \times (f_2-f_1) + R_S^2\, i_{n(f1)}^2 \times f1 \times i_n\,(f1)\frac{f2}{f1}$$

Now:

$e_n = 5\ nV/\sqrt{Hz}$ at 10 Hz (from figure 2)

$i_n = 7\ pA/\sqrt{Hz}$ at 10 Hz (from figure 4)

$$V_T^2\,(10Hz-50Hz) = [(25 + 33.1)40 + 196 \times 10 \times 1.6].10^{-18}$$

Thus: $\boxed{V_T(10Hz-50Hz) = 74\ nV}$

FIGURE 2 – NOISE VOLTAGE vs FREQUENCY.

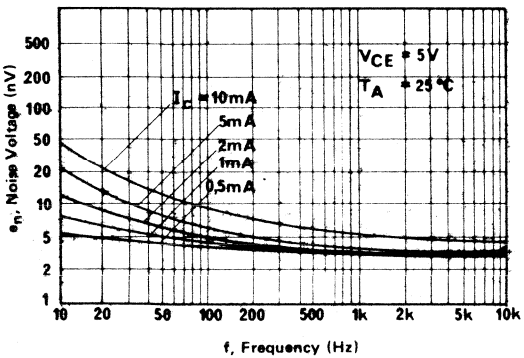


FIGURE 3. – NOISE VOLTAGE vs COLLECTOR CURRENT.

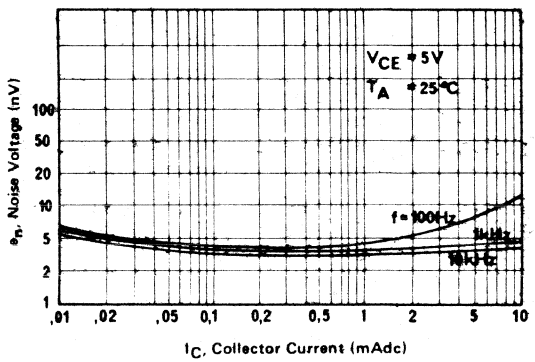


FIGURE 4. – NOISE CURRENT.

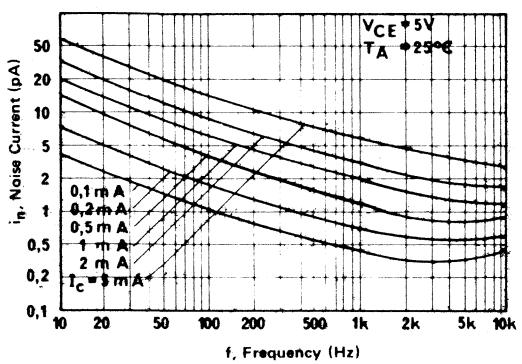


FIGURE 5. – WIDEBAND NOISE FIGURE.

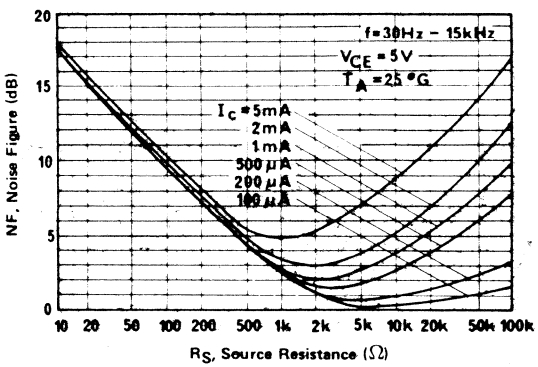


FIGURE 6. – TOTAL NOISE VOLTAGE (120 Hz).

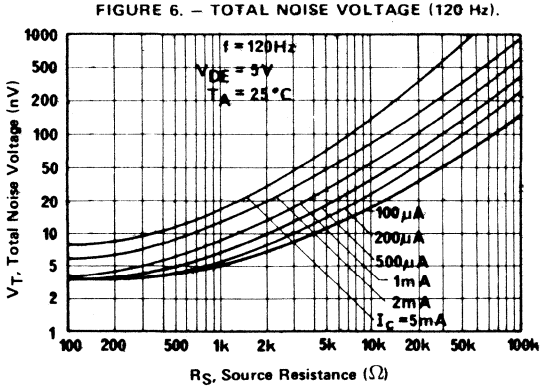


FIGURE 7. – NOISE FIGURE (120 Hz).

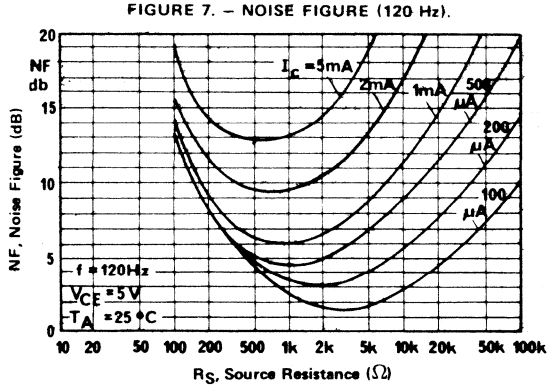


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FIGURE 8. – NORMALIZED DC CURRENT GAIN.

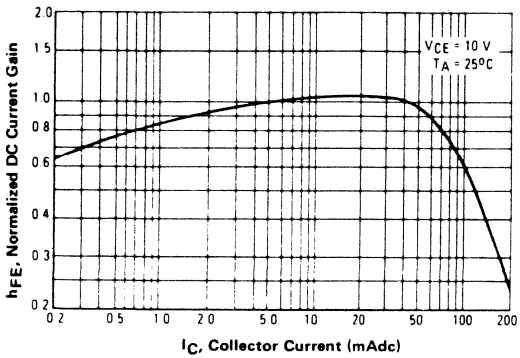


FIGURE 9. – "SATURATION" AND "ON" VOLTAGES.

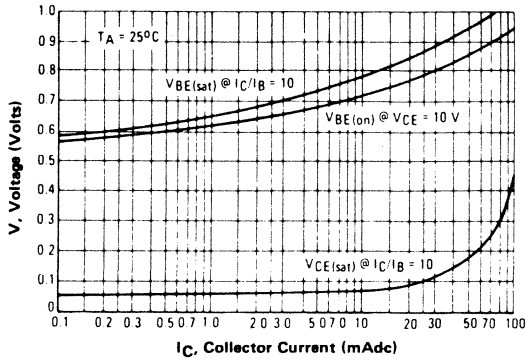


FIGURE 10. – CURRENT GAIN–BANDWIDTH PRODUCT.

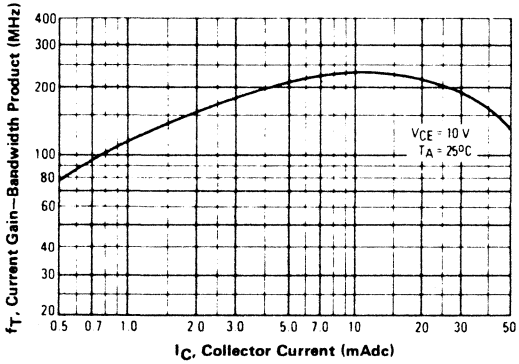


FIGURE 11. – CAPACITANCES.

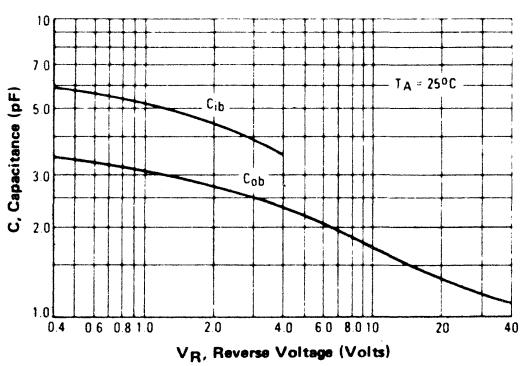


FIGURE 12. – OUTPUT ADMITTANCE.

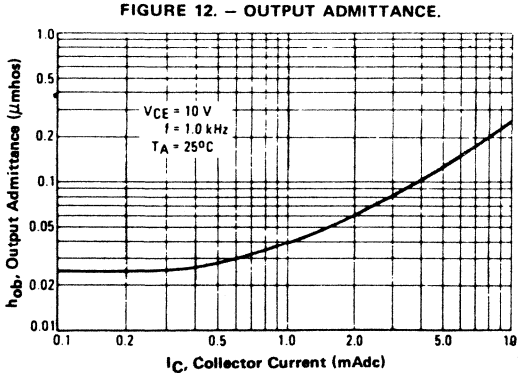
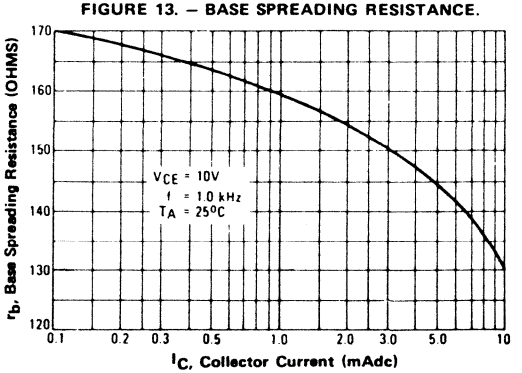


FIGURE 13. – BASE SPREADING RESISTANCE.

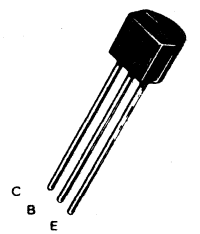


BC415
BC416

PNP SILICON ANNULAR♦
LOW NOISE, HIGH GAIN AMPLIFIER TRANSISTOR

- Low Wideband Noise Figure
  NF = 2.5dB max (30Hz-15KHz)
- Low Noise At Low Frequency
  V_T = 10nV/$\sqrt{Hz}$ max (120Hz)
- High Gain in 2 Ranges
  B range: 180 – 460
  C range: 380 – 800 } (2mA/5V)
- Full Applications Information

PNP SILICON
LOW NOISE
TRANSISTOR



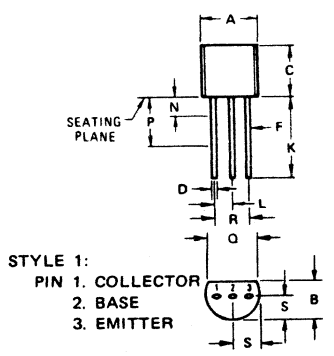
MAXIMUM RATINGS

Rating	Symbol	Value BC415	Value BC416	Unit
Collector-Emitter Voltage	V_{CEO}	35	45	Vdc
Collector-Base Voltage	V_{CBO}	45	50	Vdc
Emitter-Base Voltage	V_{EBO}	5		Vdc
Collector Current Continuous Peak	I_C	0.1 0.2		Adc Adc
Base-Current-Continuous	I_B	0.05		Adc
Total Device Dissipation at T_A = 25 °C Derate above 25 °C	P_D	350 2.81		mW mW/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	−55 to + 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	357	°C/W

♦ Annular Semiconductors Patented by Motorola Inc.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

4

ELECTRICAL CHARACTERISTICS (T_A = 25°C Unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Collector-Emitter Breakdown Voltage (I_C = 10mAdc, I_B = 0) BC415	BV_{CEO}	35			Vdc
BC416		45			
Collector-Base Breakdown Voltage (I_C = 10μAdc, I_E = 0) BC415	BV_{CBO}	45			Vdc
BC416		50			
Emitter-Base Breakdown Voltage (I_C = 10μAdc, I_C = 0)	BV_{EBO}	5			Vdc
Collector Cutoff Current (V_{CB} = 30Vdc, I_E = 0)	I_{CBO}			15	nAdc
(V_{CB} = 30Vdc, I_E = 0, T_A = + 125 °C)				5	μAdc
Emitter Cutoff Current (V_{EB} = 4Vdc, I_C = 0)	I_{EBO}			15	nAdc
On Characteristics					
DC Current Gain (I_C = 10μAdc, V_{CE} = 5Vdc) BC415B/BC416B	h_{FE}	100	150		
BC415C/BC416C		100	270		
(I_C = 2mAdc, V_{CE} = 5Vdc) BC415B/BC416B		180	290	460	
BC415C/BC416C		380	500	800	
Collector-Emitter Saturation Voltage	$V_{CE(S)}$				Vdc
(I_C = 10mAdc, I_B = 0.5mAdc)			0.075	0.25	
(I_C = 10mAdc, I_B = see note 1)			0.3	0.6	
(I_C = 100mAdc, I_B = 5mAdc, see note 2)			0.25		
Base-Emitter Saturation Voltage (I_C = 100mAdc, I_B = 5mAdc)	$V_{BE(S)}$		1.1		Vdc
Base-Emitter On Voltage	$V_{BE(ON)}$				Vdc
(I_C = 10μAdc, V_{CE} = 5 Vdc)			0.52		
(I_C = 100μAdc, V_{CE} = 5Vdc)			0.55		
(I_C = 2mAdc, V_{CE} = 5Vdc)		0.55	0.62	0.75	

Note 1: I_B is value for which I_C = 11mA at V_{CE} = 1V
Note 2: Pulse test = 300μs —— Duty Cycle = 2%

Characteristic	Symbol	Min	Typ	Max	Unit

Dynamic Characteristics

Current-Gain-Bandwidth Product (I_C = 10mAdc, V_{CE} = 5Vdc, f = 100MHz)	f_T		250		MHz
Collector-Base Capacitance (V_{CE} = 10Vdc, I_E = 0, f = 1MHz)	Ccbo		2.5		pF

h-Parameters (I_C = 2mAdc, V_{CE} = 5Vdc, f = 1KHz)

Input Impedance	h_{ie}				KΩ
BC415B/BC416B	(h_{11e})	3.2	6.0	8.5	
BC415C/BC416C		5.0	8.0	14.0	
Voltage Feedback Ratio	h_{re}				10^{-4}
BC415B/BC416B	(h_{12e})		3.5		
BC415C/BC416C			4.0		
Small Signal Current Gain	h_{fe}				
BC415B/BC416B	(h_{21e})	240	330	500	
BC415C/BC416C		450	600	900	
Output Admittance	h_{oe}				μ mhos
BC415B/BC416B	(h_{22e})		10	60	
BC415C/BC416C			12	110	

Noise Performance

Noise Figure (I_C = 200μAdc, V_{CE} = 5Vdc, R_S = 2KΩ, f = 30Hz – 15KHz)	NF		0.5	2.0	dB
Equivalent Input Noise Voltage (I_C = 200μAdc, V_{CE} = 5V, R_S = 2KΩ, f = 120Hz) See Application note, Section I	V_T		8	10	$nV/\sqrt{Hz}$
Equivalent Input Noise Voltage (I_C = 200μAdc, V_{CE} = 5V, R_S = 2KΩ, f = 10Hz – 50Hz) See Application note, Section II	V_T		74	110	$nV/\sqrt{Hz}$

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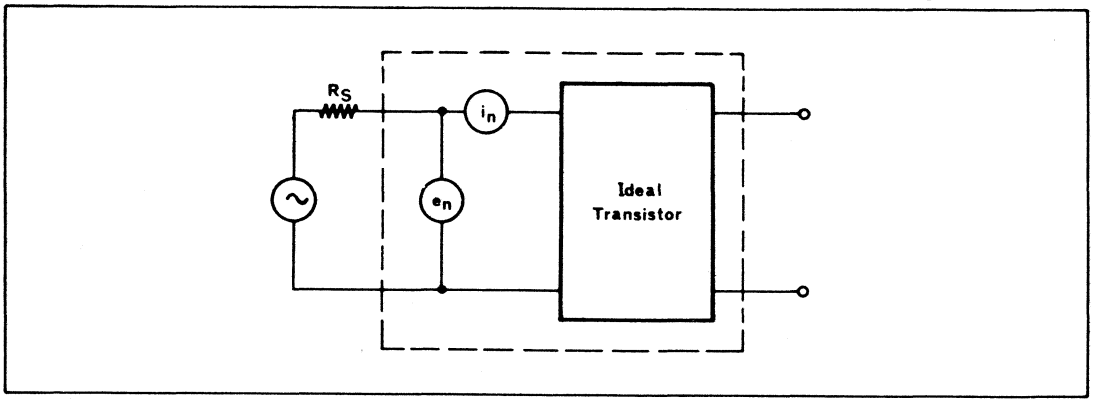
FIGURE 1. – TRANSISTOR NOISE MODEL.



NOISE APPLICATION NOTE

I. NOISE FIGURE RELATED TO V_T, e_n, and i_n

For a transistor, total noise at the input may be expressed as:

$$V_T = \left[e_n^2 + 4\,KT\,R_S + i_n^2 R_S^2\right]^{1/2} \qquad (1)$$

Where:

V_T = total noise voltage at the transistor input (Volts/$\sqrt{Hz}$)
e_n = noise voltage of the transistor referred to the input (figures 2 & 3)
i_n = noise current of the transistor referred to the input (figure 4)
K = Boltzmann's constant (1.38×10^{-23}j/°K)
T = Temperature of the source resistance (°K)
R_S = Source resistance (Ohms)

Example:
Find the total noise at the input of a BC414 for a collector current of 1mA and a source impedance of 1KΩ at a frequency of 120Hz and a temperature of 25 °C.

1. V_T is calculated from e_n, i_n

Read $e_n = 4.5nV/\sqrt{Hz}$ from figure 2 or figure 3 (Note that this is for a one cycle bandwidth)
Read $i_n = 5.8pA/\sqrt{Hz}$ from figure 4

$$V_T = [(4.5 \times 10^{-9})2 + (4).(1.38 \times 10^{-23}).(300).(1 \times 10^3) + (5.8 \times 10^{-12})2.(1 \times 10^3)2]^{1/2}$$

Thus: $\boxed{V_T = 8.2nV}$

This checks with the value of 8nV shown in figure 6.

2. Noise figure is calculated from V_T

Noise figure is defined as:

$$NF = 20 \log_{10} \frac{\text{total noise voltage}}{\text{noise voltage contributed by source resistance}}$$

or

$$NF = 20 \log_{10} \left[\frac{V_T^2}{4\,KT\,R_S}\right]^{1/2}$$

Noise figure can be calculated for the above example as follows:

$$NF = 20 \log_{10} \left[\frac{(8 \times 10^{-9})2}{16.6 \times 10^{-18}}\right]^{1/2}$$

Thus: $\boxed{NF = 5.9\ dB}$

This checks with the values of 6 dB read from figure 7;

To minimize noise in a transistor stage, one might use figure 7 and deduce that noise is minimized when Noise Figure is minimum. This is not necessarily true as shown by figure 6 where the total noise voltage is a minimum at small values of source impedance.
This can be seen from equation (1) which shows that total noise is a direct function of source resistance.

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Noise over a frequency band can be handled in one of two ways depending upon whether total transistor noise is constant or variable over the bandwidth of interest:

1. For constant transistor noise, multiply, V_T by the square root of bandwidth. i.e., $V_T = V_T \cdot f.^{1/2}$
2. For variable transistor noise integrate the spectral density V_T (where $\triangle f = 1Hz$), over the bandwidth of interest.

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Find the total noise at the input in the bandwidth $f_1 = 10Hz$, $f_2 = 50Hz$ at $I_C = 200\mu A$ and $R_S = 2K\Omega$

This example corresponds to the popular "FLICKER NOISE" test shown on many data sheets.

$$V_T^2 = \int_{-\infty}^{+\infty} V_T(f) \times [G(f)]^2 \, df$$
$$(f_1 - f_2)$$

where:

$$V_{T(f)}^2 = e_{n(f)}^2 + 4KT\,R_S + i_{n(f)}^2 R_S^2$$

$e_{n(f)}$ and 4 KT R_S are constant in the bandwidth

$$i_{n(f)} = \frac{i_n^2\ (1\ Hz)}{f}\ \text{(1/f noise spectrum density)}$$

G(f) bandpass filter

$= 1$ for $f \in (f_1, f_2)$

$= 0$ for $f \notin (f_1, f_2)$

after integration:

$$V_{T(f_1-f_2)}^2 = (e_{n(f1)}^2 + 4\,KT\,R_S) \times (f_2-f_1) + R_S^2\, i_{n(f1)}^2 \times f1 \times i_n\,(f1)\frac{f2}{f1}$$

Now:

$e_n = 5\ nV/\sqrt{Hz}$ at 10 Hz (from figure 2)

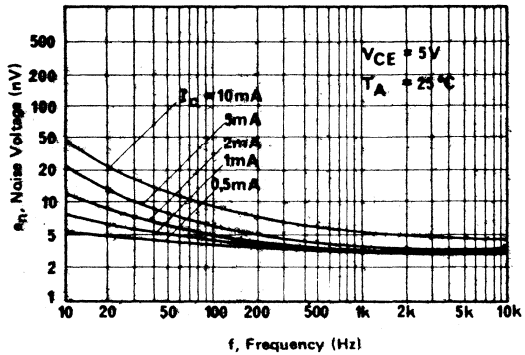
$i_n = 7\ pA/\sqrt{Hz}$ at 10 Hz (from figure 4)

$$V_T^2\,(10Hz-50Hz) = [(25 + 33.1)40 + 196 \times 10 \times 1.6].10^{-18}$$

Thus: $\boxed{V_T(10Hz-50Hz) = 74\ nV}$

4

FIGURE 2. – NOISE VOLTAGE vs FREQUENCY.



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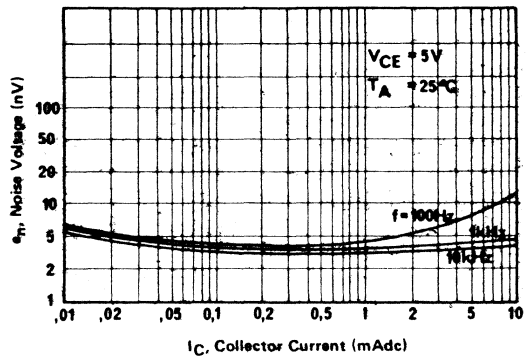
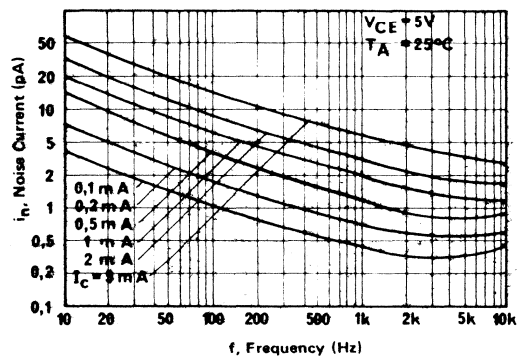


FIGURE 4. – NOISE CURRENT.



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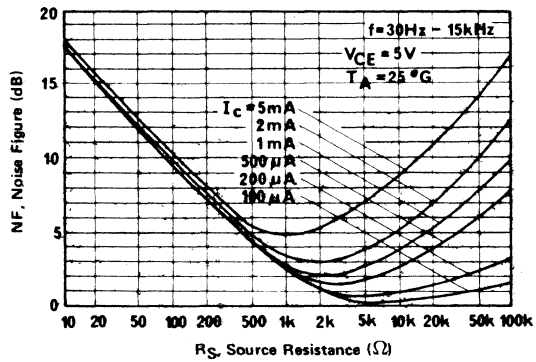
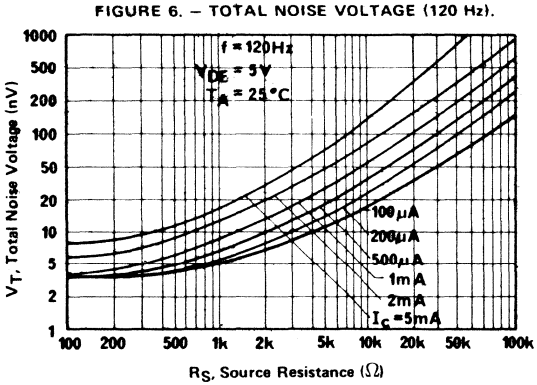


FIGURE 6. – TOTAL NOISE VOLTAGE (120 Hz).



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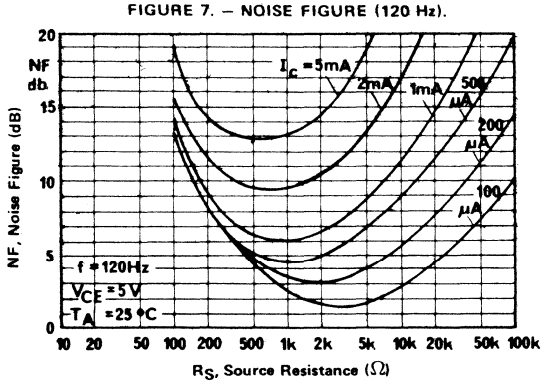

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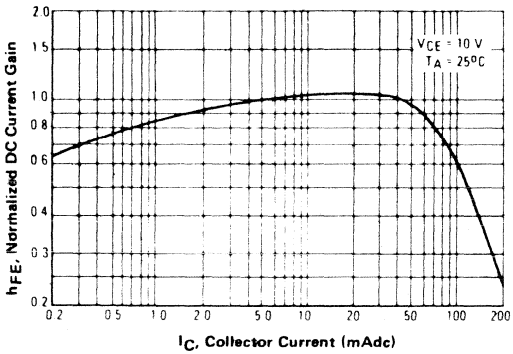

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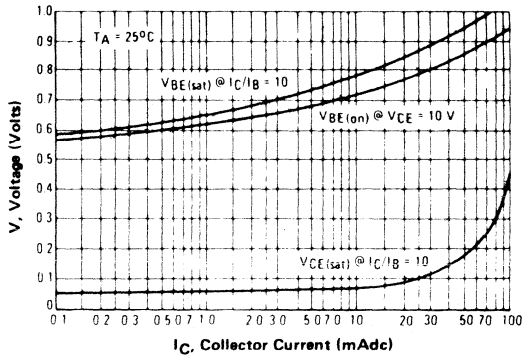

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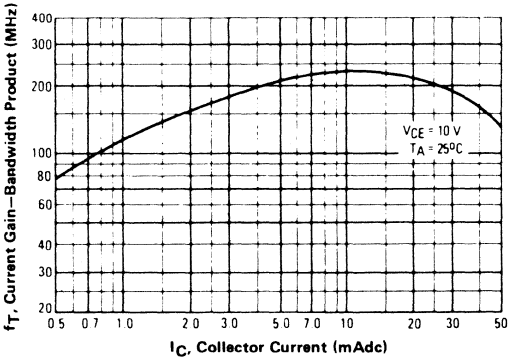

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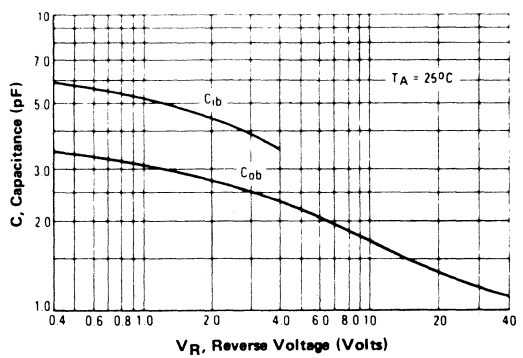

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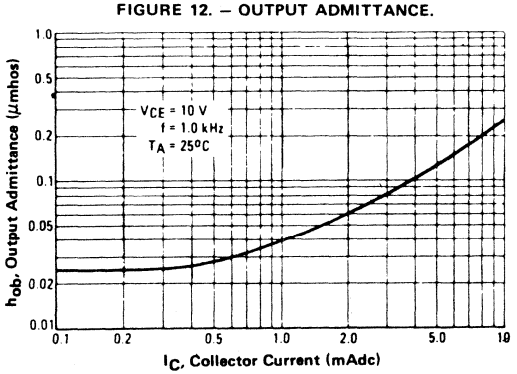

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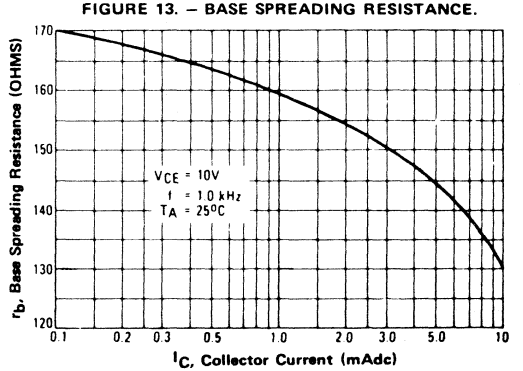

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BC445
BC447 • BC449

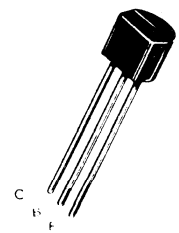
PNP SILICON ANNULAR* TRANSISTORS

... designed for use as high voltage driver and output transistors, particularly suitable as Power Darlington drivers.

- High Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 60 Vdc (Min) I_C = 1.0 mAdc — BC445
  = 80 Vdc (Min) I_C = 1.0 mAdc — BC447
  = 100 Vdc (Min) I_C = 1.0 mAdc — BC449
- Excellent Current Gain Linearity — 1.0 mAdc to 100 mAdc
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.25 Vdc (Max) I_C = 100 mAdc
- Available in standardized gain groups (A/B)

NPN SILICON

HIGH VOLTAGE TRANSISTORS



For standard package order BC445 447 449

For TO - 18 configuration order
BC445-18 BC447-18 BC449-18

For TO - 5 configuration order
BC445-5 BC447-5 BC449-5

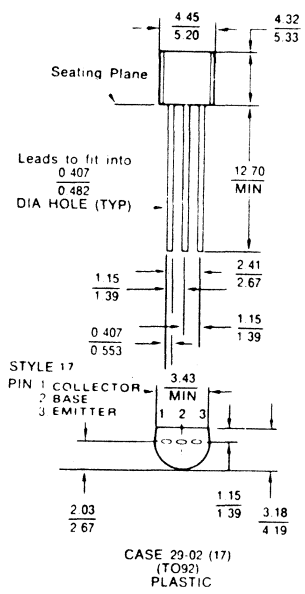
MAXIMUM RATINGS

Rating	Symbol	BC445	BC447	BC449	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5			Vdc
Collector-Current-Continuous	I_C	300			mAdc
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	625 5.0			mW mW/°C
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	1.5 12.0			W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max.	Unit
Thermal resistance, Junction to case	Θ_{JC}	83.3	°C/W
Thermal resistance, Junction to Ambient	Θ_{JA}	200	°C/W

* Annular Semiconductors patented by Motorola Inc



CASE 29-02 (17)
(TO92)
PLASTIC

Dimensions in millimeters

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage* (I_C = 1.0 mAdc, I_B = 0) BC445	BV_{CEO}	60	—	—	Vdc
BC447		80	—	—	
BC449		100	—	—	
Collector-Base Breakdown Voltage (I_C = 100 μA, I_E = 0) BC445	BV_{CBO}	60	—	—	Vdc
BC447		80	—	—	
BC449		100	—	—	
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	5	—	—	Vdc
Collector cutoff current	I_{CBO}				nAdc
V_{CB} = 30 Vdc — I_E = 0 BC445		—	—	100	
V_{CB} = 40 Vdc — I_E = 0 BC447		—	—	100	
V_{CB} = 60 Vdc — I_E = 0 BC449		—	—	100	
ON CHARACTERISTICS*					
DC Current Gain — I_C = 2mA, V_{CE} = 5V full range	h_{FE}	50		460	
A		120		220	
BC445/447 only B		180		460	
I_C = 10mA, V_{CE} = 5V full range		50			
A		100			
BC445/447 only B		160			
I_C = 100mA, V_{CE} = 5V full range		50			
A		60			
BC445/447 only B		90			
Collector-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{CE(sat)}$	—	0.1	0.25	Vdc
Base-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{BE(sat)}$	—	0.85	—	Vdc
Base-Emitter On Voltage (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	—	0.8	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain - Bandwidth Product (I_C = 50 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	f_T	100	250	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	3.0	—	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)	C_{ib}	—	16	—	pF

* Pulse test - Pulse width ≤ 300 μs - Duty cycle 2%

4

FIG. 1 — DC CURRENT GAIN

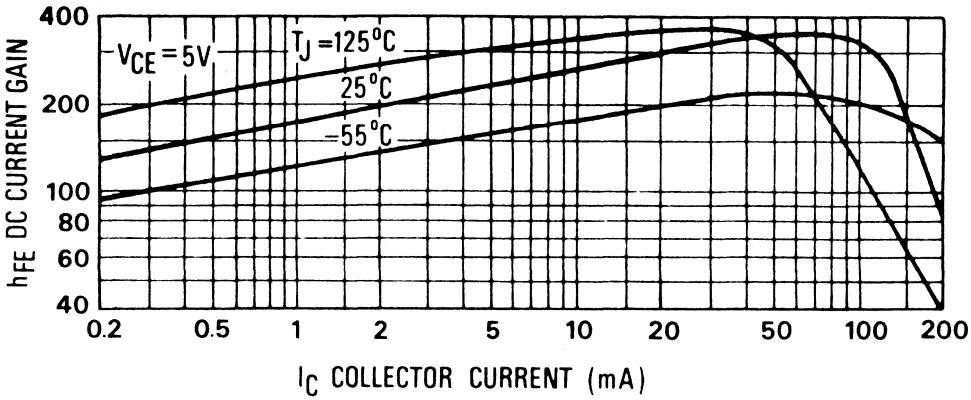


FIG. 2 — "ON" VOLTAGES

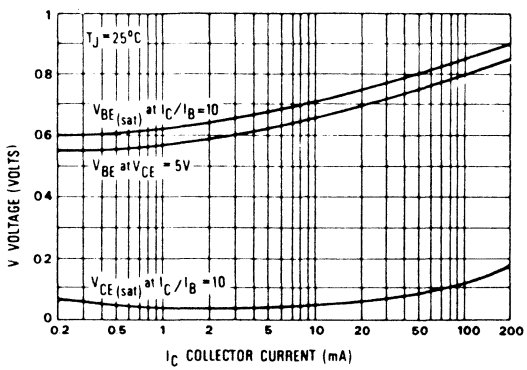


FIG. 3 — COLLECTOR SATURATION REGION

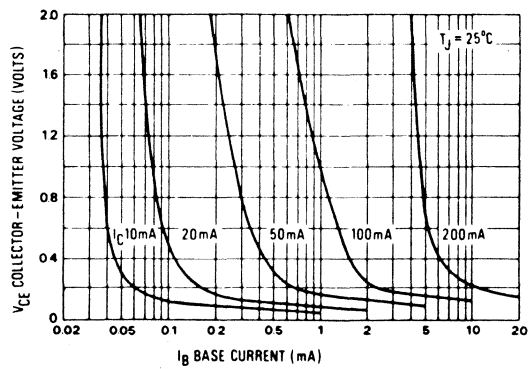


FIG. 4 — BASE-EMITTER TEMPERATURE COEFFICIENT

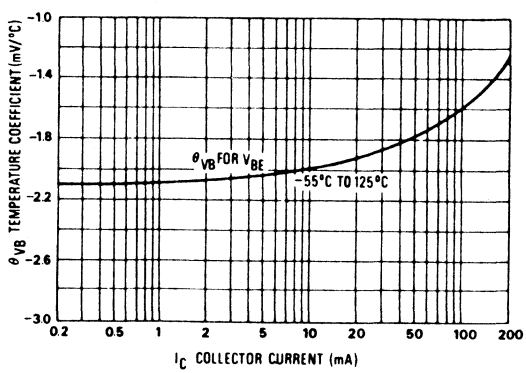


FIG. 5 — CURRENT GAIN — BANDWIDTH PRODUCT

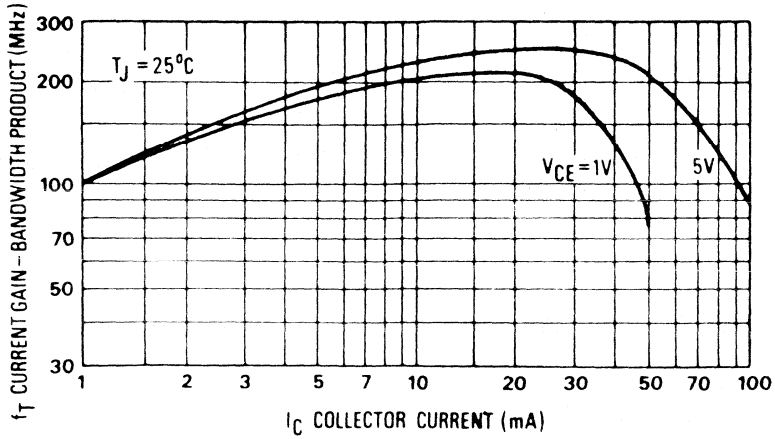
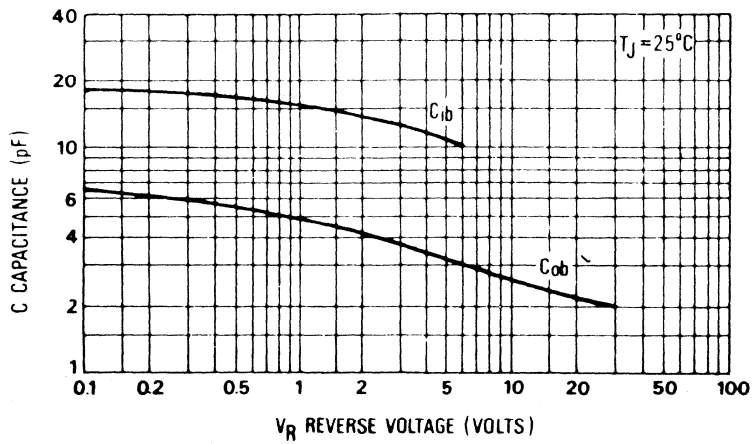


FIG. 6 — CAPACITANCE



4

BC446
BC448 • BC450

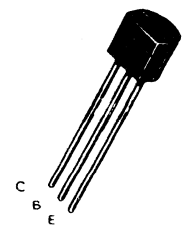
PNP SILICON ANNULAR* TRANSISTORS

... designed for use as high voltage driver and output transistors, particularly suitable as Power Darlington drivers.

- High Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 60 Vdc (Min) I_C = 1.0 mAdc — BC446
  = 80 Vdc (Min) I_C = 1.0 mAdc — BC448
  = 100 Vdc (Min) I_C = 1.0 mAdc — BC450
- Excellent Current Gain Linearity — 1.0 mAdc to 100 mAdc
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.25 Vdc (Max) I_C = 100 mAdc
- Available in standardized gain groups (A/B)

PNP SILICON

HIGH VOLTAGE TRANSISTORS



For standard package order BC446/BC448/BC450

For TO - 18 configuration order
BC446-18/BC448-18/BC450-18

For TO - 5 configuration order
BC446-5/BC448-5/BC450-5

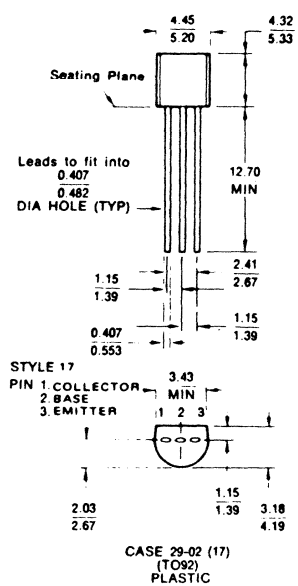
MAXIMUM RATINGS

Rating	Symbol	BC446	BC448	BC450	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5			Vdc
Collector-Current-Continuous	I_C	300			mAdc
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	625 5.0			mW mW/°C
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	1.5 12.0			W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max.	Unit
Thermal resistance, Junction to case	Θ_{JC}	83.3	°C/W
Thermal resistance, Junction to Ambient	Θ_{JA}	200	°C/W

* Annular Semiconductors patented by Motorola Inc



CASE 29-02 (17)
(TO92)
PLASTIC

Dimensions in millimeters

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage* (I_C = 1.0 mAdc, I_B = 0) BC446	BV_{CEO}	60	—	—	Vdc
BC448		80	—	—	
BC450		100	—	—	
Collector-Base Breakdown Voltage (I_C = 100 μA, I_E = 0) BC446	BV_{CBO}	60	—	—	Vdc
BC448		80	—	—	
BC450		100	—	—	
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	4.0	—	—	Vdc
Collector cutoff current	I_{CBO}				nAdc
V_{CB} = 30 Vdc — I_E = 0 BC446		—	—	100	
V_{CB} = 40 Vdc — I_E = 0 BC448		—	—	100	
V_{CB} = 60 Vdc — I_E = 0 BC450		—	—	100	
ON CHARACTERISTICS*					
DC Current Gain — I_C = 2mA, V_{CE} = 5V full range	h_{FE}	50		460	
A		120		220	
BC446/448 only B		180		460	
I_C = 10mA, V_{CE} = 5V full range		50			
A		100			
BC446/448 only B		160			
I_C = 100mA, V_{CE} = 5V full range		50			
A		60			
BC446/448 only B		90			
Collector-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{CE(sat)}$	—	0.125	0.25	Vdc
Base-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{BE(sat)}$	—	0.85	—	Vdc
Base-Emitter On Voltage (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	—	0.76	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain - Bandwidth Product (I_C = 50 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	f_T	100	200	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	3.0	—	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)	C_{ib}	—	20	—	pF

* Pulse test - Pulse width ≤ 300 μs - Duty cycle 2%

4

FIG. 1 — DC CURRENT GAIN

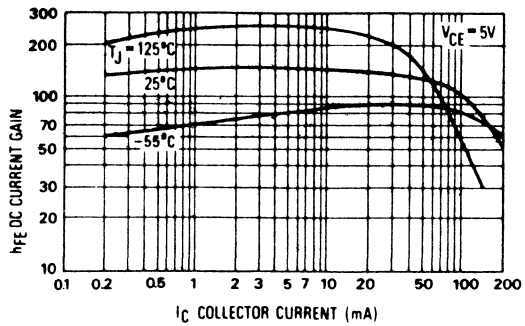


FIG. 2 — "ON" VOLTAGES

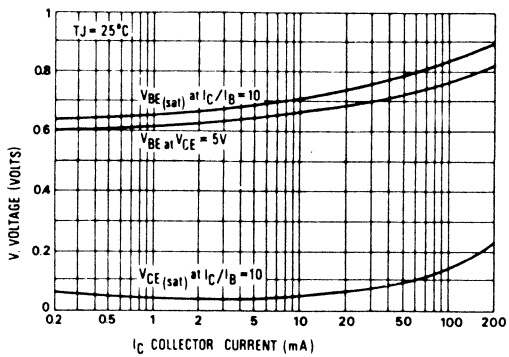


FIG. 3 — COLLECTOR SATURATION REGION

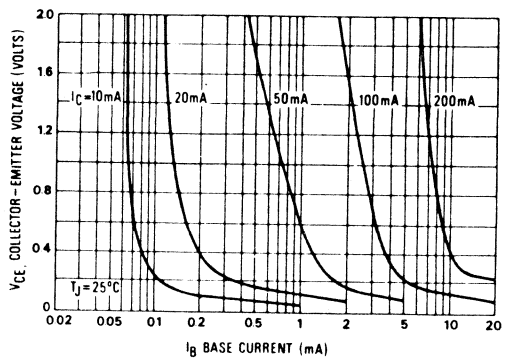


FIG. 4 — BASE-EMITTER TEMPERATURE COEFFICIENT

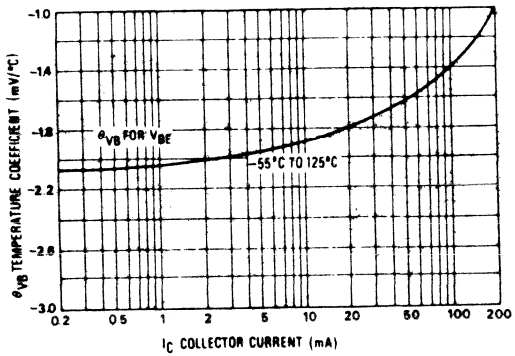


FIG. 5 — CAPACITANCE

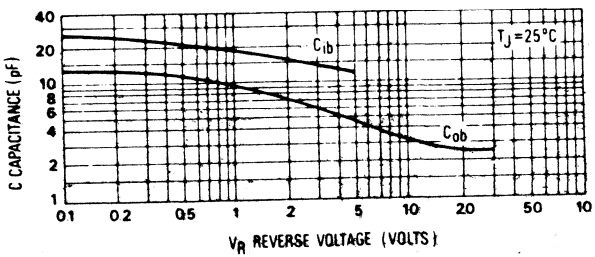
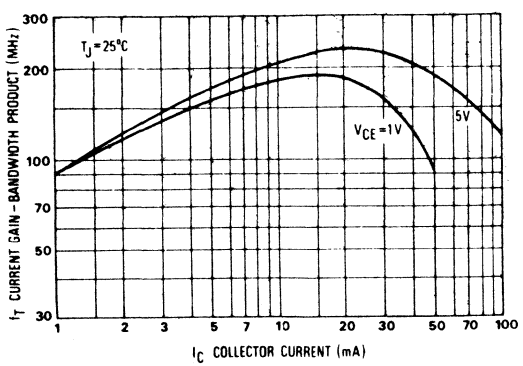


FIG. 6 — BANDWIDTH PRODUCT



BC485
BC487 • BC489

NPN SILICON ANNULAR* TRANSISTORS

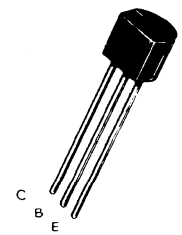
... designed for use as High Voltage-High Current driver and output transistors

- High Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 45 Vdc (Min) I_C = 1.0 mAdc — BC485
  = 60 Vdc (Min) I_C = 1.0 mAdc — BC487
  = 80 Vdc (Min) I_C = 1.0 mAdc — BC489
- Excellent Current-Gain Linearity — 1.0 mAdc to 100 mAdc
- Good h_{FE} up to 1 Amp.
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.2 Vdc (Typ) @ I_C = 500 mAdc
- Available in standardized gain groups (L/A/B)

NPN SILICON

HIGH VOLTAGE - HIGH CURRENT

TRANSISTORS



For standard package order BC485/BC487/BC489

For TO - 18 configuration order
BC485-18/BC487-18/BC489-18

For TO - 5 configuration order
BC485-5/BC487-5/BC489-5

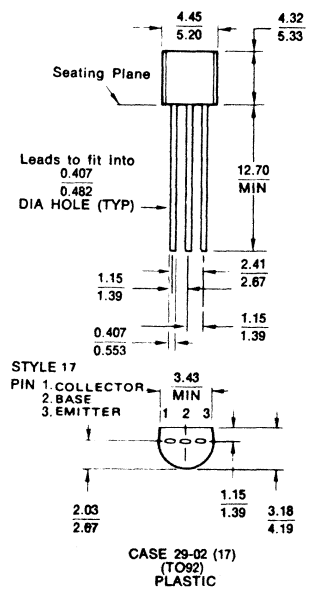
MAXIMUM RATINGS

Ratings	Symbol	BC485	BC487	BC489	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	Vdc
Emitter-Base Voltage	V_{EB}		5		Vdc
Collector Current-Continuous	I_C		1.0		Adc
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D		625 5.0		mW mW/°C
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D		1.5 12.0		W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−55 to +150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	Θ_{JC}	0.083	°C/mW
Thermal Resistance, Junction to Ambient	* Θ_{JA}	0.20	°C/mW

* Annular Semiconductors patented by Motorola Inc



CASE 29-02 (17)
(TO92)
PLASTIC

Dimensions in millimeters

ELECTRICAL CHARACTERISTICS (T_A = 25 C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage* (I_C = 10 mAdc, I_B = 0) BC485	BV_{CEO}	45	—	—	Vdc
BC487		60	—	—	
BC489		80	—	—	
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0) BC485	BV_{CBO}	45	—	—	Vdc
BC487		60	—	—	
BC489		80	—	—	
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	5.0	—	—	Vdc
Collector cutoff current	I_{CBO}				nAdc
V_{CB} = 30 Vdc — I_E = 0 BC485		—	—	100	
V_{CB} = 40 Vdc — I_E = 0 BC487		—	—	100	
V_{CB} = 60 Vdc — I_E = 0 BC489		—	—	100	
ON CHARACTERISTICS*					
DC Current Gain	h_{FE}				
I_C = 10 mAdc — V_{CE} = 2.0 Vdc		40			
I_C = 100 mAdc — V_{CE} = 2.0 Vdc					
Full Range		60		400	
— L		60	120	150	
— A		100	160	250	
— B		160	260	400	
I_C = 1 Ampdc — V_{CE} = 5.0 Vdc		15			
Collector Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
I_C = 500 mAdc — I_B = 50 mAdc		—	0.2	0.50	
I_C = 1Adc — I_B = 100 mAdc		—	0.3	—	
Base Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc)	$V_{BE(sat)}$	—	0.85	1.20	Vdc
I_C = 1 Ampdc — I_B = 100 mAdc			0.90		
DYNAMIC CHARACTERISTICS					
Current Gain - Bandwidth Product (I_C = 50 mAdc, V_{CE} = 2.0 Vdc, f= 100 MHz)	f_T	—	200	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	7	—	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)	C_{ib}	—	50	—	pF

* Pulse test - Pulse width = 300 μs - Duty cycle 2 %

4

FIG. 1 — ACTIVE REGION SAFE OPERATING AREA

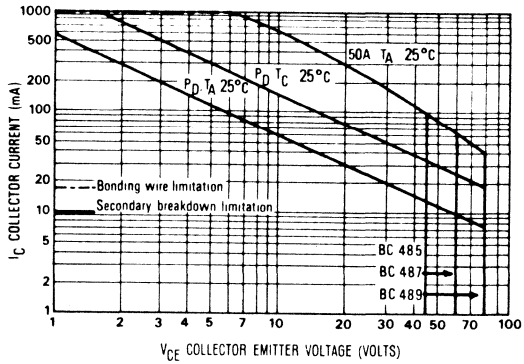


FIG. 2 — DC CURRENT GAIN

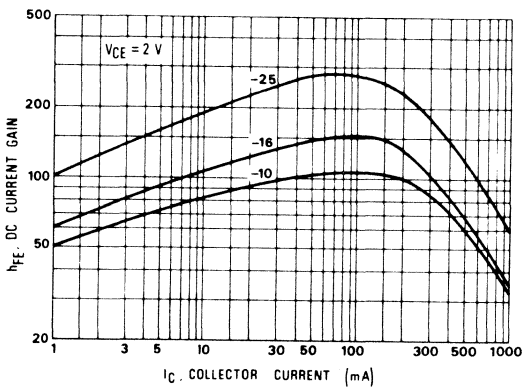


FIG. 3 — CURRENT GAIN BANDWIDTH PRODUCT

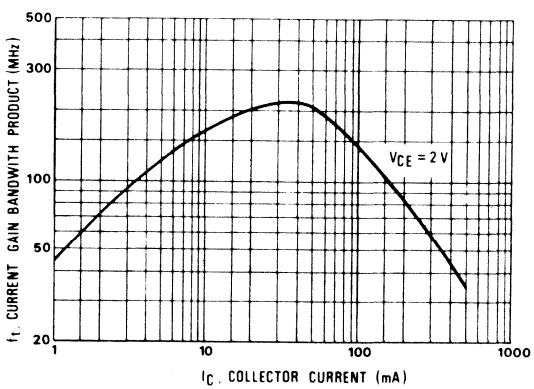


FIG. 4 — "SATURATION" AND "ON" VOLTAGES

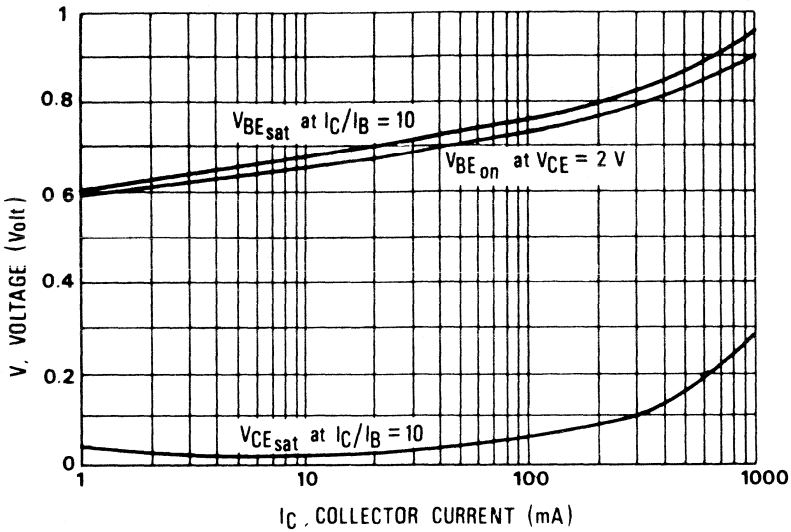
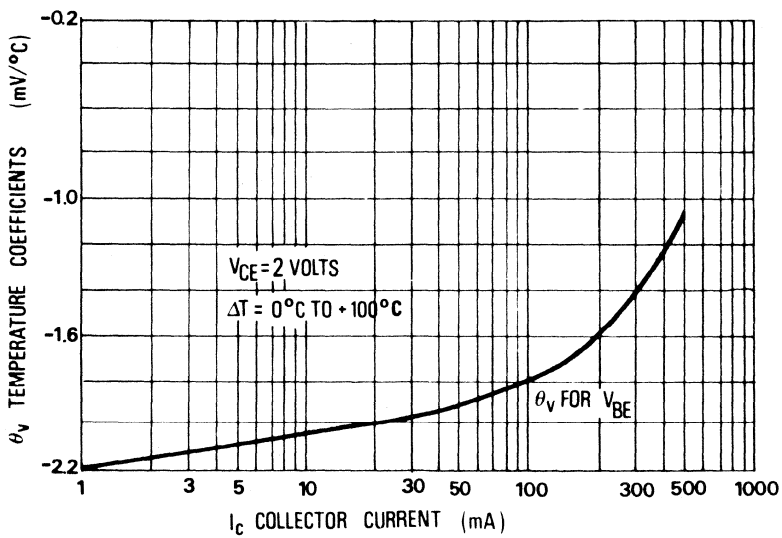


FIG. 5 — TEMPERATURE COEFFICIENTS



4

BC486
BC488 • BC490

PNP SILICON ANNULAR* TRANSISTORS

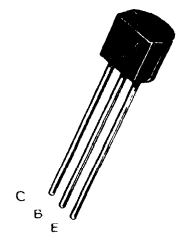
... designed for use as High Voltage-High Current driver and output transistors

- High Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 45 Vdc (Min) I_C = 1.0 mAdc — BC 486
  = 60 Vdc (Min) I_C = 1.0 mAdc — BC 488
  = 80 Vdc (Min) I_C = 1.0 mAdc — BC 490
- Excellent Current-Gain Linearity — 1.0 mAdc to 100 mAdc
- Good h_{FE} up to 1 Amp.
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.2 Vdc (Typ) @ I_C = 500 mAdc
- Available in standardized gain groups (L/A/B)

PNP SILICON

HIGH VOLTAGE - HIGH CURRENT

TRANSISTORS



For standard package order BC486/BC488/BC490

For TO - 18 configuration order
BC486-18/BC488-18/BC490-18

For TO - 5 configuration order
BC486-5/BC488-5/BC490-5

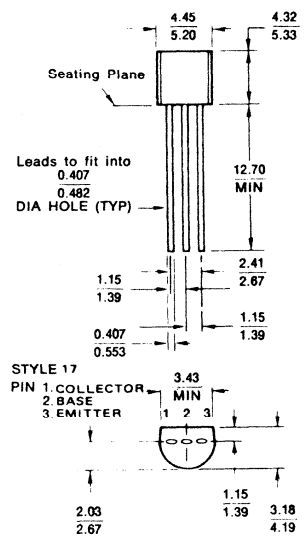
MAXIMUM RATINGS

Ratings	Symbol	BC486	BC488	BC490	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	Vdc
Emitter-Base Voltage	V_{EB}	4			Vdc
Collector Current-Continuous	I_C	1.0			Adc
Total Device Dissipation T_A = 25°C Derate above 25 C	P_D	625 5.0			mW mW/°C
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	1.5 12.0			W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	—55 to +150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	Θ_{JC}	0.083	°C/mW
Thermal Resistance, Junction to Ambient	Θ_{JA}	0.20	°C/mW

* Annular Semiconductors patented by Motorola Inc



CASE 29-02 (17)
(TO92)
PLASTIC

Dimensions in millimeters

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage* (I_C = 10 mAdc, I_B = 0) BC486	BV_{CEO}	45	—	—	Vdc
BC488		60	—	—	
BC490		80	—	—	
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0) BC486	BV_{CBO}	45	—	—	Vdc
BC488		60	—	—	
BC490		80	—	—	
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	4.0	—	—	Vdc
Collector cutoff current	I_{CBO}				nAdc
V_{CB} = 30 Vdc — I_E = 0 BC486		—	—	100	
V_{CB} = 40 Vdc — I_E = 0 BC488		—	—	100	
V_{CB} = 60 Vdc — I_E = 0 BC490		—	—	100	
ON CHARACTERISTICS*					
DC Current Gain	h_{FE}				
I_C = 10 mAdc — V_{CE} = 2.0 Vdc		40			
I_C = 100 mAdc — V_{CE} = 2.0 Vdc					
Full Range		60	—	400	
— L		60	100	150	
— A		100	140	250	
— B		160	260	400	
I_C = 1 Ampdc — V_{CE} = 5.0 Vdc		15			
Collector Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
I_C = 500 mAdc — I_B = 50 mAdc		—	0.25	0.50	
I_C = 1Adc — I_B = 100 mAdc		—	0.50	—	
Base Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc)	$V_{BE(sat)}$	—	0.90	1.20	Vdc
I_C = 1 Ampdc — I_B = 100 mAdc			1.00		
DYNAMIC CHARACTERISTICS					
Current Gain - Bandwidth Product (I_C = 50 mAdc, V_{CE} = 2.0 Vdc, f = 100 MHz)	f_T	—	150	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	9	—	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)	C_{ib}	—	110	—	pF

* Pulse test - Pulse width = 300 μs - Duty cycle 2 %

4

FIG. 1 — ACTIVE REGION SAFE OPERATING AREA

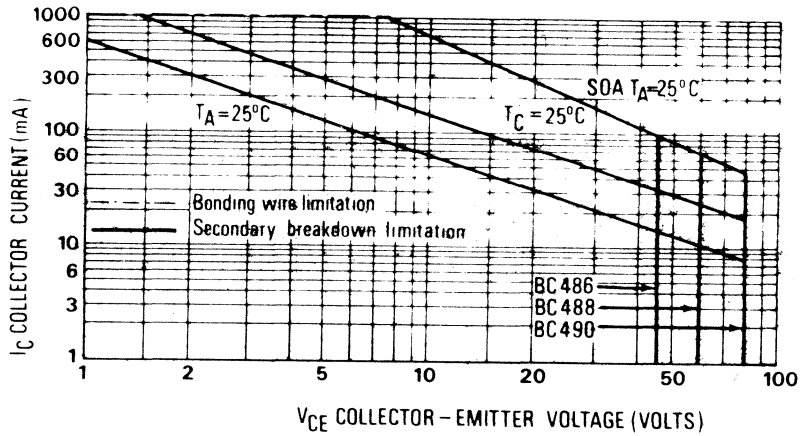


FIG. 2 — DC CURRENT GAIN

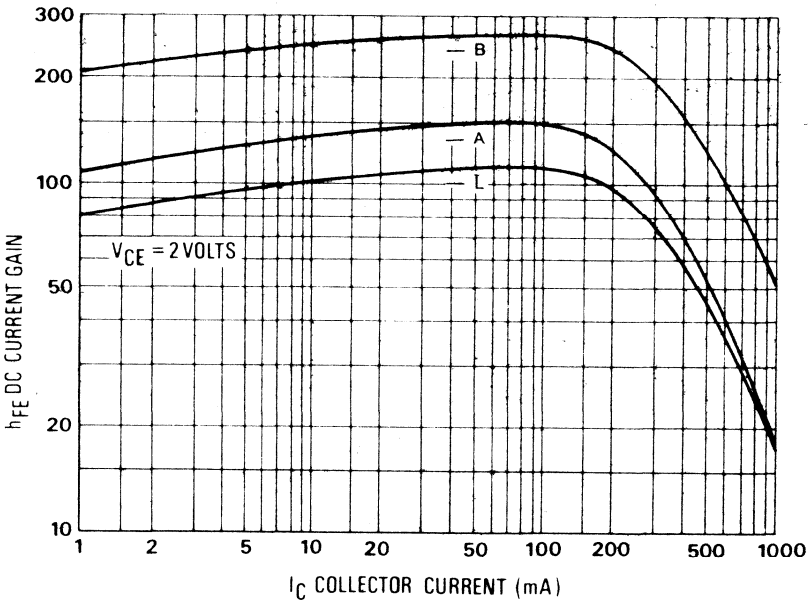


FIG. 3 — CURRENT GAIN BANDWIDTH PRODUCT

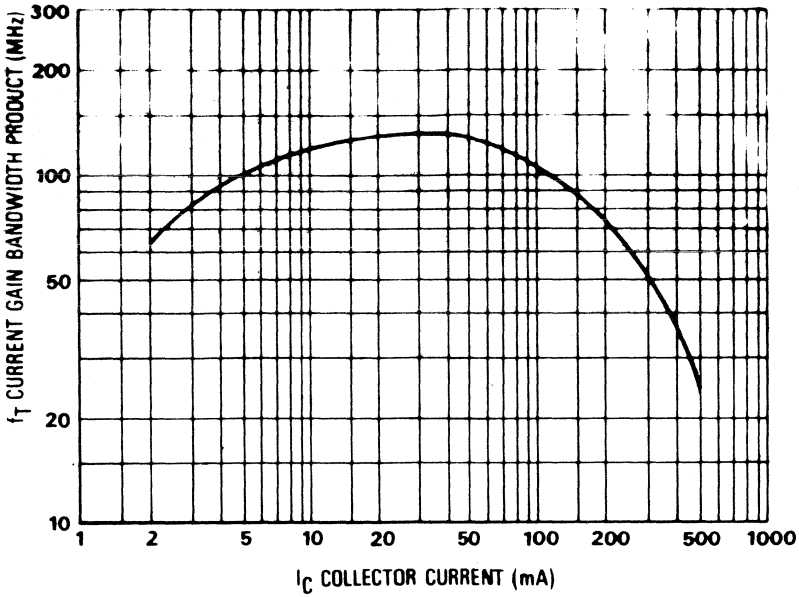


FIG. 4 — "SATURATION" AND "ON" VOLTAGES

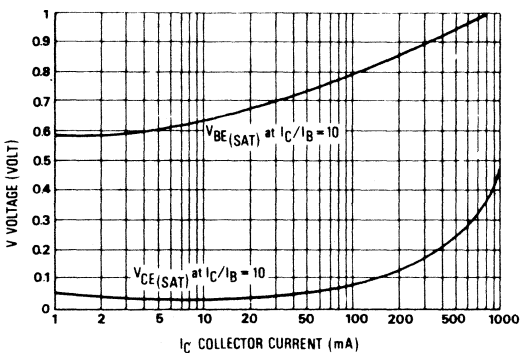
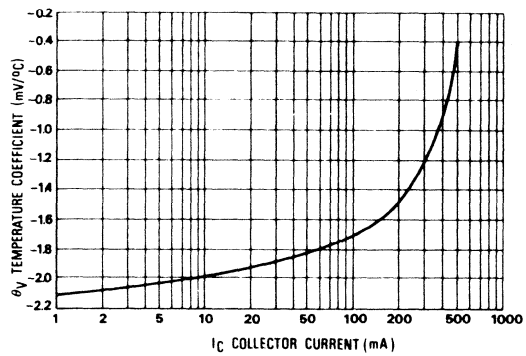


FIG. 5 — TEMPERATURE COEFFICIENTS



4

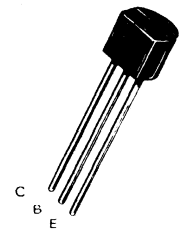
BC546
BC547 • BC548

NPN SILICON ANNULAR* TRANSISTORS

. . . designed for general-purpose use in audio, radio, and television applications.

- High Breakdown Voltage—
  BV_{CEO} = 65 Vdc (Min) @ I_C = 1.0 mAdc
- Low Collector-Emitter Saturation Voltage—
  $V_{CE(sat)}$ = 0.6 Vdc (Max) @ I_C = 100 mAdc
- Low output capacitance
  C_{ob} = 4.5 pf (Max) @ V_{CB} = 10 Vdc
- Complementary to PNP BC 556/557/558
- One-Piece, Injection-Molded Unibloc † Package

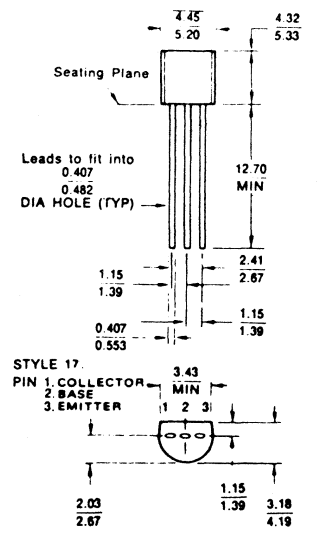
NPN SILICON AMPLIFIER TRANSISTORS



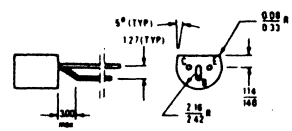
For standard package order BC546/547/548
For TO-18 configuration order BC546-18/547-18/548-18
For TO-5 configuration order BC546-5/547-5/548-5

MAXIMUM RATINGS

Rating	Symbol	BC546	BC547	BC548	Unit
Collector-Emitter Voltage	V_{CEO}	65	45	30	Vdc
Collector-Base Voltage	V_{CB}	80	50	30	Vdc
Emitter-Base Voltage	V_{EB}	6			Vdc
Collector-Current-Continuous Peak	I_C I_{CM}	100 200			mAdc
Base-Current peak	I_{BM}	200			mAdc
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	625 5			mW mW/°C
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	1.5 12			W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150			°C



CASE 29-02 (17)
(TO92)
PLASTIC



TO - 18 configuration

Dimensions in millimeters

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal resistance, Junction to case	Θ_{JC}	0.083	°C/mW
Thermal resistance, Junction to Ambient	Θ_{JA}	0.20	°C/mW

* Annular Semiconductors patented by Motorola Inc

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Characteristics	Type	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 1 mAdc, I_B = 0)	BC 546	BV_{CEO}	65			Vdc
	BC 547		45			
	BC 548		30			
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BC 546	BV_{EBO}	6			Vdc
	BC 547		6			
	BC 548		6			
Collector Cutoff Current		I_{CES}				ηAdc
(V_{CE} = 70 Vdc, V_{BE} = 0)	BC 546			0.20	15	
(V_{CE} = 50 Vdc, V_{BE} = 0)	BC 547			0.20	15	
(V_{CE} = 35 Vdc) V_{BE} = 0)	BC 548			0.20	15	
(V_{CE} = 30 V, T_A = 125 °C	BC 546				4	μAdc
	BC 547				4	
	BC 548				4	
ON CHARACTERISTICS						
DC Current Gain		h_{FE}				
(I_C = 10 μAdc, V_{CE} = 5 Vdc)	BC 546A/547A/548A			90		
	BC 546B/547B/548B			150		
	BC 548C			270		
(I_C = 2 mAdc, V_{CE} = 5 Vdc)	BC 546		120		450	
	BC 547		120		450	
	BC 548		120		800	
	BC 546A/547A/548A		120	180	220	
	BC 546B/547B/548B		200	290	450	
	BC 548C		420	520	800	
(I_C = 100 mAdc, V_{CE} = 5 Vdc)	BC 546A/547A/548A			120		
	BC 546B/547B/548B			180		
	BC 548C			300		
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 10 mA, I_B = 0.5 mA)				0.09	0.25	
(I_C = 100 mAdc, I_B = 5 mAdc)				0.2	0.60	
(I_C = 10 mA, I_B = See Note 1)				0.3	0.6	
Base Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 10 mA, I_B = 0.5 mA)				0.7		
Base-Emitter On Voltage		$V_{BE(on)}$				Vdc
(I_C = 2 mAdc, V_{CE} = 5 Vdc)			0.55		0.70	
(I_C = 10 mAdc, V_{CE} = 5 Vdc)					0.77	

Note 1: I_B is value for which I_C = 11 mA at V_{CE} = 1 V.

4

FIGURE 1 – NORMALIZED DC CURRENT GAIN

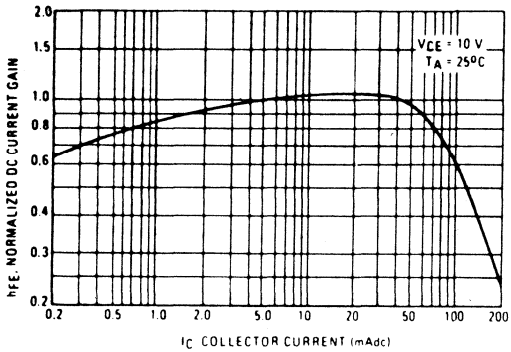


FIGURE 2 – "SATURATION" AND "ON" VOLTAGES

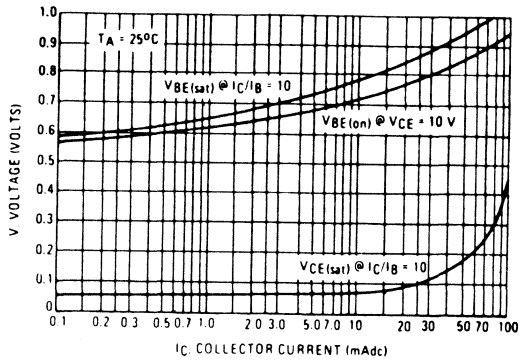


FIGURE 3 – COLLECTOR SATURATION REGION

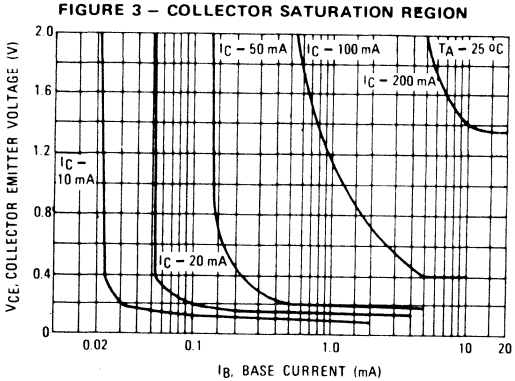


FIGURE 4 – BASE EMITTER TEMPERATURE COEFFICIENT

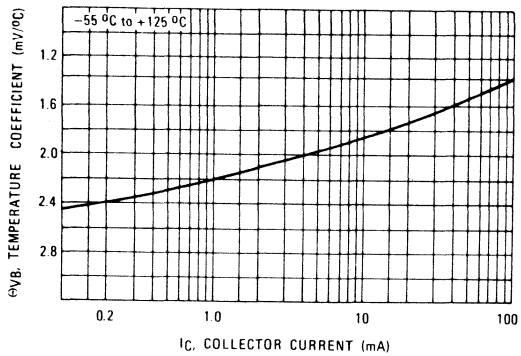


FIGURE 5 – CAPACITANCES

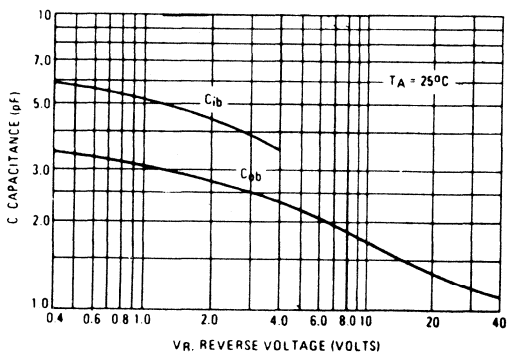


FIGURE 6 – CURRENT GAIN–BANDWIDTH PRODUCT

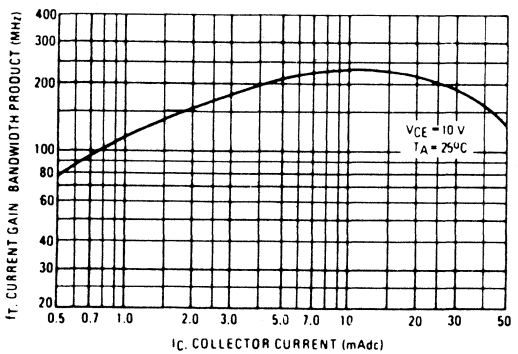


FIGURE 7 – DC CURRENT GAIN

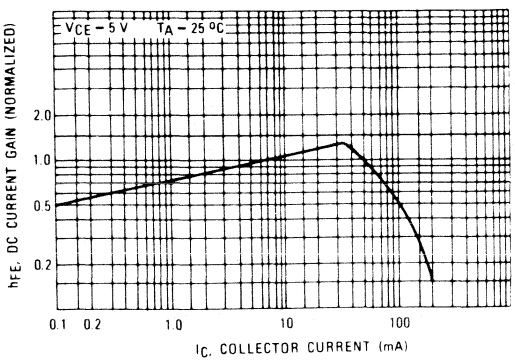


FIGURE 8 – "ON" VOLTAGE

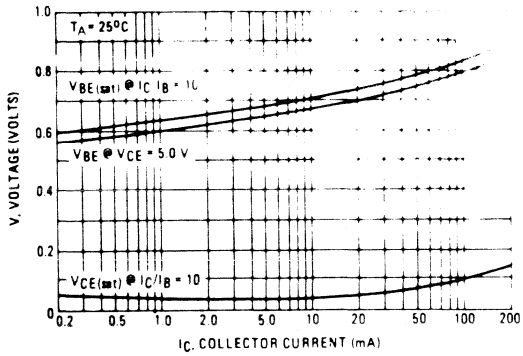


FIGURE 9 – COLLECTOR SATURATION REGION

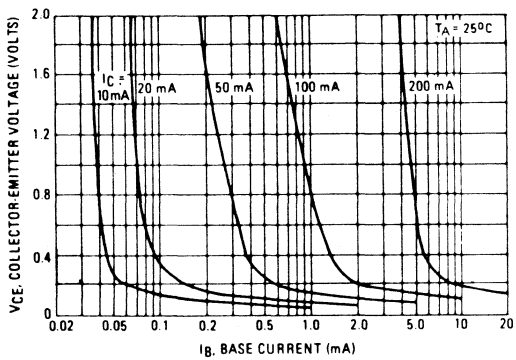


FIGURE 10 – BASE EMITTER TEMPERATURE COEFFICIENT

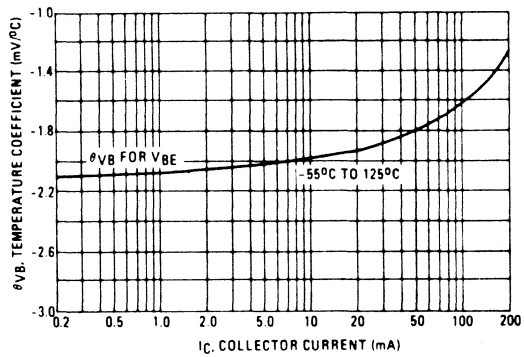


FIGURE 11 – CAPACITANCE

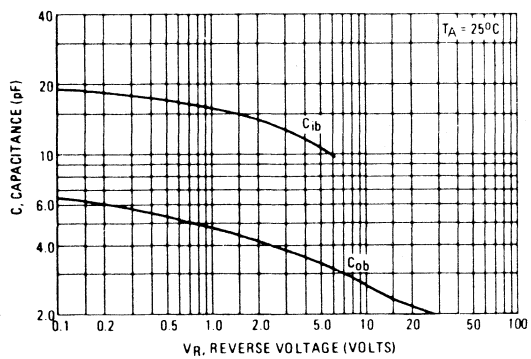
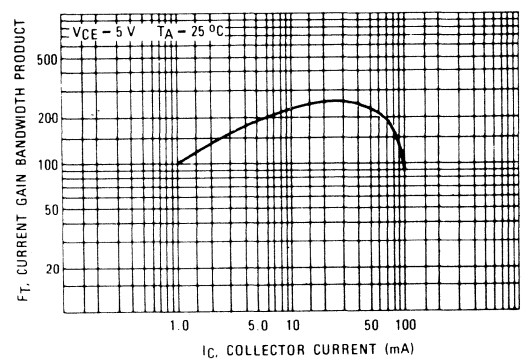


FIGURE 12 – CURRENT GAIN–BANDWIDTH PRODUCT



4

DYNAMIC CHARACTERISTICS, SMALL SIGNAL CHARACTERISTICS

Characteristics	Type	Symbol	Min	Typ	Max	Unit
Current-Gain-Bandwidth Product (I_C = 10 mAdc, V_{CE} = 5 Vdc, f = 100 MHz)	BC 546 BC 547 BC 548	f_T	 150 150 150	 300 300 300		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_C = 0, f = 1 MHz)		C_{ob}		1.7	4.5	pF
Input capacitance (V_{BE} = 0.5 V, I_C = 0, f = 1 MHz)		C_{ib}		10		pF
Input Impedance (I_C = 2 mAdc, V_{CE} = 5 Vdc, f = 1 KHz)	BC 546A/547A/548A BC 546B/547B/548B BC 548C	h_{ie}(h11e)	1.6 3.2 6.0	2.7 4.5 8.7	4.5 8.5 15.0	K ohm
Voltage Feedback Ratio (I_C = 2 mAdc, V_{CE} = 5 Vdc, f = 1 KHz)	BC 546A/547A/548A BC 546B/547B/548B BC 548C	h_{re}(h12e)		1.5 2.0 3.0		$X10^{-4}$
Small-Signal Current Gain (I_C = 2 mAdc, V_{CE} = 5 Vdc, f = 1 KHz)	BC 546A/547A/548A BC 546B/547B/548B BC 548C	h_{fe}(h21e)	125 240 450	220 330 600	260 500 900	
Output Admittance (I_C = 2 mAdc, V_{CE} = 5 Vdc, f = 1 KHz)	BC 546A/547A/548A BC 546B/547B/548B BC 548C	h_{oe}(h22e)		8 10 12	25 35 50	μ mhos
Noise Figure (I_C = 0.2 mAdc, V_{CE} = 5 Vdc, R_S = 2 Kohms, f = 1 KHz, Δf = 200 Hz)	BC 546 BC 547 BC 548	NF		2 2 2	10 10 10	dB

FIGURE 13 – THERMAL RESPONSE

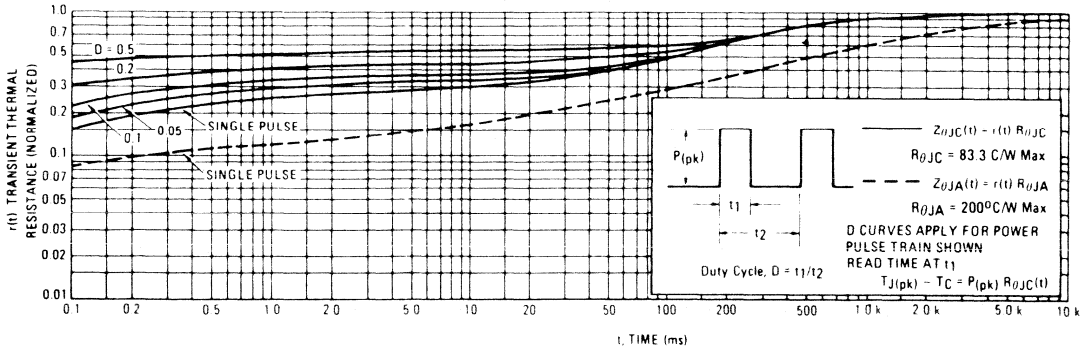
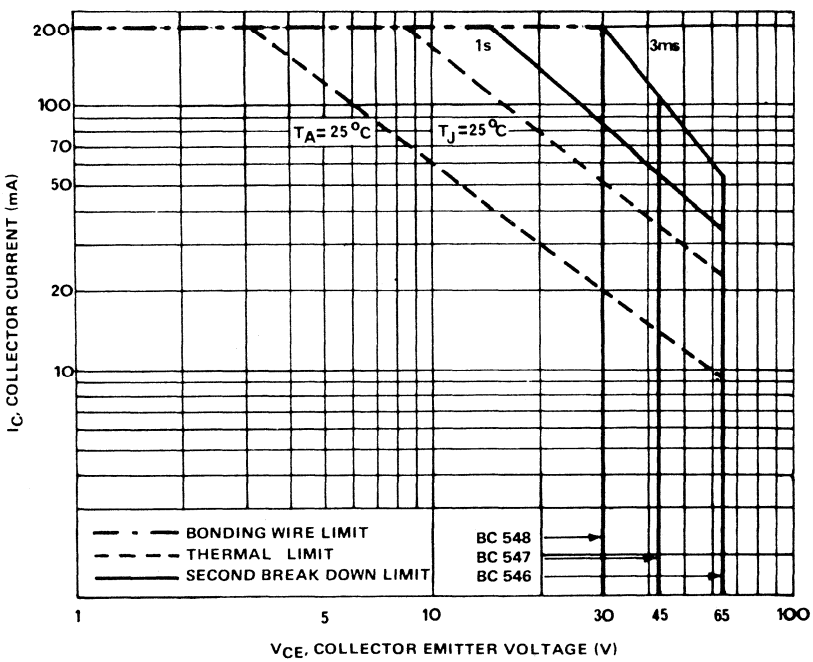


FIGURE 14 – ACTIVE REGION SAFE OPERATING AREA



The safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 14 is based upon $T_{J(pk)}$=150°C; T_C or T_A is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data of Figure 13. At high case or ambient temperatures thermal limitations will reduce the power that can be handled to values less than the limitations imposed by the secondary breakdown. (see AN 415).

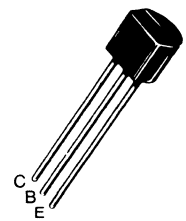
4

BC549
BC550

NPN SILICON ANNULAR♦ LOW NOISE, HIGH GAIN AMPLIFIER TRANSISTOR

- Low Wideband Noise Figure
  N_F = 2.5 dB max (30 Hz-15 KHz)
- Low Noise At Low Frequency
  V_T = 12 nV/√ Hz max (120 Hz)
- High Gain in 2 Ranges
  B range: 180 – 460
  C range: 380 – 800
  (2 mA/5 V)
- Full Applications Information

NPN SILICON LOW NOISE TRANSISTOR



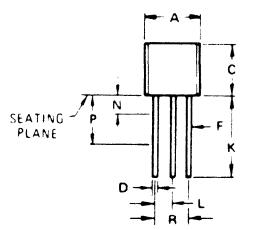
MAXIMUM RATINGS

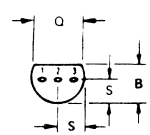
Rating	Symbol	Value BC549	Value BC550	Unit
Collector-Emitter Voltage	V_{CEO}	30	45	Vdc
Collector-Base Voltage	V_{CBO}	45	50	Vdc
Emitter-Base Voltage	V_{EBO}	5		Vdc
Collector Current Continuous Peak	I_C	0.1 0.2		Adc Adc
Base-Current-Continuous	I_B	0.05		Adc
Total Device Dissipation at T_A = 25 °C Derate above 25 °C	P_D	625 5		mW mW/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	200	°C/W

♦Annular Semiconductors Patented by Motorola Inc.





STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	
L	1.150	1.390	0.045	0.055
N	–	1.270		0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

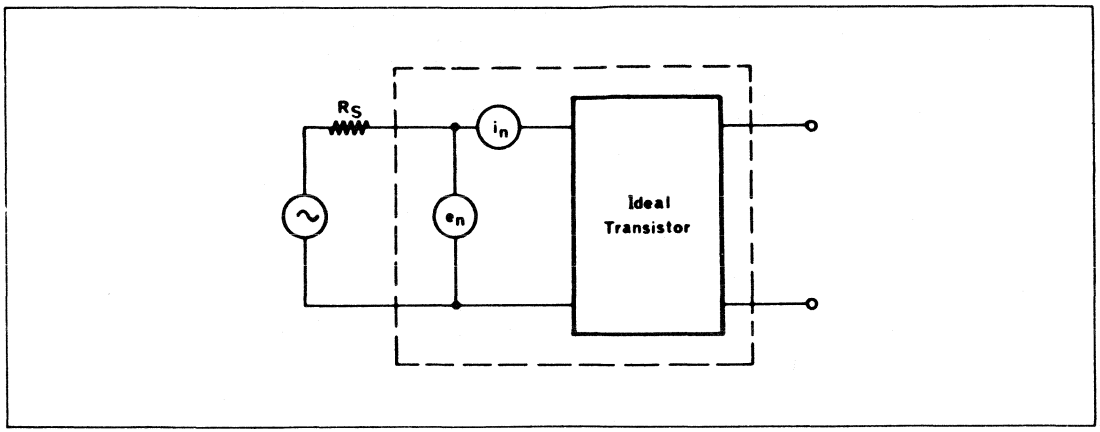
ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0) BC549	BV_{CEO}	30			Vdc
BC550		45			
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0) BC549	BV_{CBO}	45			Vdc
BC550		50			
Emitter-Base Breakdown Voltage (I_C = 10 μAdc, I_C = 0)	BV_{EBO}	5			Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}			15	nAdc
(V_{CB} = 30 Vdc, I_E = 0, T_A = + 125 °C)				5	μAdc
Emitter Cutoff Current (V_{EB} = 4 Vdc, I_C = 0)	I_{EBO}			15	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 10 μAdc, V_{CE} = 5 Vdc) BC549B/550B	h_{FE}	100	150		
BC549C/550C		100	270		
(I_C = 2 mAdc, V_{CE} = 5 Vdc) BC549B/550B		180	290	460	
BC549C/550C		380	500	800	
Collector-Emitter Saturation Voltage	$V_{CE(S)}$				Vdc
(I_C = 10 mAdc, I_B = 0.5 mAdc)			0.075	0.25	
(I_C = 10 mAdc, I_B = see note 1)			0.3	0.6	
(I_C = 100 mAdc, I_B = 5 mAdc, see note 2)			0.25	0.6	
Base-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 5 mAdc)	VBE(S)		1.1		Vdc
Base-Emitter On Voltage	$V_{BE(ON)}$				Vdc
(I_C = 10 μAdc, V_{CE} = 5 Vdc)			0.52		
(I_C = 100 μAdc, V_{CE} = 5 Vdc)			0.55		
(I_C = 2 mAdc, V_{CE} = 5 Vdc)		0.55	0.62	0.75	

Note 1: I_B is value for which I_C = 11 mA at V_{CE} = 1 V
Note 2: Pulse test = 300 μs; Duty Cycle = 2 %

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Current-Gain Bandwidth Product (I_C = 10 mAdc, V_{CE} = 5 Vdc, f = 100 MHz)	f_T		250		MHz
Collector-Base Capacitance (V_{CE} = 10 Vdc, I_E = 0, f = 1 MHz)	C_{cbo}		2.5		pF
h-PARAMETERS (I_C = 2 mAdc, V_{CE} = 5 Vdc, f = 1 KHz)					
Input Impedance BC549B/BC550B BC549C/BC550C	h_{ie}, (h_{11e})	 3.2 6.0	 6.0 8.7	 8.5 15.0	KΩ
Voltage Feedback Ratio BC549B/BC550B BC549C/BC560C	h_{re} (h_{12e})		 2.0 3.0		10^{-4}
Small Signal Current Gain BC549B/BC550B BC549C/BC550C	h_{fe} (h_{21e})	 240 450	 330 600	 500 900	
Output Admittance BC549B/BC550B BC549C/BC550C	h_{oe} (h_{22e})		 10 12	 60 110	μmhos
NOISE PERFORMANCE					
Noise Figure (I_C = 200 μAdc, V_{CE} = 5 Vdc, R_S = 2 KΩ, f = 30 Hz – 15 KHz)	N_F		0.6	2.5	dB
Equivalent Input Noise Voltage (I_C = 200 μAdc, V_{CE} = 5 V, R_S = 2 KΩ, f = 120 Hz) See Application note, Section I	V_T		8.0	12	$nV/\sqrt{Hz}$
Equivalent Input Noise Voltage (I_C = 200 μAdc, V_{CE} = 5 V, R_S = 2KΩ, f = 10 Hz – 50 Hz) See Application note, Section II	V_T		74	135	$nV/\sqrt{Hz}$

FIGURE 1 – TRANSISTOR NOISE MODEL



NOISE APPLICATION NOTE

I. NOISE FIGURE RELATED TO V_T, e_n, and i_n

For a transistor, total noise at the input may be expressed as:

$$V_T = \left[e_n^2 + 4\,KT\,R_S + i_n^2\,R_S^2\right]^{1/2} \qquad (1)$$

Where:

V_T = total noise voltage at the transistor input (Volts/$\sqrt{Hz}$)
e_n = noise voltage of the transistor referred to the input (figures 2 & 3)
i_n = noise current of the transistor referred to the input (figure 4)
K = Boltzmann's constant (1.38×10^{-23} j/°K)
T = Temperature of the source resistance (°K)
R_S = Source resistance (Ohms)

Example:
Find the total noise at the input of a BC550 for a collector current of 1mA and a source impedance of 1KΩ at a frequency of 120 Hz and a temperature of 25 °C.

1. V_T is calculated from e_n, i_n

Read e_n 4.5 nV/$\sqrt{Hz}$ from figure 3 (Note that this is for a one cycle bandwidth)
Read i_n 5.8 pA/$\sqrt{Hz}$ from figure 4

$$V_T = [(3.5 \times 10^{-9})^2 + (4).(1.38 \times 10^{-23}).(300).(1 \times 10^3) + (5.8 \times 10^{-12})^2.(1 \times 10^3)^2]^{1/2}$$

Thus: $\boxed{V_T = 8.2\ nV}$

This checks with the value of 8 nV shown in figure 6.

2. Noise figure is calculated from V_T

Noise figure is defined as:

$$NF = 20 \log_{10} \frac{\text{total noise voltage}}{\text{noise voltage contributed by source resistance}}$$

or

$$NF = 20 \log_{10} \left[\frac{V_T^2}{4\,KT\,R_S}\right]^{1/2}$$

Noise figure can be calculated for the above example as follows:

$$NF = 20 \log_{10} \left[\frac{(8 \times 10^{-9})2}{16.6 \times 10^{-18}}\right]^{1/2}$$

Thus: $\boxed{NF = 5.9\ dB}$

This checks with the values of 6 dB read from figure 7.

To minimize noise in a transistor stage, one might use figure is minimum. This is not necessarily true as shown by figure 6 where the total noise voltage is a minimum at small values of source impedance.
This can be seen from equation (1) which shows that total noise is a direct function of source resistance.

4

II. NOISE VARIATION WITH FREQUENCY

Noise over a frequency band can be handled in one of two ways depending upon whether total transistor noise is constant or variable over the bandwidth of interest:

1. For constant transistor noise, multiply, V_T by the square root of bandwidth. i.e., $V_T = V_T . f.^{1/2}$
2. For variable transistor noise integrate the spectral density V_T (where $\triangle f$ = 1 Hz), over the bandwidth of interest.

Example: Low Frequency Noise

Find the total noise at the input in the bandwidth f_1 = 10 Hz, f_2 = 50 Hz at I_C = 200 μA and R_S = 2 KΩ

This example corresponds to the popular "FLICKER NOISE" test shown on many data sheets.

$$V_T^2 = \int_{-\infty}^{+\infty} V_T(f) \times [G(f)^2 \, df$$

$(f_1 - f_2)$

where:

$$V_{T(f)}^2 = e_{n(f)}^2 + 4 \, KT \, R_S + i_{n(f)}^2 \, R_S^2$$

$e_{n(f)}$ and 4 KT R_S are constant in the bandwidth

$$i_{n(f)} = \frac{i_n^2 \, (1 \, Hz)}{f} \quad \text{(1/f noise spectrum density)}$$

G(f) bandpass filter

= 1 for $f \in (f_1, f_2)$

= 0 for $f \notin (f_1, f_2)$

after integration:

$$V_{T(f_1-f_2)}^2 = (e_{n(f1)}^2 + 4 \, KT \, R_S) \times (f_2 - f_1) + R_S^2 \, i_{n(f1)}^2 \times f1 \times i_{n(f1)} \frac{f2}{f1}$$

Now:

e_n = 5 nV/$\sqrt{Hz}$ at 10 Hz (from figure 2)

i_n = 7 pA/$\sqrt{Hz}$ at 10 Hz (from figure 4)

$$V_T^2 \, (10 \, Hz - 50 \, Hz) = [(25 + 33.1) \, 40 + 196 \times 10 \times 1.6] . 10^{-18}$$

Thus: $\boxed{V_T(10 \, Hz - 50 \, Hz) = 74 \, nV}$

FIGURE 2 – NOISE VOLTAGE vs FREQUENCY

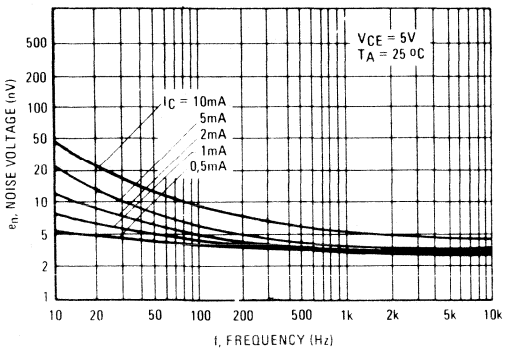


FIGURE 3 – NOISE VOLTAGE vs COLLECTOR CURRENT

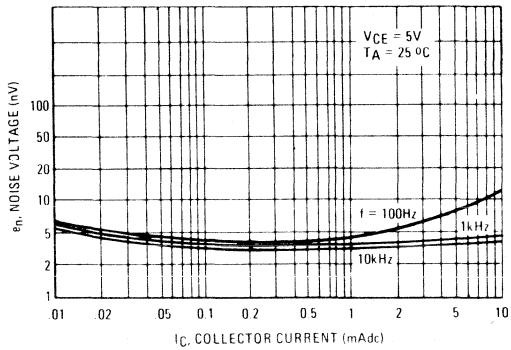


FIGURE 4 – NOISE CURRENT

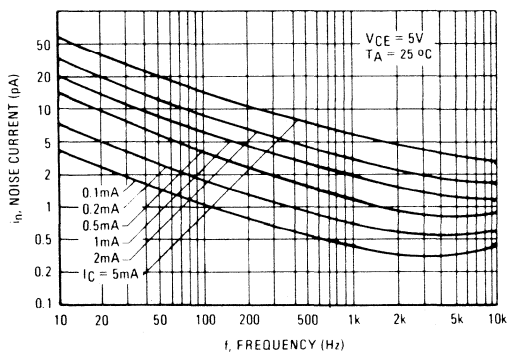


FIGURE 5 – WIDEBAND NOISE FIGURE

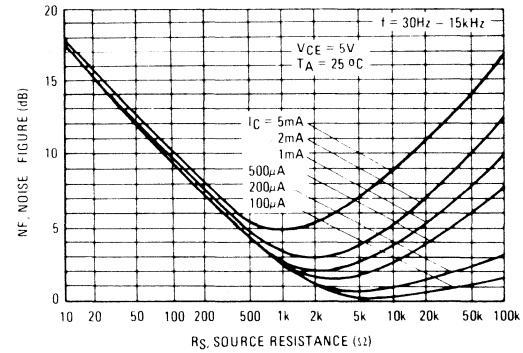


FIGURE 6 – TOTAL NOISE VOLTAGE (120 Hz)

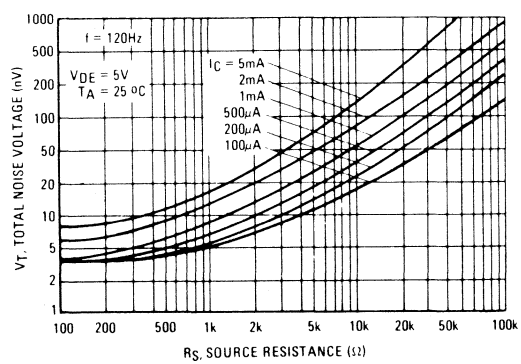


FIGURE 7 – NOISE FIGURE (120 Hz)

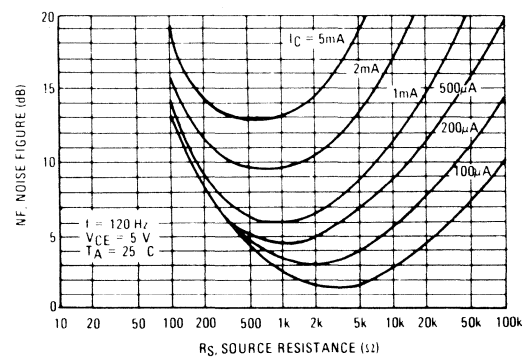


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FIGURE 8 – NORMALIZED DC CURRENT GAIN

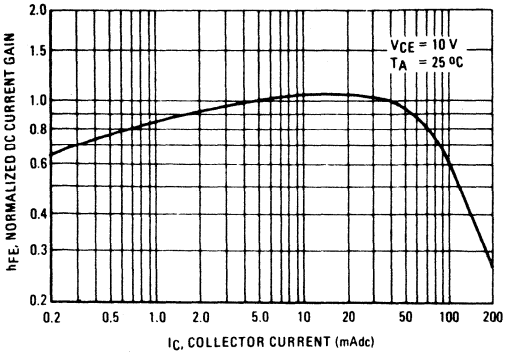


FIGURE 9 – "SATURATION" AND "ON" VOLTAGES

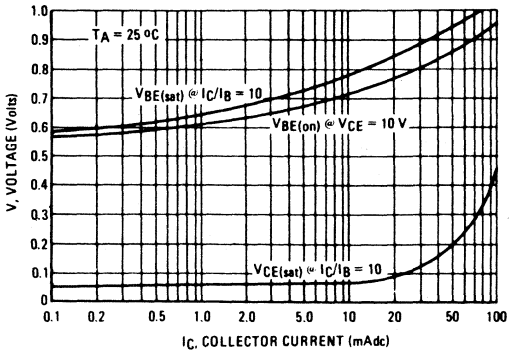


FIGURE 10 – CURRENT GAIN-BANDWIDTH PRODUCT

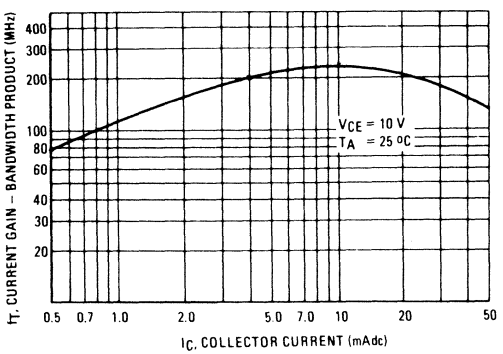


FIGURE 11 – CAPACITANCE

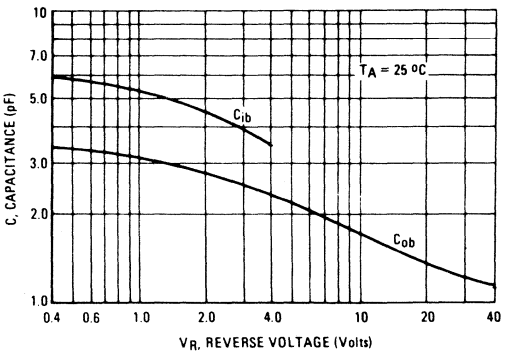


FIGURE 12 – OUTPUT ADMITTANCE

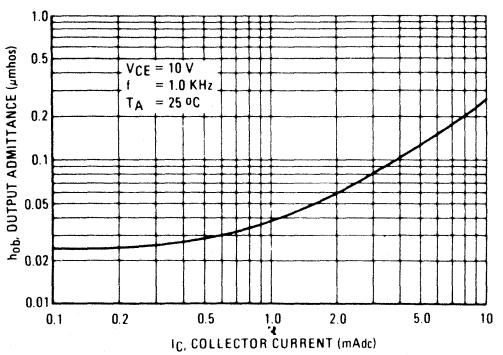
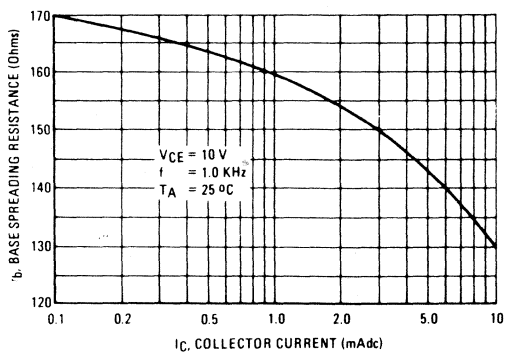


FIGURE 13 – BASE SPREADING RESISTANCE



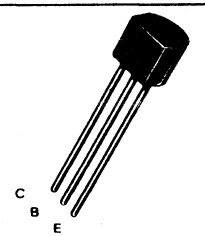
BC556
BC557 • BC558

PNP SILICON ANNULAR* TRANSISTORS

. . . designed for general purpose use in audio, radio, and television applications.

- High Breakdown Voltage—
  BV_{CEO} = 65 Vdc (Min) @ I_C = 1.0 mAdc
- Low Collector-Emitter Saturation Voltage—
  $V_{CE\ (sat)}$ = 0.25 Vdc (Typ) @ I_C = 100 mAdc
- Low output capacitance
  C_{ob} = 6.0 pF (Max) @ V_{CB} = 10 Vdc
- Complementary to NPN BC546/547/548
- One-Piece, Injection-Molded Unibloc† Package

PNP SILICON AMPLIFIER TRANSISTORS



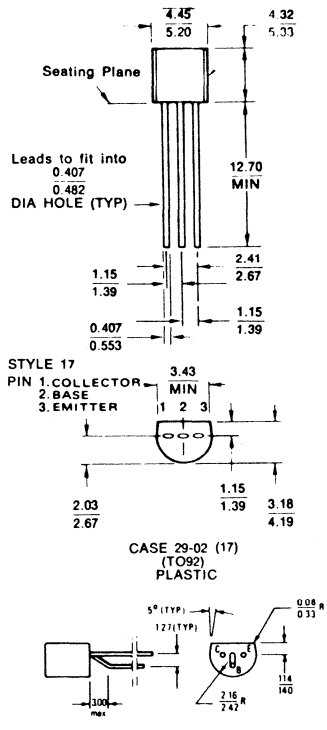
For standard package order BC556/557/558
For TO-18 configuration order BC556-18/557-18/558-18
For TO-5 configuration order BC556-5/557-5/558-5

MAXIMUM RATINGS

Rating	Symbol	BC556	BC557	BC558	Unit
Collector-Emitter Voltage	V_{CEO}	65	45	30	Vdc
Collector-Base Voltage	V_{CB}	80	50	30	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector-Current-Continuous Peak	I_C I_{CM}	100 200			mAdc
Base-Current peak	I_{BM}	200			mAdc
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	625 5			mW mW/°C
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	1.5 12			W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal resistance, Junction to case	Θ_{JC}	0.083	°C/mW
Thermal resistance, Junction to Ambient	Θ_{JA}	0.20	°C/mW



* Annular Semiconductors Patented by Motorola Inc.
† Trademark of Motorola Inc.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Type	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 2.0 mAdc, I_B = 0)	BC 556	BV_{CEO}	65	–	–	Vdc
	BC 557		45	–	–	
	BC 558		30	–	–	
Emitter-Base Breakdown Voltage (I_E = 100μAdc, I_C = 0)	BC 556	BV_{EBO}	5	–	–	Vdc
	BC 557		5	–	–	
	BC 558		5	–	–	
Collector-Emitter Leakage Current		I_{CES}				
V_{CES} = 40 V	BC 556		–	2	100	nA
V_{CES} = 20 V	BC 557		–	2	100	
	BC 558		–	2	100	
V_{CES} = 20 V, T_A = 125 °C	BC 556		–	–	4	μA
	BC 557		–	–	4	
	BC 558		–	–	4	
DC Current Gain		h_{FE}				
(I_C = 10 μ Adc, V_{CE} = 5 Vdc)	BC 556A/557A/558A		–	90	–	
	BC 556B/557B/558B		–	150	–	
	BC 557C/558C		–	270	–	
(I_C = 2 mAdc, V_{CE} = 5 Vdc)	BC 556		120	–	450	
	BC 557		120	–	450	
	BC 558		120	–	800	
	BC 556A/557A/558A		120	170	220	
	BC 556B/557B/558B		180	290	460	
	BC 557C/558C		380	500	800	
(I_C = 100 mAdc, V_{CE} = 5 Vdc)	BC 556A/557A/558A		–	120	–	
	BC 556B/557B/558B		–	180	–	
	BC557C/558C		–	300	–	
Collector-Emitter Saturation Voltage		V_{CE} (sat)				Vdc
(I_C = 10 mAdc, I_B = 0,5 mAdc)			–	0.075	0.3	
(I_C = 10 mAdc, I_B = see Note 1)			–	0.30	0.60	
(I_C = 100 mAdc, I_B = 5 mAdc)			–	0.25	0.65	
Base-Emitter Saturation Voltage		V_{BE} (sat)				Vdc
(I_C = 10 mAdc, I_B = 0.5 mAdc)			–	0.70	–	
(I_C = 100 mAdc, I_B = 5 mAdc)			–	1.00	–	
Base-Emitter on Voltage		V_{BE} (on)				Vdc
(I_C = 2 mAdc, V_{CE} = 5 Vdc)			0.55	0.62	0.70	
I_C = 10 mA, V_{CE} = 5 Vdc				0.7	0.82	

Note 1 : I_C = 10 mAdc on the constant base current characteristic, which yields the point I_C = 11 mAdc, V_{CE} = 1 V

FIGURE 1 – NORMALIZED DC CURRENT GAIN

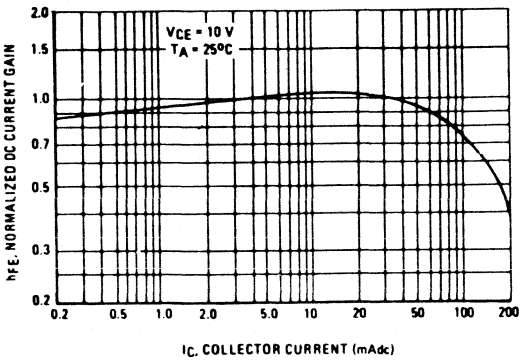

FIGURE 2 – "SATURATION" AND "ON" VOLTAGES

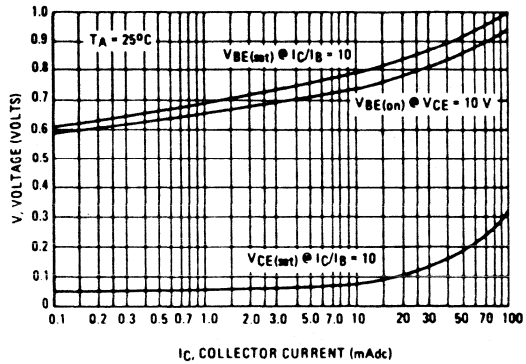

FIGURE 3 – COLLECTOR SATURATION REGION

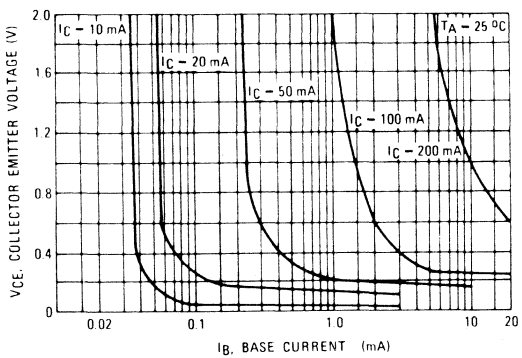

FIGURE 4 – BASE EMITTER TEMPERATURE COEFFICIENT

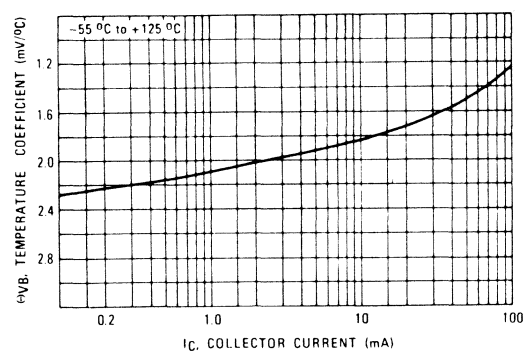

FIGURE 5 – CAPACITANCES

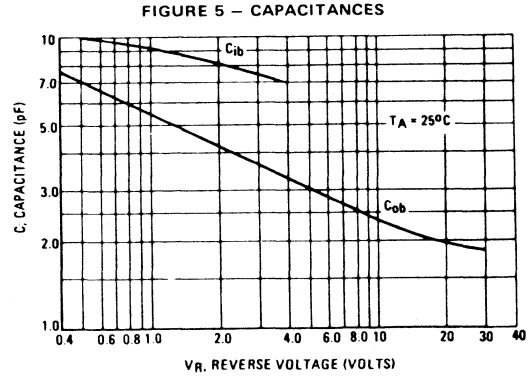

FIGURE 6 – CURRENT GAIN–BANDWIDTH PRODUCT

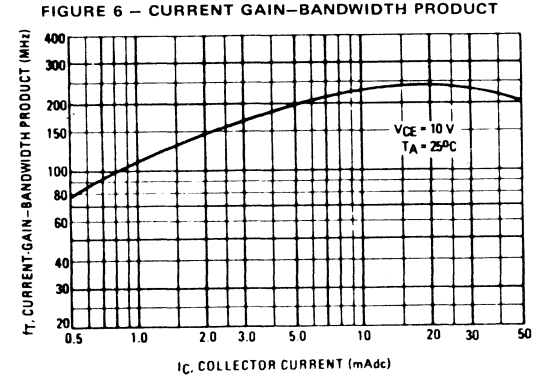

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FIGURE 7 – DC CURRENT GAIN

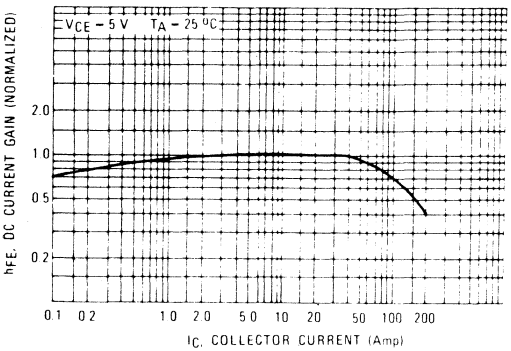


FIGURE 8 – "ON" VOLTAGE

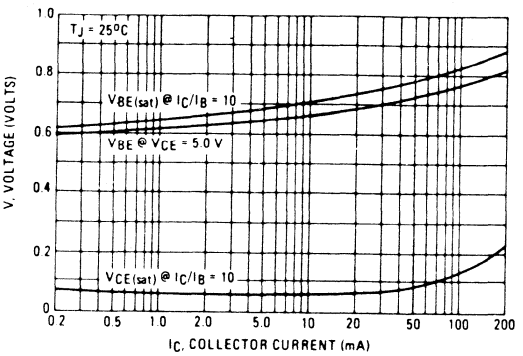


FIGURE 9 – COLLECTOR SATURATION REGION

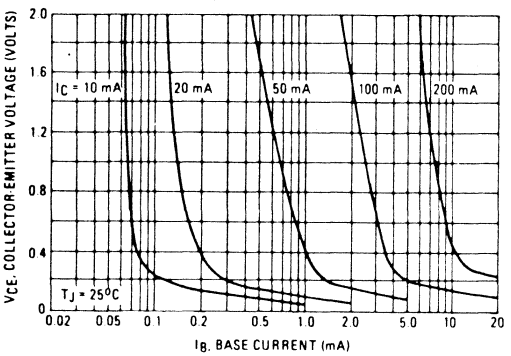


FIGURE 10 – BASE EMITTER TEMPERATURE COEFFICIENT

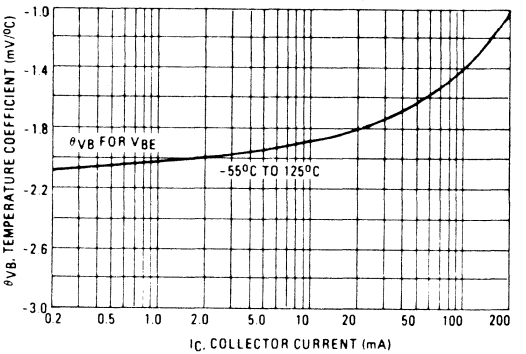


FIGURE 11 – CAPACITANCE

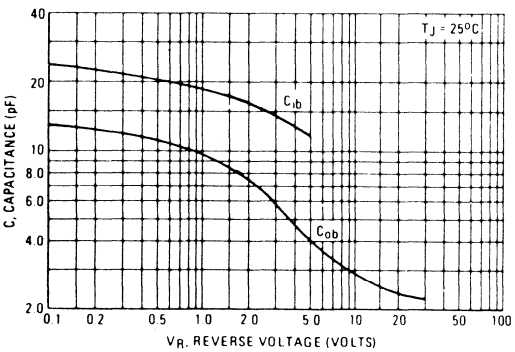
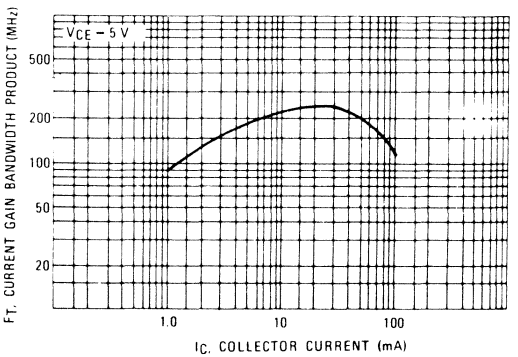


FIGURE 12 – CURRENT GAIN–BANDWIDTH PRODUCT



DYNAMIC CHARACTERISTICS / SMALL SIGNAL CHARACTERISTICS

Characteristic	Type	Symbol	Min	Typ	Max	Unit
Current-Gain – Bandwidth Product (I_C= 10 mAdc, V_{CE}= 5 Vdc, f = 50 MHz)		f_T				MHz
	BC 556		–	280	–	
	BC 557		–	320	–	
	BC 558		–	360	–	
Output Capacitance (V_{CB}= 10 Vdc, I_C= 0, f = 1 MHz)		C_{ob}	–	3	6.0	pF
Noise Figure (I_C= 0,2 mAdc, V_{CE}= 5 Vdc, R_S= 2 Kohms, f = 1 KHz, f = 200 Hz)		NF				dB
	BC 556		–	2	10	
	BC 557		–	2	10	
	BC 558		–	2	10	
Input Impedance (I_C= 2 mAdc, V_{CE}= 5 Vdc, f = 1 KHz)		$h_{ie}(h_{11e})$				kΩ
	BC 556A/557A/558A		1.2	2.7	4.5	
	BC 556B/557B/558B		3.0	4.5	8.0	
	BC 557C/558C		5.0	8.0	14.0	
Voltage Feedback Ratio (I_C= 2 mAdc, V_{CE}= 5 Vdc, f = 1 KHz)		$h_{re}(h_{12e})$				10^{-4}
	BC 556A/557A/558A		–	3.0	–	
	BC 556B/557B/558B		–	3.5	–	
	BC 557C/558C		–	4.0	–	
Small Signal Current Gain (I_C= 2 mAdc, V_{CE}= 5 Vdc f = 1 KHz)		$h_{fe}(h_{21e})$				–
	BC 556A/557A/558A		125	220	260	
	BC 556B/557B/558B		240	330	500	
	BC 557C/558C		450	600	900	
Output Admittance (I_C= 2 mAdc, V_{CE}= 5 Vdc, f= 1 KHz)		$h_{oe}(h_{22e})$				μmhos
	BC 556A/557A/558A		–	25	50	
	BC 556B/557B/558B		–	30	70	
	BC 557C/558C		–	60	110	

4

FIGURE 13 – THERMAL RESPONSE

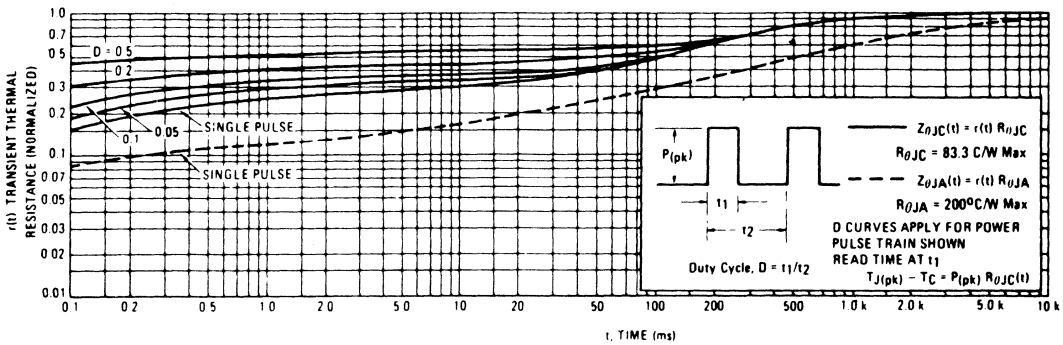
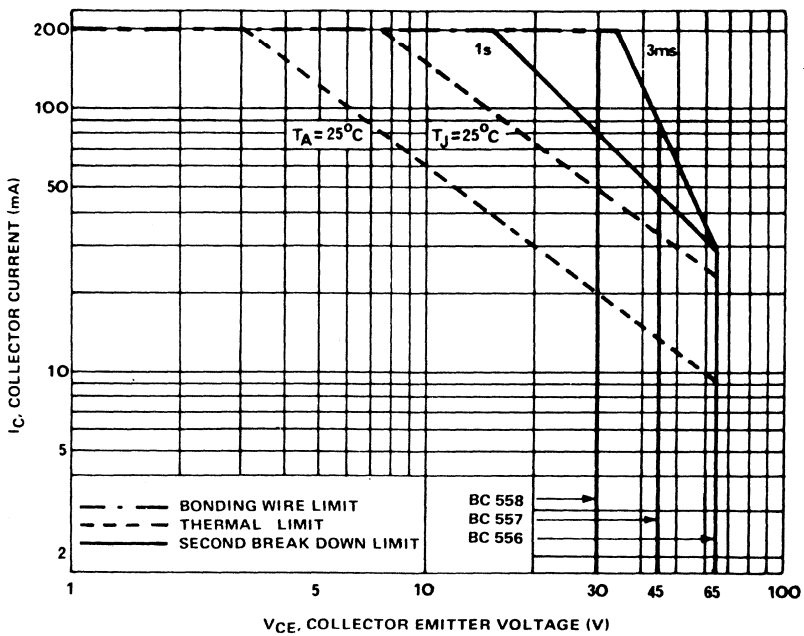


FIGURE 14 – ACTIVE REGION SAFE OPERATING AREA



The safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

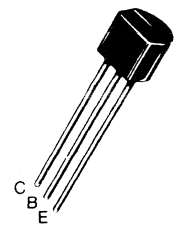
The data of Figure 14 is based upon $T_{J(pk)}$=150°C; T_C or T_A is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150°C$. $T_{J(pk)}$ may be calculated from the data of Figure 13. At high case or ambient temperatures thermal limitations will reduce the power that can be handled to values less than the limitations imposed by the secondary breakdown. (see AN 415).

BC559
BC560

PNP SILICON ANNULAR♦ LOW NOISE, HIGH GAIN AMPLIFIER TRANSISTOR

- Low Wideband Noise Figure
  N_F = 2.5 dB max (30 Hz-15 KHz)
- Low Noise At Low Frequency
  V_T = 10 nV/√ Hz max (120 Hz)
- High Gain in 2 Ranges
  B range: 180 – 460
  C range: 380 – 800
  } (2 mA/5 V)
- Full Applications Information

PNP SILICON LOW NOISE TRANSISTOR



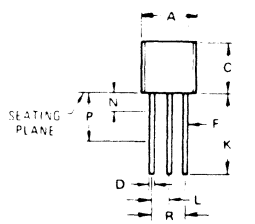
MAXIMUM RATINGS

Rating	Symbol	Value BC559	Value BC560	Unit
Collector-Emitter Voltage	V_{CEO}	35	45	Vdc
Collector-Base Voltage	V_{CBO}	45	50	Vdc
Emitter-Base Voltage	V_{EBO}	5		Vdc
Collector Current Continuous Peak	I_C	0.1 0.2		Adc Adc
Base-Current-Continuous	I_B	0.05		Adc
Total Device Dissipation at T_A = 25 °C Derate above 25 °C	P_D	625 5		mW mW/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150		°C

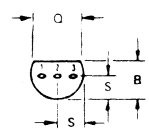
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	200	°C/W

♦Annular Semiconductors Patented by Motorola Inc.



STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

4

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

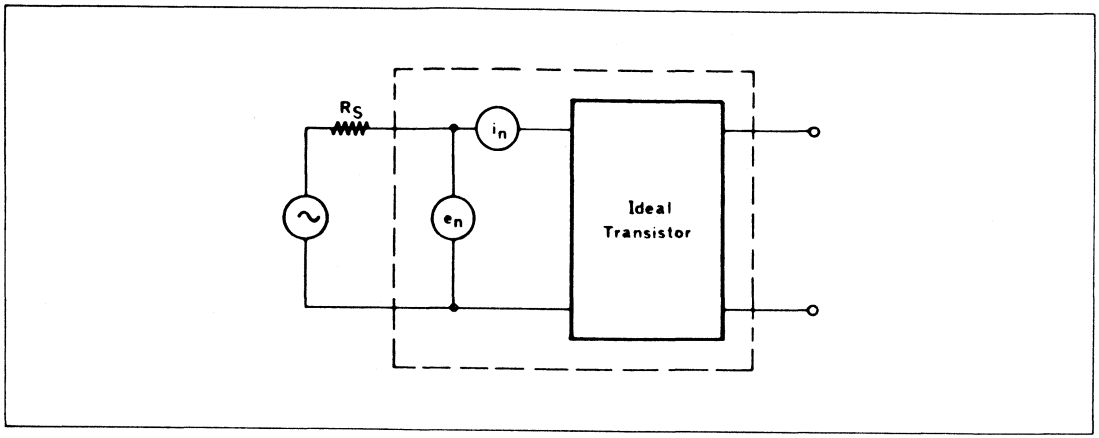
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0) BC559	BV_{CEO}	35			Vdc
BC560		45			
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0) BC559	BV_{CBO}	45			Vdc
BC560		50			
Emitter-Base Breakdown Voltage (I_C = 10 μAdc, I_C = 0)	BV_{EBO}	5			Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}			15	nAdc
(V_{CB} = 30 Vdc, I_E = 0, T_A = +125 °C)				5	μAdc
Emitter Cutoff Current (V_{EB} = 4 Vdc, I_C = 0)	I_{EBO}			15	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 10 μAdc, V_{CE} = 5 Vdc) BC559B/560B	h_{FE}	100	150		
BC559C/560C		100	270		
(I_C = 2 mAdc, V_{CE} = 5 Vdc) BC559B/560B		180	290	460	
BC559C/560C		380	500	800	
Collector-Emitter Saturation Voltage	$V_{CE(S)}$				Vdc
(I_C = 10 mAdc, I_B = 0.5 mAdc)			0.075	0.25	
(I_C = 10 mAdc, I_B = see note 1)			0.3	0.6	
(I_C = 100 mAdc, I_B = 5 mAdc, see note 2)			0.25		
Base-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 5 mAdc)	$V_{BE(S)}$		1.1		Vdc
Base-Emitter On Voltage (I_C = 10 μAdc, V_{CE} = 5 Vdc)	$V_{BE(ON)}$		0.52		Vdc
(I_C = 100 μAdc, V_{CE} = 5 Vdc)			0.55		
(I_C = 2 mAdc, V_{CE} = 5 Vdc)		0.55	0.62	0.75	

Note 1: I_B is value for which I_C = 11 mA at V_{CE} = 1 V
Note 2: Pulse test = 300 μs; Duty Cycle = 2 %.

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Current-Gain Bandwidth Product (I_C = 10 mAdc, V_{CE} = 5 Vdc, f = 100 MHz)	f_T		250		MHz
Collector-Base Capacitance (V_{CE} = 10 Vdc, I_E = 0, f = 1 MHz)	C_{cbo}		2.5		pF
h-PARAMETERS (I_C = 2 mAdc, V_{CE} = 5 Vdc, f = 1 KHz)					
Input Impedance BC559B/BC560B BC559C/BC560C	h_{ie}, (h_{11e})	 3.2 5.0	 6.0 8.0	 8.5 14.0	KΩ
Voltage Feedback Ratio BC559B/BC560B BC559C/BC560C	h_{re} (h_{12e})		 3.5 4.0		10^{-4}
Small Signal Current Gain BC559B/BC560B BC559C/BC560C	h_{fe} (h_{21e})	 240 450	 330 600	 500 900	
Output Admittance BC559B/BC560B BC559C/BC560C	h_{oe} (h_{22e})		 10 12	 60 110	μmhos
NOISE PERFORMANCE					
Noise Figure (I_C = 200 μAdc, V_{CE} = 5 Vdc, R_S = 2 KΩ, f = 30 Hz – 15 KHz)	N_F		0.5	2.0	dB
Equivalent Input Noise Voltage (I_C = 200 μAdc, V_{CE} = 5 V, R_S = 2 KΩ, f = 120 Hz) See Application note, Section I	V_T		8.0	10	$nV/\sqrt{Hz}$
Equivalent Input Noise Voltage (I_C = 200 μAdc, V_{CE} = 5 V, R_S = 2KΩ, f = 10 Hz – 50 Hz) See Application note, Section II	V_T		74	110	$nV/\sqrt{Hz}$

4

FIGURE 1 – TRANSISTOR NOISE MODEL



NOISE APPLICATION NOTE

I. NOISE FIGURE RELATED TO V_T, e_n, and i_n

For a transistor,, total noise at the input may be expressed as:

$$V_T = \left[e_n^2 + 4\,KT\,R_S + i_n^2\,R_S^2\right]^{1/2} \qquad (1)$$

Where:

V_T = total noise voltage at the transistor input (Volts/$\sqrt{Hz}$)

e_n = noise voltage of the transistor referred to the input (figures 2 & 3)

i_n = noise current of the transistor referred to the input (figure 4)

K = Boltzmann's constant (1.38×10^{-23} j/°K)

T = Temperature of the source resistance (°K)

R_S = Source resistance (Ohms)

Example:
Find the total noise at the input of a BC560 for a collector current of 1mA and a source impedance of 1KΩ at a frequency of 120 Hz and a temperature of 25 °C.

1. V_T is calculated from e_n, i_n

Read e_n 4.5 nV/$\sqrt{Hz}$ from figure 3 (Note that this is for a one cycle bandwidth)

Read i_n 5.8 pA/$\sqrt{Hz}$ from figure 4

$$V_T = [(3.5 \times 10^{-9})^2 + (4).(1.38 \times 10^{-23}).(300).(1 \times 10^3) + (5.8 \times 10^{-12})^2.(1 \times 10^3)^2]^{1/2}$$

Thus: $\boxed{V_T = 8.2\ nV}$

This checks with the value of 8 nV shown in figure 6.

2. Noise figure is calculated from V_T

Noise figure is defined as:

$$NF = 20 \log_{10} \frac{\text{total noise voltage}}{\text{noise voltage contributed by source resistance}}$$

or

$$NF = 20 \log_{10} \left[\frac{V_T^2}{4\,KT\,R_S}\right]^{1/2}$$

Noise figure can be calculated for the above example as follows:

$$NF = 20 \log_{10} \left[\frac{(8 \times 10^{-9})2}{16.6 \times 10^{-18}}\right]^{1/2}$$

Thus: $\boxed{NF = 5.9\ dB}$

This checks with the values of 6 dB read from figure 7.

To minimize noise in a transistor stage, one might use figure is minimum. This is not necessarily true as shown by figure 6 where the total noise voltage is a minimum at small values of source impedance.
This can be seen from equation (1) which shows that total noise is a direct function of source resistance.

II. NOISE VARIATION WITH FREQUENCY

Noise over a frequency band can be handled in one of two ways depending upon whether total transistor noise is constant or variable over the bandwidth of interest:

1. For constant transistor noise, multiply, V_T by the square root of bandwidth. i.e., $V_T = V_T . f.^{1/2}$
2. For variable transistor noise integrate the spectral density V_T (where $\triangle f = 1$ Hz), over the bandwidth of interest.

Example: Low Frequency Noise

Find the total noise at the input in the bandwidth $f_1 =$ 10 Hz, $f_2 = 50$ Hz at $i_C = 200\ \mu A$ and $R_S = 2\ K\Omega$
This example corresponds to the popular "FLICKER NOISE" test shown on many data sheets.

$$V_T^2 = \int_{-\infty}^{+\infty} V_T(f) \times [G(f)^2\ df$$

$(f_1 - f_2)$

where:

$$V_{T(f)}^2 = e_{n(f)}^2 + 4\ KT\ R_S + i_{n(f)}^2\ R_S^2$$

$e_{n(f)}$ and $4\ KT\ R_S$ are constant in the bandwidth

$$i_{n(f)} = \frac{i_n^2\ (1\ Hz)}{f} \quad \text{(1/f noise spectrum density)}$$

G(f) bandpass filter

$= 1$ for $f \in (f_1, f_2)$
$= 0$ for $f \notin (f_1, f_2)$

after integration:

$$V_{T(f_1-f_2)}^2 = (e_{n(f1)}^2 + 4\ KT\ R_S) \times (f_2-f_1) + R_S^2\ i_{n(f1)}^2 \times f1 \times i_{n(f1)} \frac{f2}{f1}$$

Now:
$e_n = 5\ nV/\sqrt{Hz}$ at 10 Hz (from figure 2)
$i_n = 7\ pA/\sqrt{Hz}$ at 10 Hz (from figure 4)

$$V_T^2\ (10\ Hz-50\ Hz) = [(25 + 33.1)\ 40 + 196 \times 10 \times 1.6].10^{-18}$$

Thus: $\boxed{V_T(10\ Hz-50\ Hz) = 74\ nV}$

4

FIGURE 2 – NOISE VOLTAGE V_S FREQUENCY

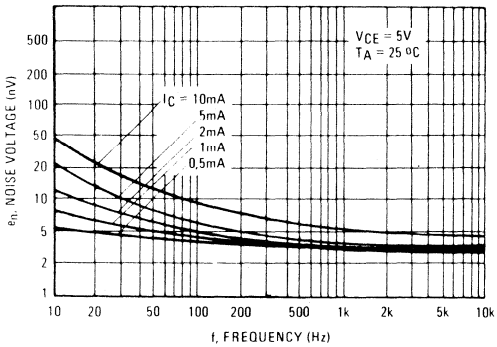


FIGURE 3 – NOISE VOLTAGE V_S COLLECTOR CURRENT

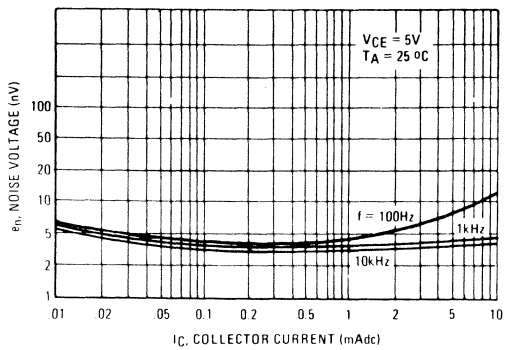


FIGURE 4 – NOISE CURRENT

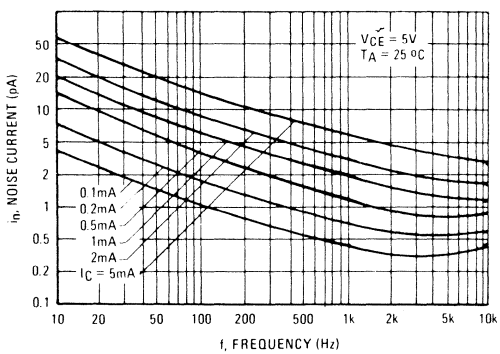


FIGURE 5 – WIDEBAND NOISE FIGURE

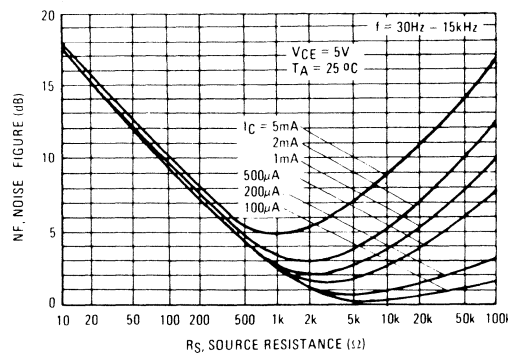


FIGURE 6 – TOTAL NOISE VOLTAGE (120 Hz)

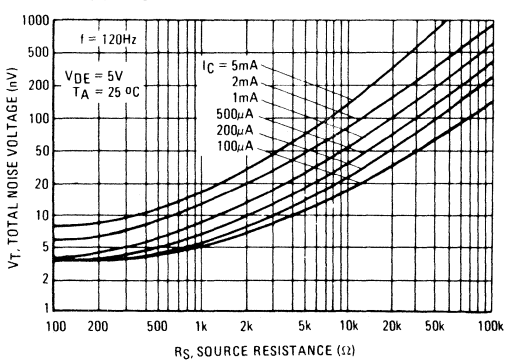


FIGURE 7 – NOISE FIGURE (120 Hz)

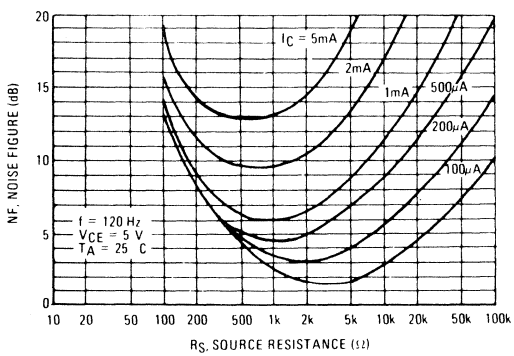


FIGURE 8 – NORMALIZED DC CURRENT GAIN

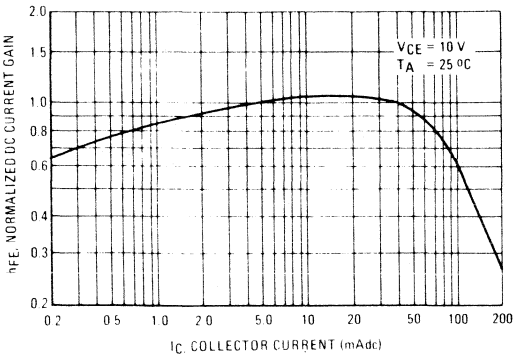


FIGURE 9 – "SATURATION" AND "ON" VOLTAGES

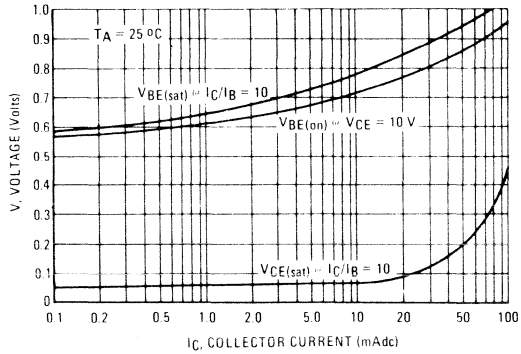


FIGURE 10 – CURRENT GAIN-BANDWIDTH PRODUCT

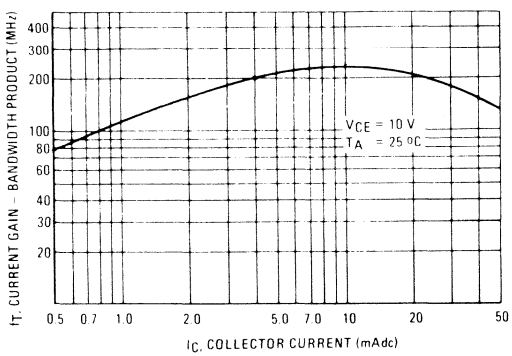


FIGURE 11 – CAPACITANCE

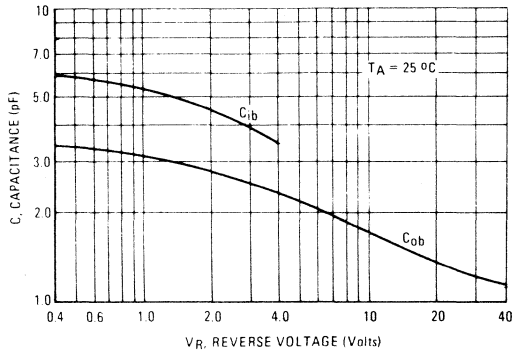


FIGURE 12 – OUTPUT ADMITTANCE

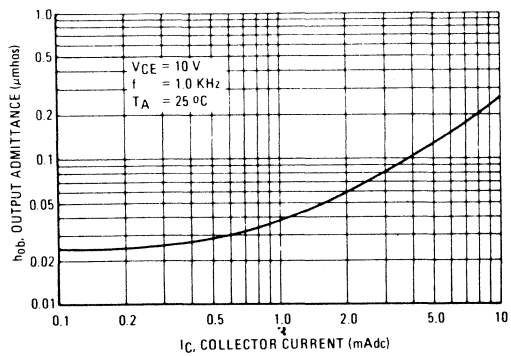
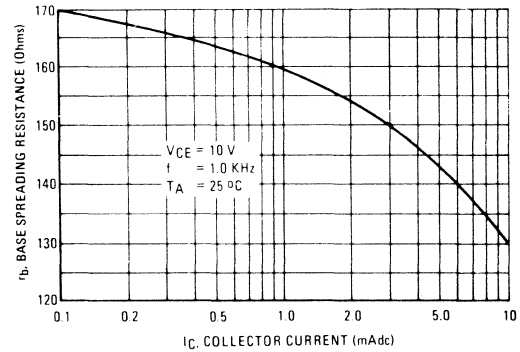


FIGURE 13 – BASE SPREADING RESISTANCE



4

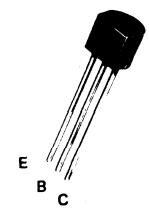
BC650,S
BC651,S

NPN SILICON ANNULAR▲ AMPLIFIER TRANSISTORS

. . . designed for use in low-level, low-noise amplifier applications.

- Very Low Noise Figure:
  NF = 0.5 dB (Typ) – BC650/S – BC651/S
  @ 100 Hz, 10 KΩ, 0.1 mA, 5.0 Volts
- Excellent h_{FE} Linearity from 1.0 μA to 10 mA
- High DC Current Gain:
  h_{FE} @ I_C = 2 mA, V_{CE} = 5 V
  C range: : 380 – 820
  D range: 680 – 1400
- Excellent Reliability with Nitride Chip Passivation and Third Generation Epoxy

NPN SILICON
LOW NOISE
AUDIO AMPLIFIER
TRANSISTORS

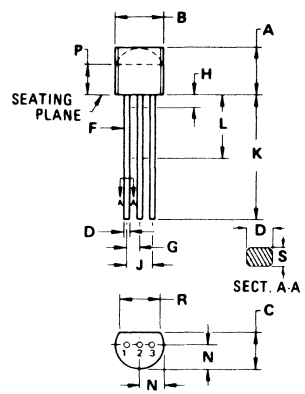


MAXIMUM RATINGS*			
Rating	**Symbol**	**Value**	**Unit**
Collector-Base Voltage BC651 BC650	V_{CB}	45 30	Vdc
Collector-Emitter Voltage BC651 BC650	V_{CEO}	45 30	Vdc
Emitter-Base Voltage	V_{EB}	6.0	Vdc
Collector Current	I_C	200	mAdc
Total Power Dissipation @ T_A = 25 °C Derate above 25 °C	P_D	625 5.0	mW mW/°C
Total Power Dissipation @ T_A = 25 °C Derate above 25 °C	P_D	1.5 12	Watts mW/°C
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	Max.	Unit
Thermal Resistance, Junction to Ambient	$R\theta_{JA}$	200	°C/W
Thermal Resistance, Junction to Case	$R\theta_{JC}$	83.3	°C/W

* Indicates JEDEC Registered Data



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.
CASE 29-02
TO-92

▲ Annular Semiconductors Patented by Motorola.

***ELECTRICAL CHARACTERISTICS** (T_A = 25 °C unless otherwise noted)

Characteristics		Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS					
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)		I_{CBO}	–	0.015	μA
Collector-Emitter Current (V_{CE} = 30 Vdc)		I_{CEO}	–	0.025	μA
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	BC650 BC651	$V_{(BR)CBO}$	30 45	–	Vdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	0.015	μA
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BC650 BC651	$V_{(BR)CEO}$	30 45	–	Vdc
ON CHARACTERISTICS					
DC Current Gain I_C = 2 mAdc, V_{CE} = 5 Vdc	BC650/BC651 BC650C/BC651C BC650D/BC651D	h_{FE}	380 380 680	1400 820 1400	
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 0.5 mAdc) (I_C = 100 mAdc, I_B = 5.0 mAdc)		$V_{CE(sat)}$	– –	0.2 0.6	Vdc
Base Emitter On Voltage (I_C = 2 mAdc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	0.55	0.70	Vdc
DYNAMIC CHARACTERISTICS					
Input Impedance (I_C = 2 mAdc, V_{CE} = 5.0 Vdc, f = **1.0 kHz**)	BC650C/BC651C BC650D/BC651D	h_{ie}	2.0 4.0	20 60	kΩ
Voltage Feedback Ratio (I_C = 2 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	BC650C/BC651C BC650D/BC651D	h_{re}	1.0 2.0	30 60	X10-4
Output Admittance (I_C = 2 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	BC650C/BC651C BC650D/BC651D	h_{oe}	10 20	60 120	μmhos
Small Signal Current Gain (I_C = 2 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	BC650/BC651	h_{fe}	380	1600	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	–	3.0	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)		C_{ib}	–	8.0	pF
Current Gain – Bandwidth Product (I_C = 1.0 mAdc, V_{CE} = 5.0 V, f = 100 MHz)		f_T	100	700	MHz

NOISE FIGURE/TOTAL NOISE VOLTAGE CHARACTERISTICS (V_{CE} = 5.0 V, I_C = 0.2 mA T_A = 25 °C)

	NF Max. (1)	VT Max. (1)	NF Max. (2)	VT Max. (2)	NF Max. (3)	VT Max. (3)	Unit	Unit
BC650, BC651, C, D	8	14.4	2.5	7.6	1	6.4	dB	nV
BC650S, BC651S, CS, DS	4	9.1	1.5	6.8	1	6.4	dB	nV

(1) RS = 2 kΩ, BW = 1.0 Hz, f = 10 Hz
(2) RS = 2 kΩ, BW = 1.0 Hz, f = 120 Hz
(3) RS = 2 kΩ, BW = 1.0 Hz, f = 1 kHz

4

NOISE APPLICATION NOTE

For a transistor, total noise at the input may be expressed as:

$$V_T = \left[e_n^2 + 4KT\,R_S + i_n^2\,R_S^2 \right]^{1/2} \qquad (1)$$

Where:

V_T = total noise voltage at the transistor input (Volts $/\sqrt{Hz}$)

e_n = noise voltage of the transistor referred to the input

i_n = noise current of the transistor referred to the input

K = Boltzman's constant (1.38×10^{-23} j/°K)

T = temperature of the source resistance (°K)

R_S = source resistance (Ohms)

Example:

Find the total noise at the input of a BC650 for a collector current of 100 μA and a source impedance of 50 kilohm at a frequency of 100 Hz and at a temperature of 25 °C.

Read e_n = 2.0 nV $/\sqrt{Hz}$ from Figure 7.

(Note that this is for a one cycle bandwidth)

Read i_n = 0.31 pA $/\sqrt{Hz}$ from Figure 8.

$V_T = [(2.0 \times 10^{-9})^2 + (4)(1.38 \times 10^{-23})(297)(5 \times 10^4) + (0.31 \times 10^{-12})^2 (5 \times 10^4)^2]^{1/2} =$ 32.6 nV $/\sqrt{Hz}$.

Note that for the resistor alone ($e_n = i_n = 0$), V_T is 28.6 nV $/\sqrt{Hz}$.

Noise figure is defined as:

$$NF = 20 \log_{10} \frac{\text{total noise voltage}}{\text{noise voltage contributed by the Source Resistance}}$$

or

$$NF = 20 \log_{10} \left[\frac{V_T^2}{4\,KT\,R_S} \right]^{1/2} \qquad (2)$$

Noise figure can be calculated for the above example as follows:

$$NF = 20 \log_{10} \left[\frac{(32.6 \times 10^{-9})^2}{8.2 \times 10^{-16}} \right]^{1/2} = 1.1\text{dB}$$

To minimize noise in a transistor stage, one might assume that noise is minimized when Noise Figure is minimum. This is not necessarily true since the total noise voltage is a minimum at small values of source impedance. This can be seen from equation (1) which shows that total noise is a direct function of source resistance.

Noise over a frequency band can be handled in one of two ways depending upon whether total transistor noise is constant or variable over the bandwidth of interest:

1. For Constant transistor noise, multiply, V_T by the square root of bandwidth. i.e., $V'_T = V_T \cdot \Delta f^{1/2}$.
2. For variable transistor noise, plot V_T (where Δf = 1.0 Hz) versus frequency over the bandwidth and integrate the result.

Total noise voltage at the output of the transistor stage can be found by multiplying V_T or V'_T by the voltage gain of the stage.

COMPUTER MODEL

In their book "Low-Noise Electronic Design," published by Wiley & Sons, (copyright 1973), the authors, C.D. Motchenbacher and F.C. Fitchen have presented a computer program for Noise Figure circuit analysis. The computer constants for both models of the BC650/S, BC651/S transistor are presented below for your convenience.

"NOSMOD" Model

Computer Symbol	Value
E	Read e_n from figure 7 at 10 kHz for desired current
I	Read i_n from figure 8 at 10 kHz for desired current
F1	1.0 Hz
F2	100,000 kHz
F3	100 Hz
F4	100,000 kHz

"XISTOR" Model

Computer Symbol	Value
N5	100 Ω
N6	70 Ω
14	Collector Current of application
17	5×10^{-10} Amps
F7	110000
F8	Read f_T from figure 16 for desired current
Q1	1.37
Q2	1.25
B	actual measured h_{FE}

TYPICAL NOISE CHARACTERISTICS

(V_{CE} = 5.0 V, T_A = 25°C)

CONTOURS OF CONSTANT NOISE FIGURE

NARROW BAND

FIGURE 1 – 10 Hz

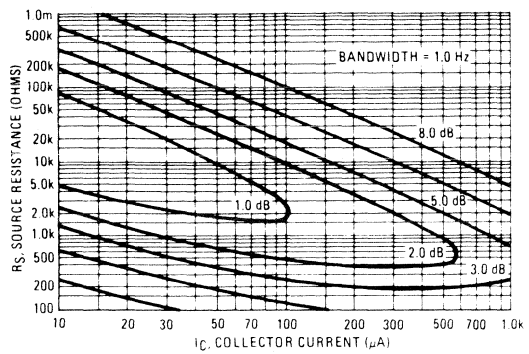
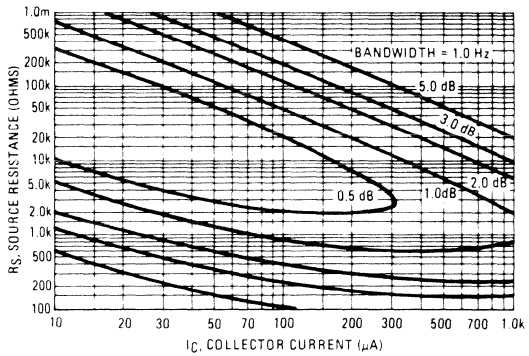


FIGURE 2 – 100 Hz



NARROW BAND

FIGURE 3 – 1.0 kHz

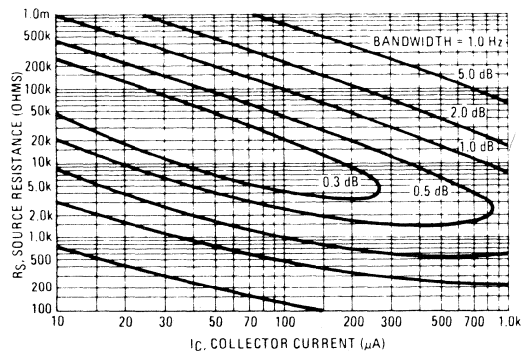
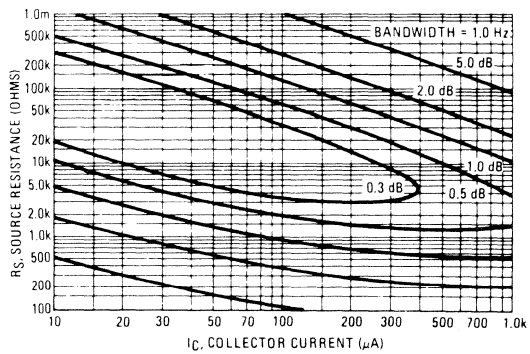


FIGURE 4 – 10 kHz



BROAD BAND

FIGURE 5 – 10 Hz – 10 kHz

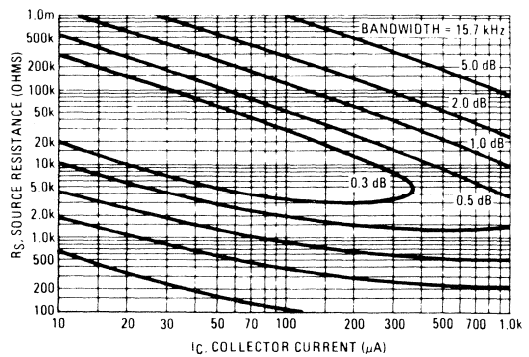
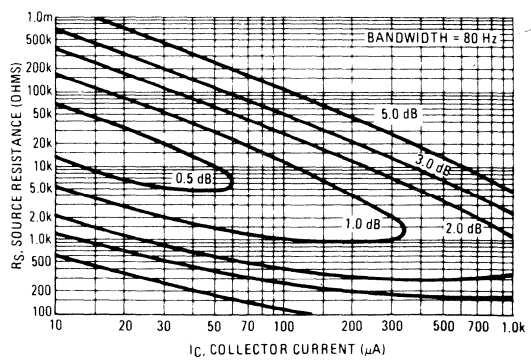


FIGURE 6 – 10 – 50 Hz LOW-FREQUENCY



4

TYPICAL ELECTRICAL CHARACTERISTICS
(V_{CE} = 5.0 V, T_A = 25°C)

FIGURE 7 – NOISE VOLTAGE

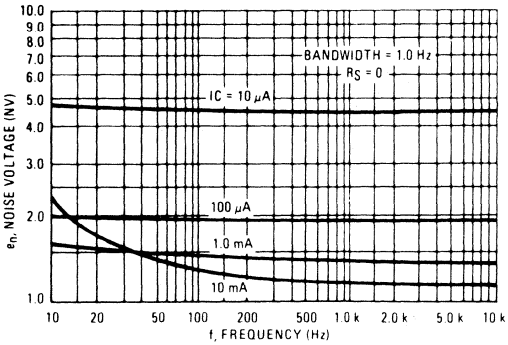


FIGURE 8 – NOISE CURRENT

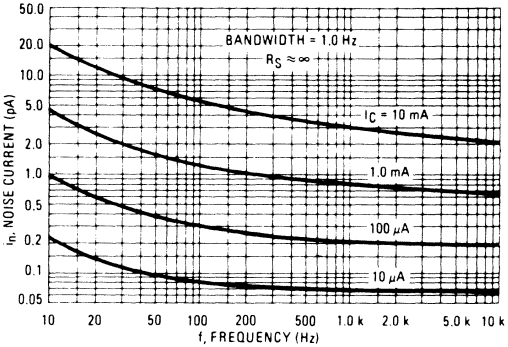


FIGURE 9 – SMALL-SIGNAL CURRENT GAIN

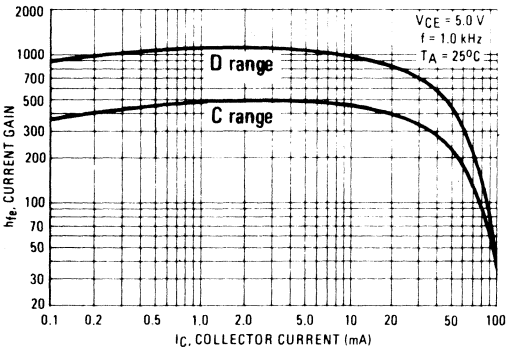


FIGURE 10 – INPUT IMPEDANCE

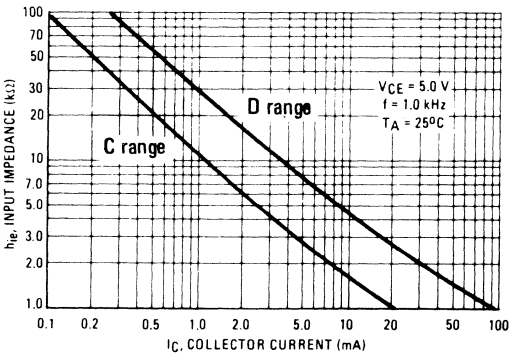


FIGURE 11 – OUTPUT ADMITTANCE

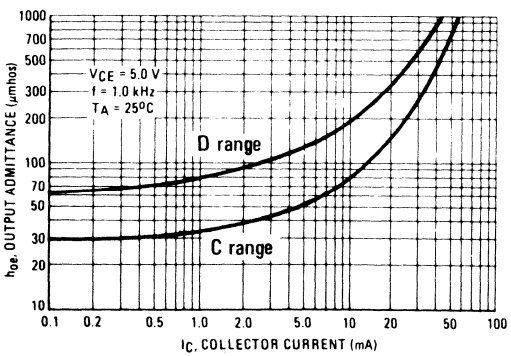


FIGURE 12 – TEMPERATURE COEFFICIENTS

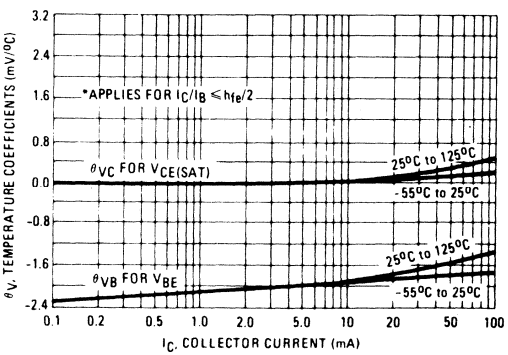


FIGURE 13 – DC CURRENT GAIN

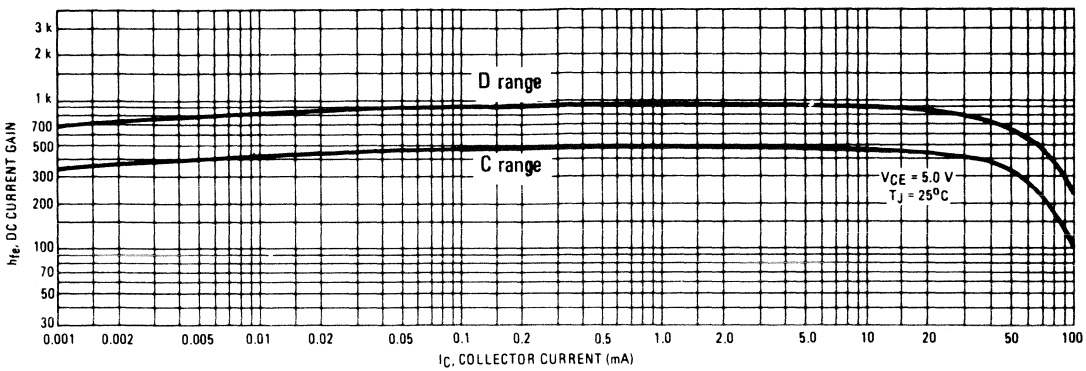


FIGURE 14 – COLLECTOR SATURATION REGION

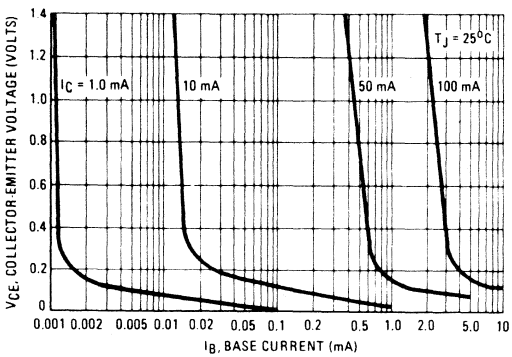


FIGURE 15 – "ON" VOLTAGES

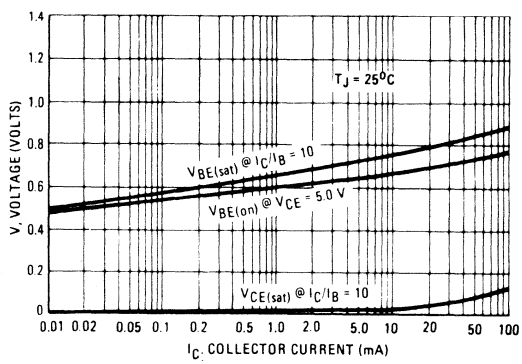


FIGURE 16 – CURRENT-GAIN – BANDWIDTH PRODUCT

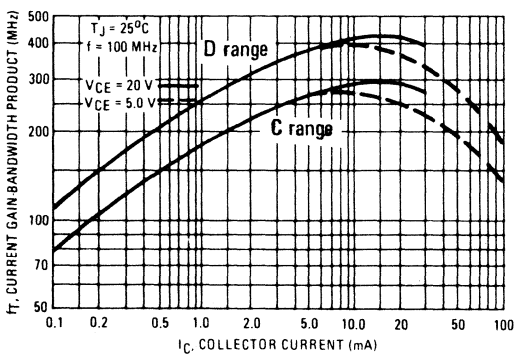
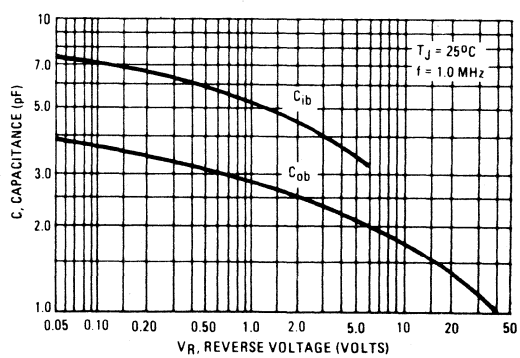


FIGURE 17 – CAPACITANCE



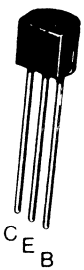
4

NPN SILICON ANNULAR♦ TRANSISTOR

. . . Transistor with low feedback capacitance especially for TV/IF Amplifier

- High detection level
- Low common emitter feedback capacitance
  C_{RE}: 0.25 pF (typ)
- High F_t . 750 MHz (typ)
- Y Parameter characteristics @ 35 MHz

NPN SILICON RF TRANSISTOR

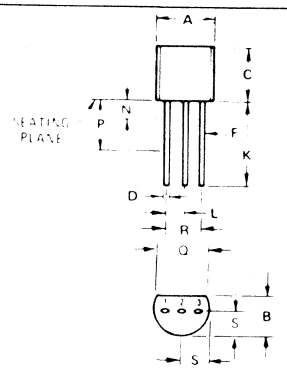


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	25	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	4	Vdc
Collector Current	I_C	100	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25 C	P_D	625 5.0	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	— 55 to + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	200	°C/W
Thermal Resistance, Junction to Case	θ_{JC}	83	°C/W



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700		0.500	
L	1.150	1.390	0.045	0.055
N		1.270		0.050
P	6.350		0.250	
Q	3.430		0.135	
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

♦ Annular Semiconductors Patented by Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min.	Typ	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 2 mAdc, I_B = 0)	BV_{CEO}	25			Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	40			Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	4			Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	I_{CBO}			100	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 7 mAdc, V_{CE} = 10 Vdc)	h_{FE}	40	85		
Base-Emitter On Voltage (I_C = 7 mAdc, V_{CE} = 10 Vdc)	$V_{BE(on)}$		770	900	mVdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 5 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	400	750		MHz
Collector-Base Capacitance (common emitter feedback capacitance) (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{re}		0.25	0.35	pF
Noise figure I_C = 4 mA, V_{CE} = 10 V, R_S = 50 Ω, f = 35 MHz	N_f		2.5		dB

TYPICAL ADMITTANCE PARAMETERS (I_C = 7 mAdc, V_{CE} = 10 Vdc, frequency as stated)

Symbol	f = 35 MHz	Unit
g_{11e}	4.0	mmhos
b_{11e}	7.0	mmhos
g_{22e}	25	μmhos
b_{22e}	380	μmhos
g_{12e}	−15.0	μmhos
b_{12e}	−70.0	μmhos
g_{21e}	150	mmhos
b_{21e}	−35	mmhos

4

FIGURE 1 – DC CURRENT GAIN

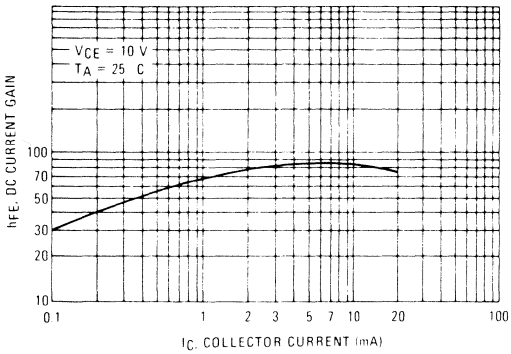


FIGURE 2 – CURRENT GAIN – BANDWITH PRODUCT

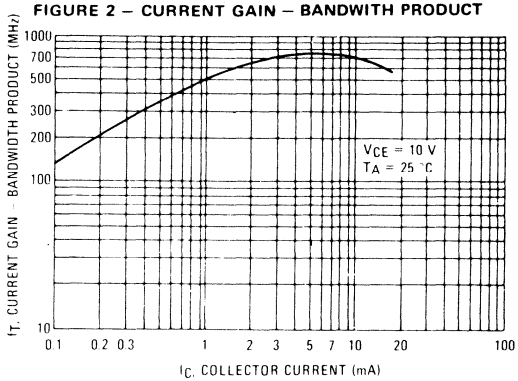


FIGURE 3 – FORWARD TRANSFER ADMITTANCE

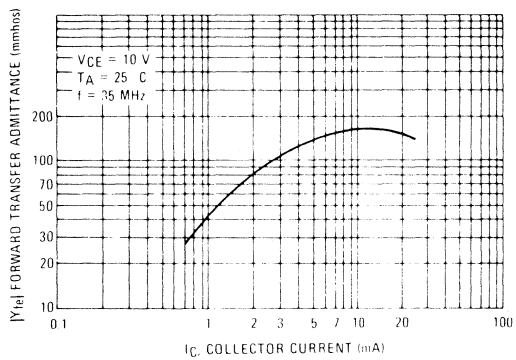


FIGURE 4 – CAPACITANCES

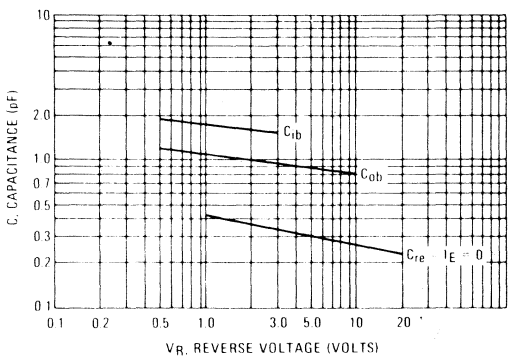
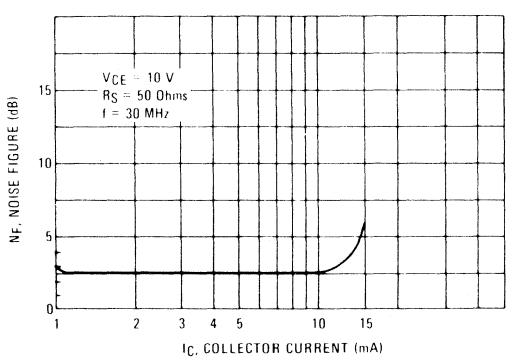


FIGURE 5 – NOISE FIGURE



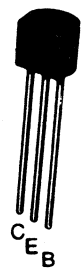
BF240
BF241

NPN SILICON ANNULAR♦ TRANSISTOR

AM/FM Amplifier (Common Emitter Circuit).

Input stages for AM. General RF input, Mixer and oscillator stages.

NPN SILICON RF TRANSISTOR

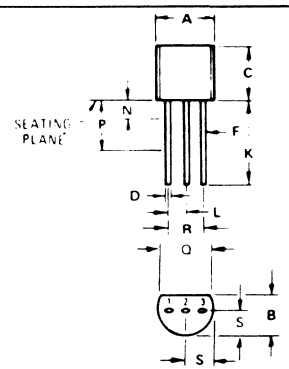


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	4	Vdc
Collector Current	I_C	25	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 2.81	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	— 55 to + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	0.357	°C/mW
Thermal Resistance, Junction to Case	θ_{JC}	0.125	°C/mW



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

♦nnular Semiconductors Patented by Motorola Inc.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min.	Typ	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 2 mAdc, I_B = 0)	BV_{CEO}	40			Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	40			Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	4			Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	I_{CBO}			100	nAdc
ON CHARACTERISTICS					
DC Current Gain I_C = 1 mAdc, V_{CE} = 10 Vdc BF240 BF241	h_{FE}	 67 36		 222 125	
Base-Emitter On Voltage (I_C = 1.0 mAdc, V_{CE} = 10 Vdc)	$V_{BE(on)}$	.65	.70	.74	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 100 MHz) BF 240 BF 241	f_T		600 470		MHz
Collector-Base Capacitance (common emitter feedback capacitance) (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{re}		.28	.34	pF
Noise Figure (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, R_S = 200 Ω – f = 100 KHz R_S = 50 Ω – f = 100 MHz	NF		 2.5	3.5	dB
Output Admittance (I_C = 1mAdc, V_{CE} = 10 Vdc, f = 450 KHz f = 10.7 MHz	g_{oe}			8.3 10.5	μmho μmho

(1) Pulse test: pulse width ≤ 300 μs. Duty cycle ≤ 2.0%

FIGURE 1 – CURRENT GAIN-BANDWIDTH PRODUCT

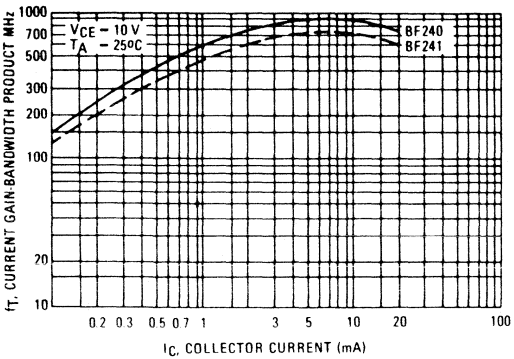


FIGURE 2 – CAPACITANCES

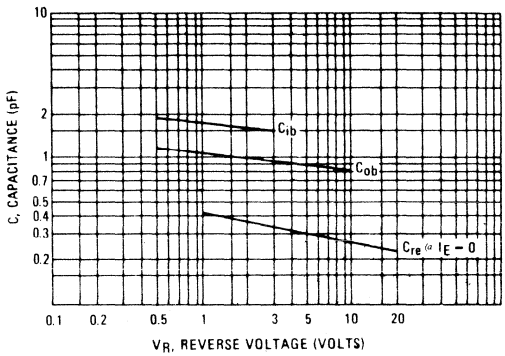


FIGURE 3 – DC CURRENT GAIN

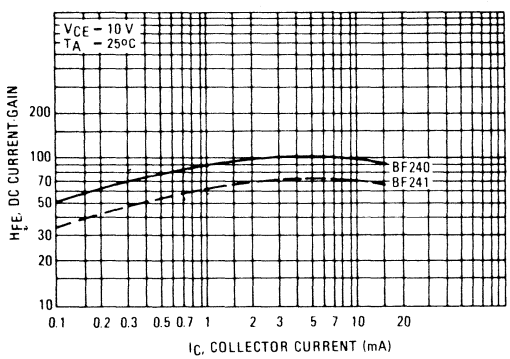


FIGURE 4 – b11e

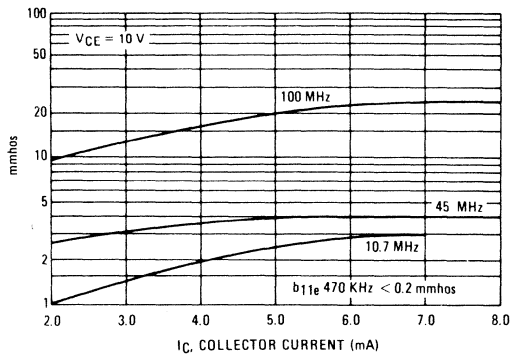


FIGURE 5 – b21e

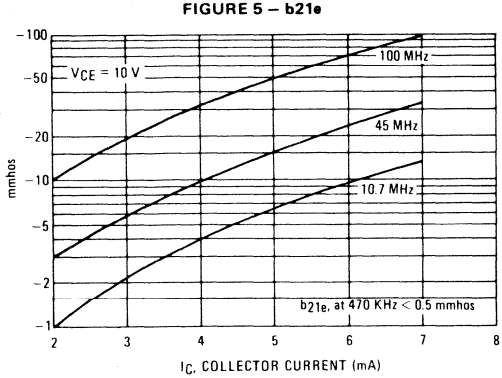
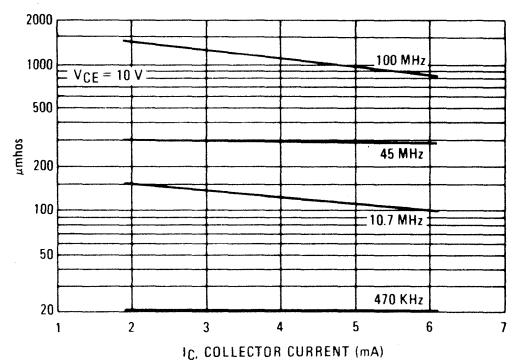


FIGURE 6 – b22e (boe)



4

FIGURE 7 – g11e (gie)

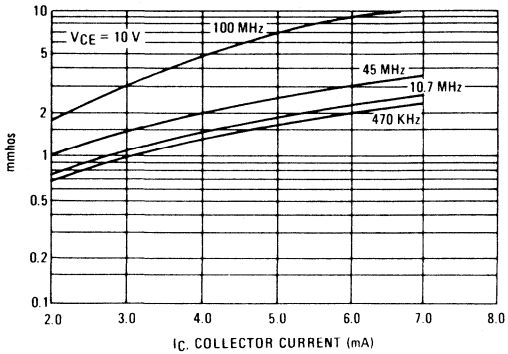


FIGURE 8 – g21e (Yfe)

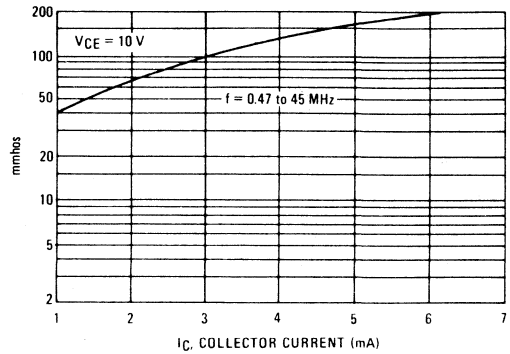
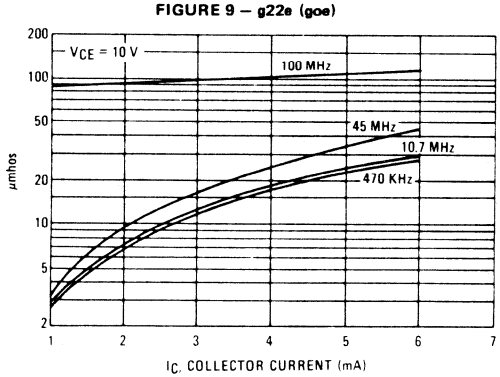


FIGURE 9 – g22e (goe)

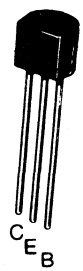


BF254
BF255

NPN SILICON ANNULAR♦ TRANSISTOR

- Designed as a Common emitter amplifier for AM radios and FM/IF stages.
- High output impedance
- Complete Y-Parameter characterisation

NPN SILICON RF TRANSISTOR

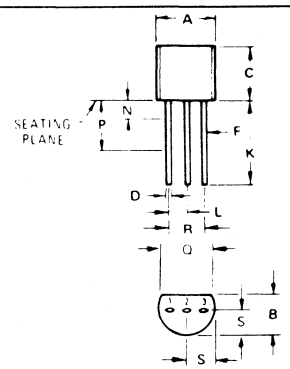


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CB}	30	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current	I_C	100	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	— 55 to + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	Θ_{JA}	200	°C/W
Thermal Resistance, Junction to Case	Θ_{JC}	83	°C/W



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4 450	5 200	0 175	0 205
B	3 180	4 190	0 125	0 165
C	4 320	5 330	0 170	0 210
D	0 407	0 533	0 016	0 021
F	0 407	0 482	0 016	0 019
K	12 700	-	0 500	-
L	1 150	1 390	0 045	0 055
N	-	1 270	-	0 050
P	6 350	-	0 250	-
Q	3 430	-	0 135	-
R	2 410	2 670	0 095	0 105
S	2 030	2 670	0 080	0 105

CASE 29-02
TO-92

♦ Annular Semiconductors Patented by Motorola Inc.

4

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min.	Typ	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	20			Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	BV_{CBO}	30			Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	5.0			Vdc
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}			100	nAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	I_{EBO}			100	nAdc
ON CHARACTERISTICS					
DC Current Gain I_C = 1.0 mA, V_{CE} = 10 Vdc BF254 BF254-3 BF254-4 BF255 BF255-2 BF255-3	h_{FE}	 65 65 100 35 35 65		 220 125 220 125 75 125	
Base-Emitter On Voltage (I_C = 1.0 mAdc, V_{CE} = 10 Vdc) BF254 BF255	$V_{BE(on)}$		0.68		Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 100 MHz) BF254 BF255	f_T		260 200		MHz
Collector-Base Capacitance (common emitter feedback capacitance) (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{re}		0.90		pF
Noise Figure (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1 MHz, R_S = 50 ohms)	NF		1.7		dB

TYPICAL ADMITTANCE PARAMETERS (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, frequency as stated)

Symbol	f = 450 KHz		f = 10.7 MHz		Unit
	BF254	BF255	BF254	BF255	
g_{11e}	.20	.40	.26	.5	mmhos
b_{11e}	.05	.06	1.2	1.6	mmhos
g_{22e}	3.0	1.5	5.3	4.5	μmhos
b_{22e}	8.0	8.0	190	190	μmhos
b_{12e}	−5.0	−5.0	−130	−130	μmhos
g_{12e}	−0.7	−0.4	−3.0	−3.5	μmhos
g_{21e}	30	30	30	30	mmhos
b_{21e}	−0.003	−0.004	−0.7	−1.0	mmhos

FIGURE 1 – DC CURRENT GAIN

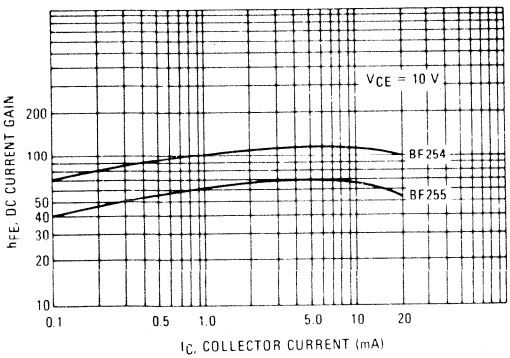


FIGURE 2 – CURRENT GAIN–BANDWITH PRODUCT

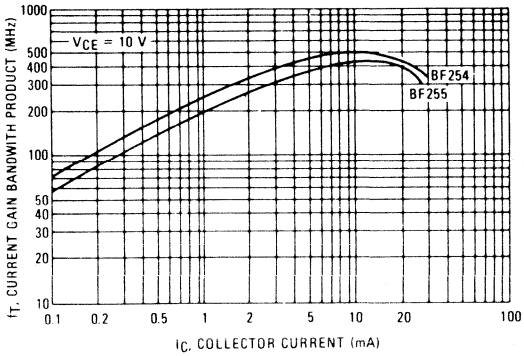


FIGURE 3 – "ON" VOLTAGE

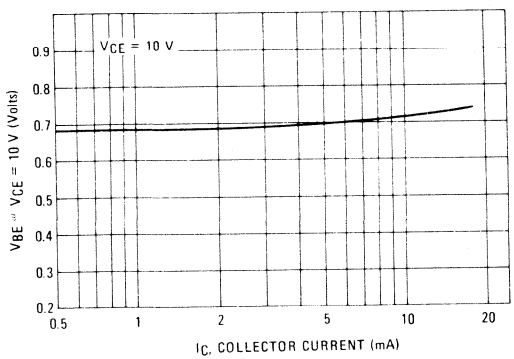
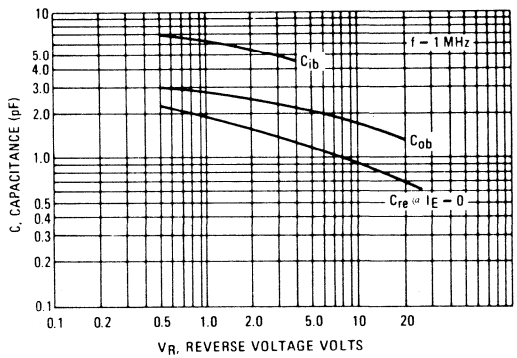


FIGURE 4 – CAPACITANCES



4

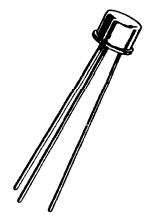
BF257
BF258 • BF259

NPN SILICON ANNULAR♦ TRANSISTORS

. . . designed for high-voltage DC - VHF video amplifier applications.

- High Collector-Emitter Breakdown Voltage –
  BV_{CEO} = 300 (Min) @ I_C = 30 mAdc – BF259
- Low Collector Cutoff Current –
  I_{CBO} = 50 nAdc (Max) @ V_{CB} = 250 Vdc – BF259
- DC Current Gain –
  h_{FE} = 25 (Min) @ I_C = 30 mAdc

NPN SILICON AMPLIFIER TRANSISTORS



MAXIMUM RATINGS

Rating	Symbol	BF257	BF258	BF259	Unit
Collector-Emitter Voltage	V_{CEO}	160	250	300	Vdc
Collector-Emitter Voltage	V_{CER}	160	250	300	Vdc
Collector-Base Voltage	V_{CB}	160	250	300	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current – Continuous	I_C	← 100 →			mAdc
Total Device Dissipation @ T_C = 25°C	P_D	← 5.0 →			Watts
Operating Junction Temperature Range	T_J	← +175 →			°C

THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	30	°C/W

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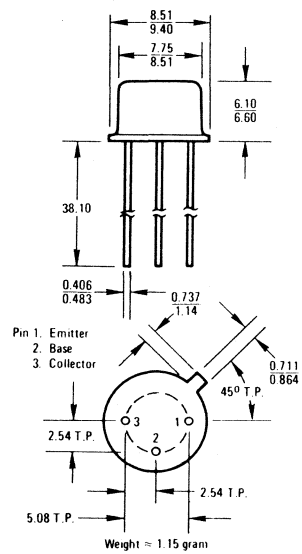


CASE 31 (1)
TO-5
All Dimensions in Millimeters

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage		BV_{CEO}				Vdc
(I_C = 30 mAdc, I_B = 0)	BF257		160	–	–	
	BF258		250	–	–	
	BF259		300	–	–	
Collector-Base Breakdown Voltage		BV_{CBO}				Vdc
(I_C = 100 μAdc, I_E = 0)	BF257		160	–	–	
	BF258		250	–	–	
	BF259		300	–	–	
Emitter-Base Breakdown Voltage		BV_{EBO}	5.0	–	–	Vdc
(I_E = 100 μAdc, I_C = 0)						
Collector Cutoff Current		I_{CBO}				nAdc
(V_{CB} = 100 Vdc, I_E = 0)	BF257		–	–	50	
(V_{CB} = 200 Vdc, I_E = 0)	BF258		–	–	50	
(V_{CB} = 250 Vdc, I_E = 0)	BF259		–	–	50	
ON CHARACTERISTICS						
DC Current Gain		h_{FE}	25	–	–	–
(I_C = 30 mAdc, V_{CE} = 10 Vdc)						
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	–	–	1.0	Vdc
(I_C = 30 mAdc, I_B = 6.0 mAdc)						
DYNAMIC CHARACTERISTICS						
Current-Gain – Bandwidth Product		f_T	–	110	–	MHz
(I_C = 30 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)						
Reverse Transfer Capacitance		C_{re}	–	3.5	–	pF
(V_{CB} = 30 Vdc, I_E = 0, f = 500 kHz)						
Collector-Base Capacitance		C_{cb}	–	5.5	–	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 500 kHz)						

BF491
BF492 • BF493

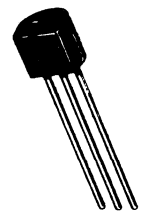
SILICON ANNULAR♦ TRANSISTORS

. . . designed for high voltage video applications in television receivers requiring high breakdown voltage and low capacitance.

– High Collector-Emitter Breakdown Voltage @ I_C = 1.0 mAdc

BV_{CEO} =	200 Vdc	BF491
	250 Vdc	BF492
	300 Vdc	BF493

PNP SILICON HIGH VOLTAGE TRANSISTORS



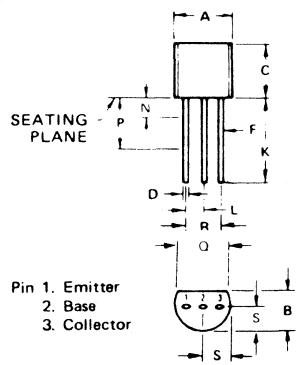
MAXIMUM RATINGS

Rating	Symbol	BF491	BF492	BF493	Unit
Collector-Emitter Voltage	V_{CEO}	200	250	300	Vdc
Collector-Base Voltage	V_{CB}	200	250	300	Vdc
Emitter-Base Voltage	V_{EB}	6.0	8.0	8.0	Vdc
Collector Current—Continuous	I_C	500			mAdc
Total Device Dissipation @ T_A = 25 °C Derate Above 25 °C	P_D	625 1.2			mW mW/°C
Total Device Dissipation @ T_C = 25 °C Derate Above 25 °C	P_D	1.5 12			Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	83.3	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	200	°C/W

♦ Annular Semiconductors Patented by Motorola Inc.



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Characteristics		Symbol	Min	Max	Unit
Off Characteristics					
Collector-Emitter Breakdown Voltage (1)		BV_{CEO}			Vdc
(I_C = 1 mAdc, I_B = 0)	BF491		200	–	
	BF492		250	–	
	BF493		300	–	
Collector-Base Breakdown Voltage		BV_{CBO}			Vdc
(I_C = 100 μAdc, I_E = 0)	BF491		200	–	
	BF492		250	–	
	BF493		300	–	
Emitter-Base Breakdown Voltage		BV_{EBO}			Vdc
(I_E = 100 μAdc, I_C = 0)	BF491		6.0	–	
	BF492		8.0	–	
	BF493		8.0	–	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 160 Vdc, I_E = 0)	BF491		–	0.1	
(V_{CB} = 200 Vdc, I_E = o)	BF492		–	0.1	
(V_{CB} = 200 Vdc, I_E = 0)	BF493		–	0.1	
Emitter Cutoff Current		I_{EBO}			μAdc
(V_{BE} = 4.0 Vdc, I_C = 0)	BF491		–	0.1	
(V_{BE} = 6.0 Vdc, I_C = 0)	BF492		–	0.1	
(V_{BE} = 6.0 Vdc, I_C = 0)	BF493		–	0.1	
On Characteristics					
DC Current Gain		h_{FE}			–
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)	All Types		25	–	
(I_C = 10 mAdc, V_{CE} = 10 Vdc)	All Types		40	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 20 mAdc, I_B = 2.0 mAdc)				2.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 20 mA, I_B = 2.0 mA)				2.0	
Dynamic Characteristics					
Current-Gain – Bandwidth Product		f_T			MHz
(I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 20 MHz			50	–	
Collector-Base Capacitance		C_{re}			pF
(V_{CB} = 100 Vdc, I_E = 0, f = 1.0 MHz)				1.6	

(1) Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

4

FIGURE 1 – DC CURRENT GAIN

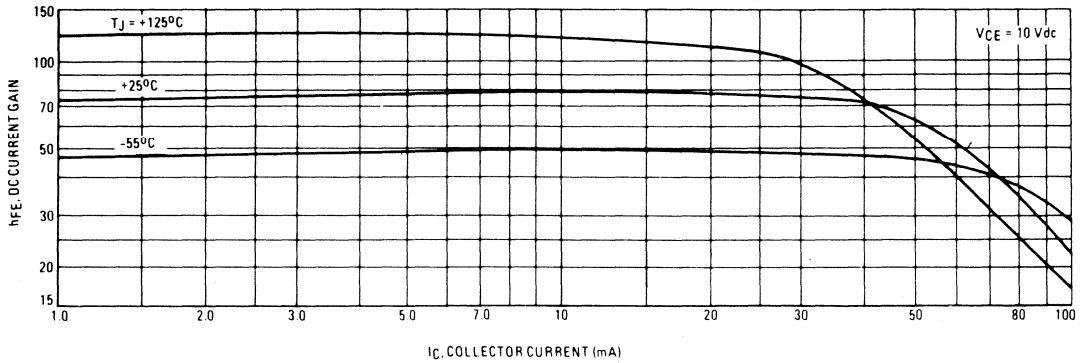


FIGURE 2 – CAPACITANCES

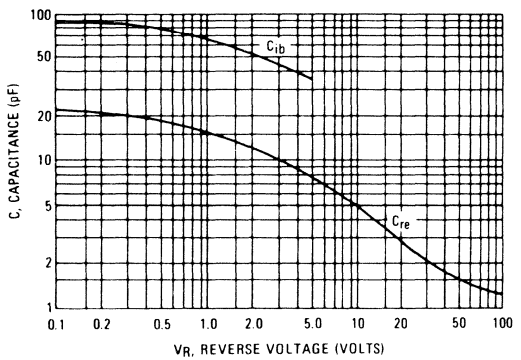


FIGURE 3 – CURRENT-GAIN–BANDWIDTH PRODUCT

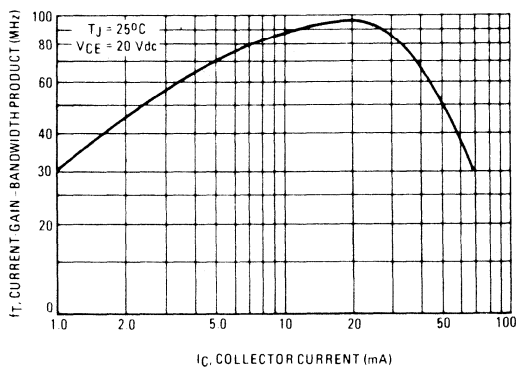


FIGURE 4 – "ON" VOLTAGES

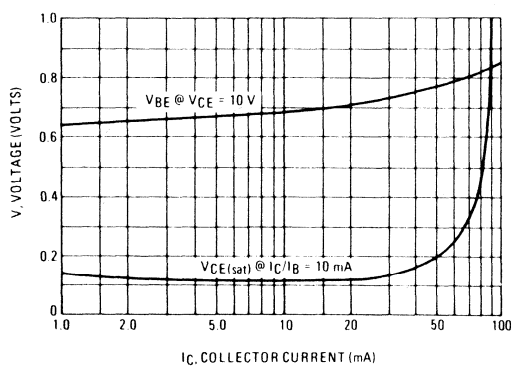
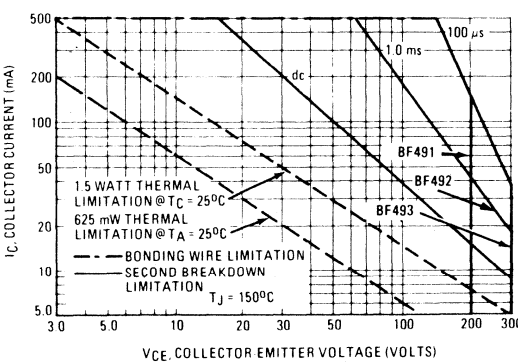


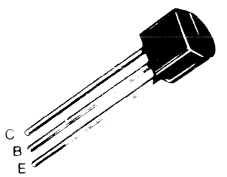
FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA

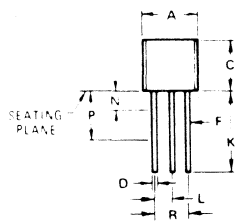


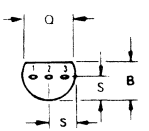
PNP SILICON ANNULAR♦ TRANSISTOR DESIGNED FOR TV TUNER APPLICATIONS AS VHF OSCILLATOR AND MIXER

- High Oscillator Power
- Low Cross Modulation
- Plastic TO-92 Package

PNP SILICON VHF TRANSISTOR







STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	4	Vdc
Collector current	I_C	50	mAdc
Total Device Dissipation @ T_A = 25 °C Derate above 25 °C	P_D	625 5.00	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	0.200	°C/mW

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

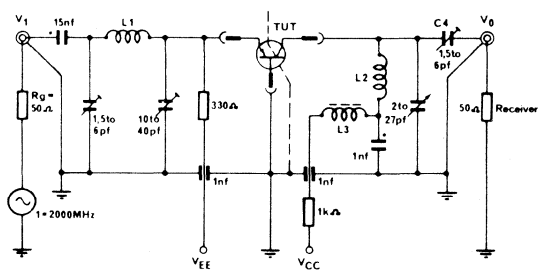
CASE 29-02
TO-92

♦ Annular Semiconductors Patented by Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	BV_{CEO}	35	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	40	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	4	–	–	Vdc
Collector Cutoff Current (V_{CB} = 20 V, I_E = 0)	I_{CBO}	–	–	100	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 3 mAdc, V_{CE} = 10 Vdc)	h_{FE}	20	–	–	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 1 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	400	600	–	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{CBO}	–	0.6	0.9	pF
Feedback Capacitance (Grounded Base) (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{rb}	–	0.15	0.25	pF
Noise Figure (I_C = 1 mA, R_S = 50 Ω, f = 200 MHz, V_{CC} = 6 V)	N_F	–	2.5	4	dB
Power Gain (I_C = 3 mA, R_L = 1 KΩ, f = 200 MHz, V_{CC} = 10.8 V)	G_{pb}	14	22	–	dB

200 MHz POWER GAIN NOISE FIGURE TEST CIRCUIT



• Leadless ceramic disc capacitor
L1 = 3 turns 0.0 mm enamel, 4 mm dia
L2 = 2 turns 1 mm enamel, 6.5 mm dia

FIGURE 1 – CURRENT GAIN – BANDWIDTH PRODUCT

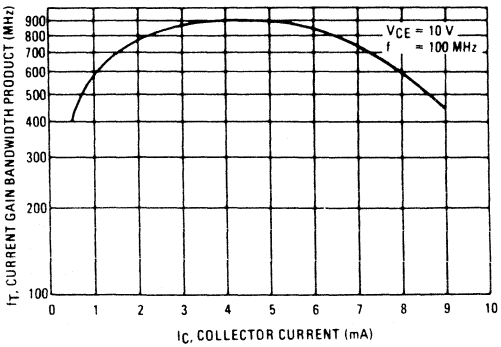


FIGURE 2 – NOISE FIGURE

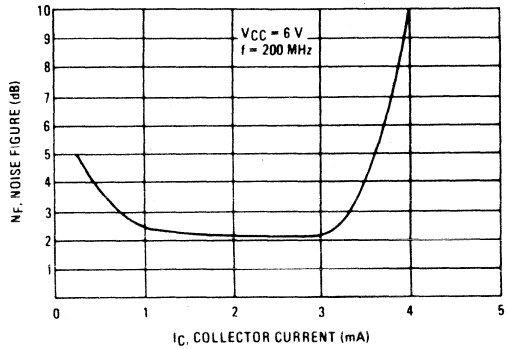


FIGURE 3 – FORWARD TRANSFER ADMITTANCE

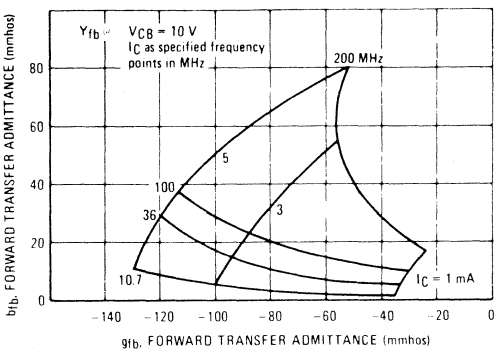


FIGURE 4 – INPUT ADMITTANCE

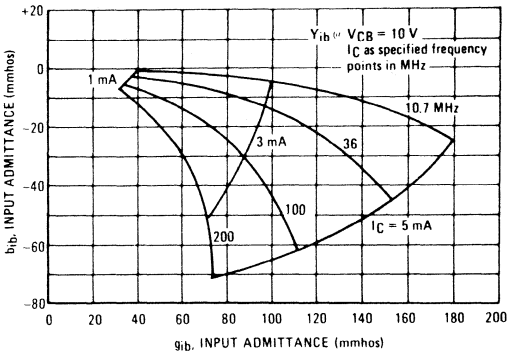
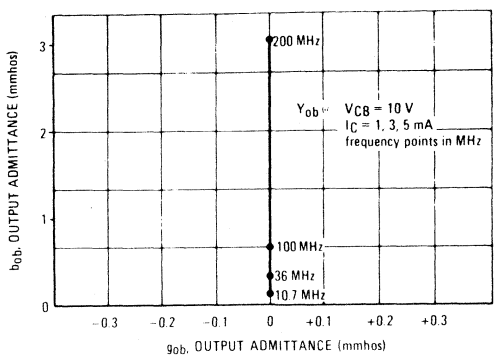


FIGURE 5 – OUTPUT ADMITTANCE



4

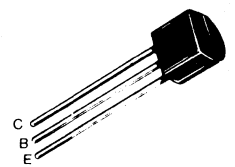
BF509

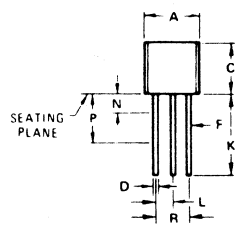
PNP SILICON ANNULAR♦ TRANSISTOR DESIGNED FOR TV TUNER APPLICATIONS

To be used as VHF Amplifier

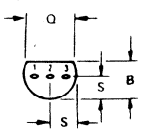
- High Power Gain
- Low Noise Figure
- Guaranteed AGC Range for 35 dB Gain Reduction at 200 MHz
- Plastic TO-92 Package

PNP SILICON VHF TRANSISTOR





STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4 450	5 200	0 175	0 205
B	3 180	4 190	0 125	0 165
C	4 320	5 330	0 170	0 210
D	0 407	0 533	0 016	0 021
F	0 407	0 482	0 016	0 019
K	12 700	–	0 500	–
L	1 150	1 390	0 045	0 055
N	–	1 270	–	0 050
P	6 350	–	0 250	–
Q	3 430	–	0 135	–
R	2 410	2 670	0 095	0 105
S	2 030	2 670	0 080	0 105

CASE 29-02
TO-92

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	4	Vdc
Collector current	I_C	50	mAdc
Total Device Dissipation @ T_A = 25 °C Derate above 25 °C	P_D	625 5.00	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	0.200	°C/mW

♦ Annular Semiconductors Patented by Motorola Inc.

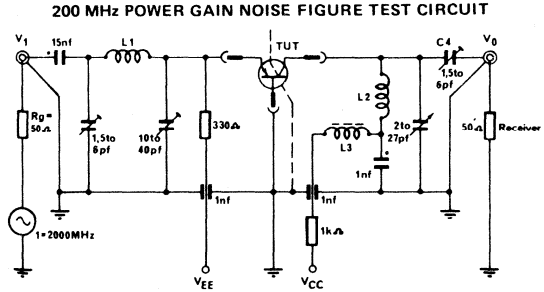
ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	BV_{CEO}	35	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	40	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	4	–	–	Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	I_{CBO}	–	–	100	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 3 mAdc, V_{CE} = 10 Vdc)	h_{FE}	20	–	–	
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product (I_C = 3 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	600	850	–	MHz
Feedback Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{rb}	–	.15	.25	pF
Collector base capacitance (V_{CB} = 10 V, I_E =0, f = 1.0 MHz)	C_{CBO} (Cre)	–	0.6	0.9	pF
Noise Figure (I_C = 3 mAdc, V_{CC} = 10.8 V R_S = 50 Ohms, f = 200 MHz)	NF	–	–	2.5	dB
FUNCTIONAL TEST (see test jig fig 1)					
Common-base Amplifier Power Gain (I_C = 3 mAdc, V_{CC} = 10.8 V, R_L = 1 KΩ, f = 200 MHz)	G_{pb}	15	22	–	dB
Forward AGC Current $I_{C(Agc)}$ (Gain Reduction = 30 dB, R_S = 50 Ohms, V_{CC} = 10.8 V, f = 200 MHz)	$I_{C(Agc)}$	6	–	8.8	mAdc

AGC CHARACTERISTICS

V_{CC} = 10.8 Vdc, R_S = 50 Ohms, f = 200 MHz, See Figure 1 and 2.

200 MHz POWER GAIN NOISE FIGURE TEST CIRCUIT



*Leadless ceramic disk capacitor
L1 – 3 turns 0.0 mm enamel, 4 mm dia
L2 – 2 turns 1 mm enamel, 6.5 mm dia

4

FIGURE 1 – DC CURRENT GAIN

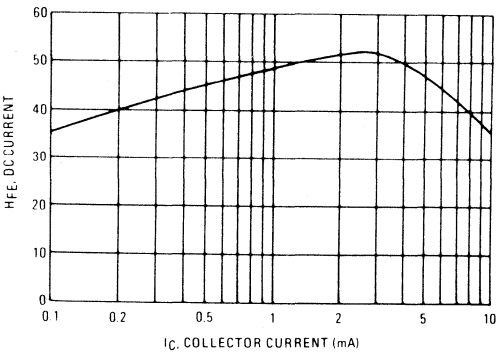


FIGURE 2 – CURRENT GAIN – BANDWIDTH PRODUCT

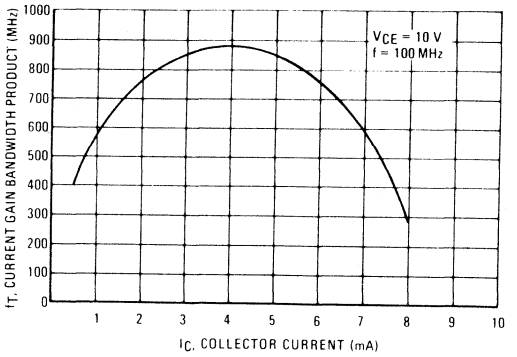


FIGURE 3 – CAPACITANCES

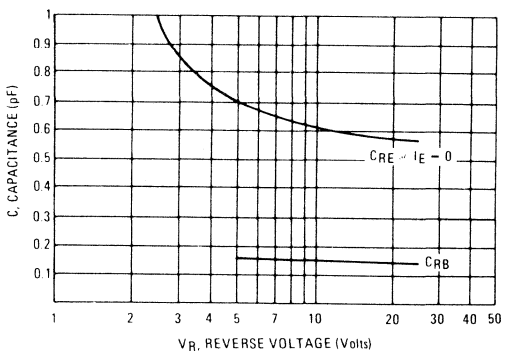


FIGURE 4 – TYPICAL POWER GAIN

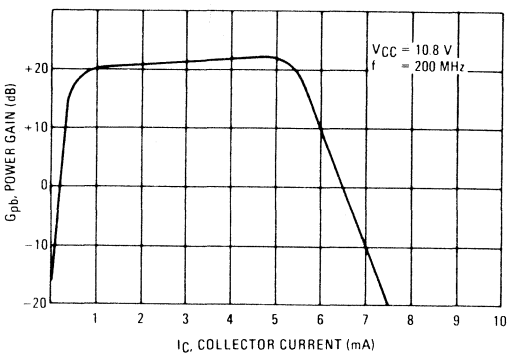


FIGURE 5 – FORWARD TRANSFER ADMITTANCE

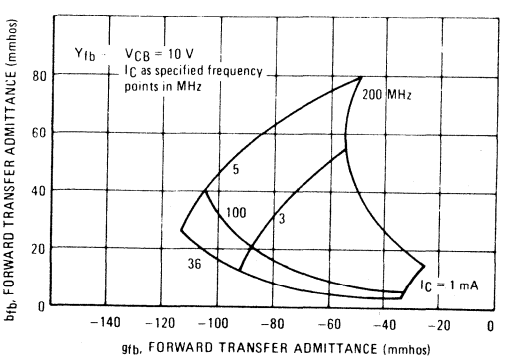


FIGURE 6 – INPUT ADMITTANCE

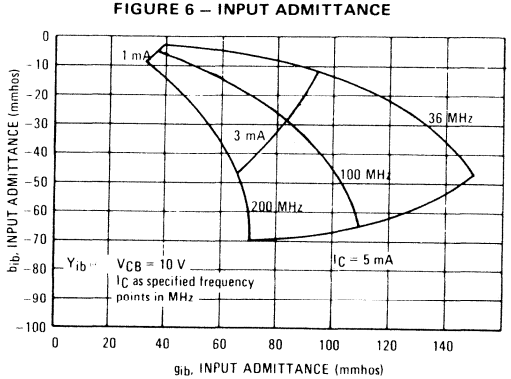
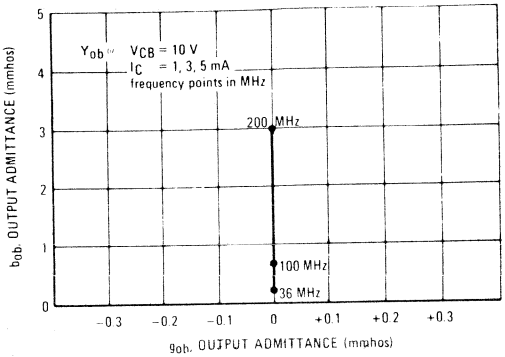


FIGURE 7 – OUTPUT ADMITTANCE



4

NPN

BF787/788/789

PNP

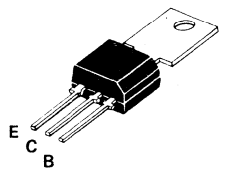
BF790/791/792

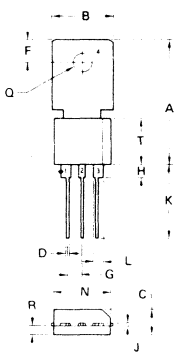
SILICON ANNULAR♦ HIGH VOLTAGE AMPLIFIER TRANSISTORS LOW CRE

. . . electrically Low CRE identical in Duowatt package to BF469/470, and BF471/472 Case 77.
Designed for high-voltage TV video and chroma output circuits, high-voltage linear amplifiers, and high-voltage transistor regulators.

- High Collector-Emitter Breakdown Voltage — BV_{CEO} = 350 Vdc (Min) @ I_C = 1.0 mAdc — BF789/792.
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.0 V (Max) @ I_C = 10 mAdc.
- Low Collector Base Capacitance — C_{re} = 1.8 pF (Max) @ V_{CB} = 30 Vdc.
- Duowatt Package — 2 Watts Free Air Dissipation @ T_A = 25 °C.

COMPLEMENTARY SILICON AMPLIFIER TRANSISTORS





STYLE 2
PIN 1 EMITTER
2 COLLECTOR
3 BASE
4 COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.56	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.78	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.041	0.069
T	7.87	9.14	0.310	0.360

CASE 306-04

MAXIMUM RATINGS

Ratings	Symbol	BF787 BF790	BF788 BF791	BF789 BF792	Unit
Collector-Emitter Voltage	V_{CEO}	250	300	350	Vdc
Collector-Base Voltage	V_{CBO}	250	300	350	Vdc
Collector Current — Continuous Peak	I_C	0.1 0.2			Adc
Total Power Dissipation @ T_A = 25 °C Derate above 25 °C	P_D	2.0 16			Watts mW/°C
Total Power Dissipation @ T_C = 25 °C Derate above 25 °C	P_D	10 40			Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	−55 to +150			°C
Solder Temperature, 1/16" from Case for 10 Seconds	—	260			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	25	°C/W

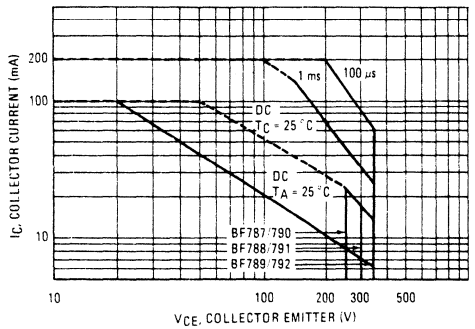
ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Characteristic		Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Voltage (I_C = 1.0 mAdc, I_B = 0)	BF787/790 BF788/791 BF789/792	BV_{CEO}	 250 300 350		Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	BF787/790 BF788/791 BF789/792	BV_{CBO}	 250 300 350		Bdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)		BV_{EBO}	 5		Vdc
Collector-Cutoff Current (V_{CB} = 150 Vdc, I_E = 0) (V_{CB} = 200 Vdc, I_E = 0) (V_{CB} = 250 Vdc, I_E = 0)	 BF787/790 BF788/791 BF789/792	I_{CBO}		 0.2 0.2 0.2	μAdc
Emitter-Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}		10	μAdc
Collector-cutoff Current (V_{CE} = 150 Vdc, V_{BE} = 0) (V_{CE} = 200 Vdc, V_{BE} = 0) (V_{CE} = 250 Vdc, V_{BE} = 0)	 BF787/790 BF788/791 BF789/792	I_{CES}		 10 10 10	μAdc
ON CHARACTERISTICS[1]					
DC Current Gain (I_C = 25 mAdc, V_{CE} = 20 Vdc)		h_{FE}	50		
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)		$V_{CE(sat)}$		1	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Gandwidth Product (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)		f_T	60		MHz
Common-Emitter Reverse Transfer Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 1.0 MHz)		C_{re}		1.8	pF
Collector-Saturation RF Voltage (I_C = 25 mA)		$V_{CE(sat)}$ hf	Typical 20		V

[1] Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

4

FIGURE 1 – ACTIVE-REGION SAFE-OPERATING AREA



TYPICAL CHARACTERISTICS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 1 is based on $T_{J(pk)}$ = 150 °C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycle to 10% provided $T_{J(pk)} \leq 150$ °C. $T_{J(pk)}$ may be calculated from the data in figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

FIGURE 2 – DC CURRENT GAIN

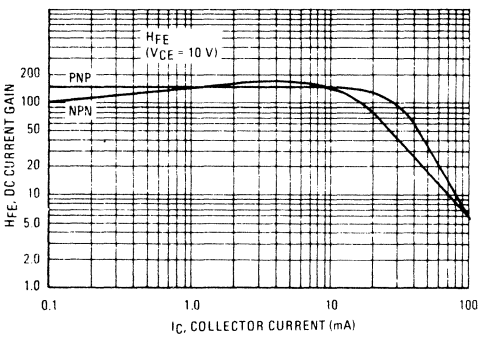


FIGURE 3 – SATURATION VOLTAGE

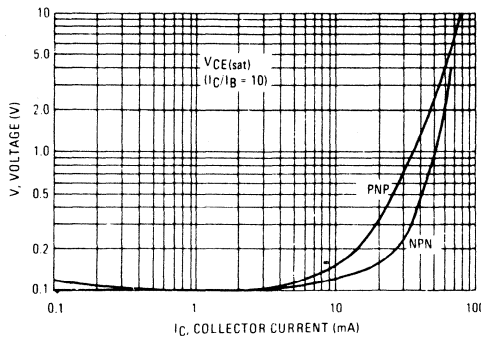
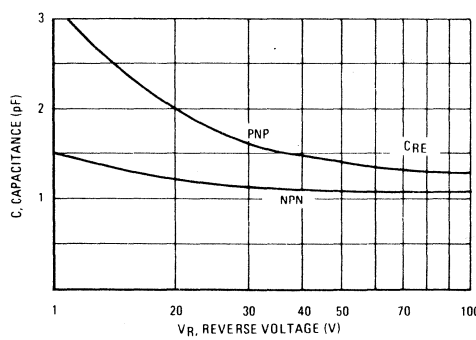


FIGURE 4 – CAPACITANCE



BF 959

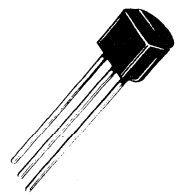
NPN SILICON HIGH-FREQUENCY TRANSISTORS

DESIGNED PRIMARILY FOR USE WITH

SURFACE ACOUSTIC WAVE FILTER

- HIGH CURRENT - GAIN - BANDWIDTH PRODUCT
- FT 1.6 GHz (TYP) Ic = 20 mA
- Low cross modulation distortion at high
- current.

NPN SILICON
RF TRANSISTOR

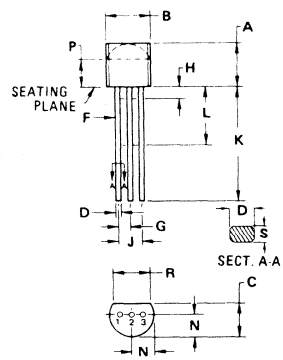


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CB}	30	Vdc
Emitter-Base Voltage	V_{EB}	3	Vdc
Collector current	I_C	50	mAdc
Total Device Dissipation @ T_A 25 C Derate above 25 C	P_D	625 5.00	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	0.200	°C/mW



STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

CASE 29-02
TO-92

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DS5670

4

ELECTRICAL CHARACTERISTICS (T_A = 25 C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	20	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 10 µAdc, I_E = 0)	BV_{CBO}	30	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 µAdc, I_C = 0)	BV_{EBO}	3.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0	I_{CBO}	–	–	100	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5mAdc, V_{CE} = 10 Vdc) (I_C = 20mAdc, V_{CE} = 10 Vdc)	h_{FE}	35 40			
Collector-Emitter Saturation Voltage (I_C = 30mAdc, I_B = 2.0mAdc)	$V_{CE\ (sat)}$			1.0	Vdc
Base-Emitter Saturation Voltage (I_C = 30mAdc, I_B = 2.0mAdc)	$V_{BE\ (sat)}$			1	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain-Bandwidth Product (I_C = 20mAdc, V_{CE} = 10 Vdc, f = 100 MHz) (I_C = 30mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	ft	700 600			MHz
Collector-Base Capacitance (common emitter feedback capacitance) (V_{CB} = 10 Vdc, P_f = 0 f = 10 MHz)	C_{re}		0.65		pF
Noise figure (I_C = 4mA, V_{CE} = 10 V, R_S = 50 Ω, f = 200 MHz)	N_f		3		dB

FIGURE 1 – Hfe AT 10 V

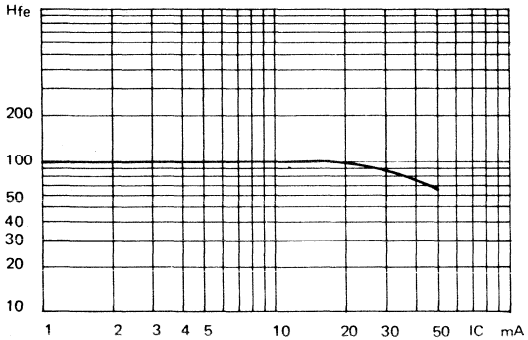


FIGURE 2 – VCE Sat AT IC/IB = 10

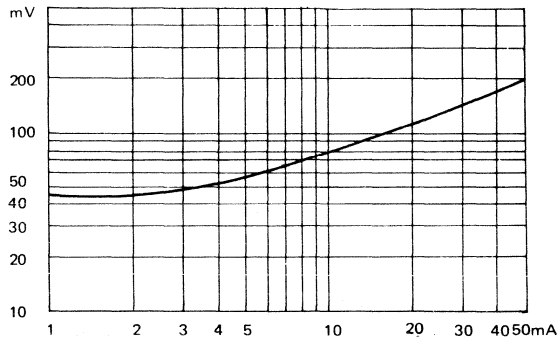


FIGURE 3 – CURRENT-GAIN – BANDWIDTH-PRODUCT

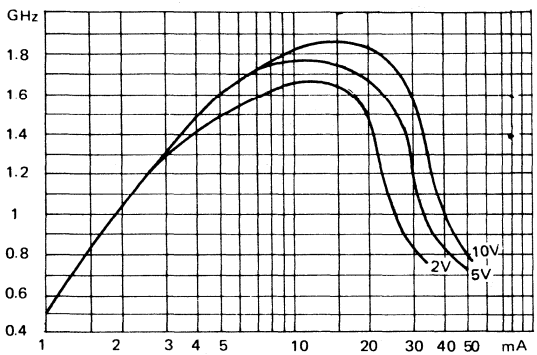


FIGURE 4 – CAPACITANCES

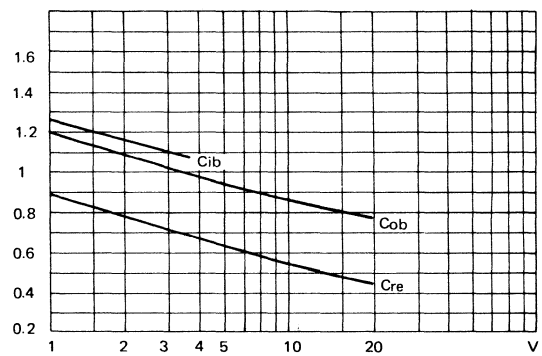


FIGURE 5 – INPUT IMPEDANCE AT 30 MHz

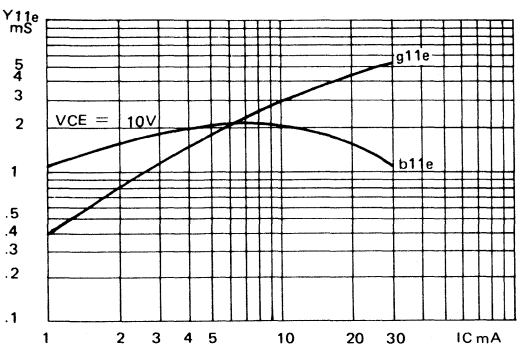
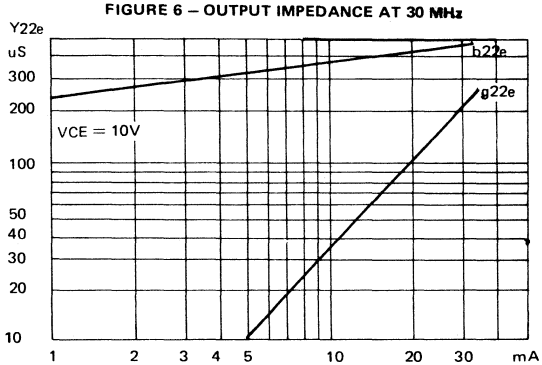


FIGURE 6 – OUTPUT IMPEDANCE AT 30 MHz



4

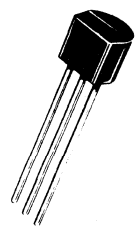
MPS-A05, MPS-A06 (NPN)
MPS-A55, MPS-A56 (PNP)

COMPLEMENTARY SILICON ANNULAR♦
AMPLIFIER TRANSISTORS

. . . designed for use as medium-power driver and low-power outputs.

- High Collector-Emitter Breakdown Voltage –
  BV_{CEO} = 60 Vdc (Min) @ I_C = 1.0 mAdc – MPS-A05, MPS-A55
  = 80 Vdc (Min) @ I_C = 1.0 mAdc – MPS-A06, MPS-A56
- Excellent Current-Gain Linearity –
  1.0 mAdc to 150 mAdc – MPS-A55, MPS-A56
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.25 Vdc (Max) @ I_C = 100 mAdc

COMPLEMENTARY SILICON
AMPLIFIER TRANSISTORS



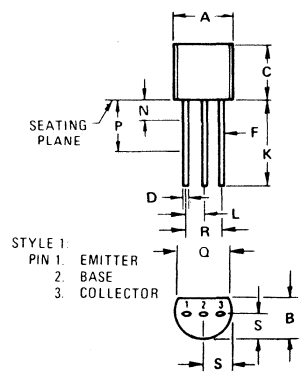
MAXIMUM RATINGS

Rating	Symbol	MPS-A05 MPS-A55	MPS-A06 MPS-A56	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	4.0		Vdc
Collector Current – Continuous	I_C	500		mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0		mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12		Watts mW/°C
Operating and Storage Temperature Temperature Range	T_J,T_{stg}	-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	oC/W

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

♦Annular Semiconductors Patented by Motorola Inc.

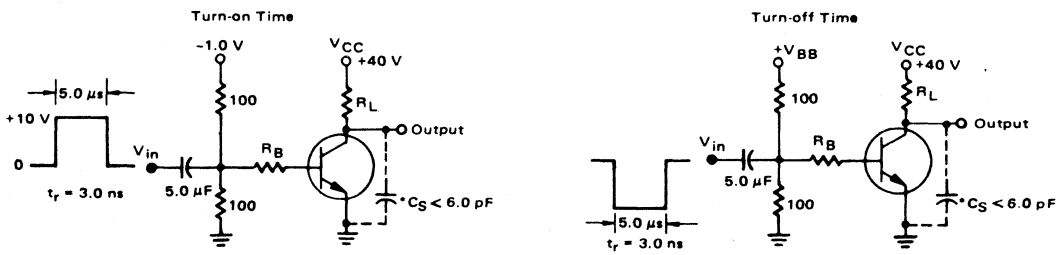
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 1.0 mAdc, I_B = 0)	MPS-A05, MPS-A55	BV_{CEO}	60	–	Vdc
	MPS-A06, MPS-A56		80	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	4.0	–	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0)		I_{CEO}	–	0.1	μAdc
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 60 Vdc, I_E = 0)	MPS-A05, MPS-A55		–	0.1	
(V_{CB} = 80 Vdc, I_E = 0)	MPS-A06, MPS-A56		–	0.1	
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)			50	–	
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)			50	–	
Collector-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)		$V_{CE(sat)}$	–	0.25	Vdc
Base-Emitter On Voltage (I_C = 100 mAdc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	–	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain–Bandwidth Product (2) (I_C = 10 mAdc, V_{CE} = 2.0 Vdc, f = 100 MHz)		f_T	100	–	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

FIGURE 1 – SWITCHING TIME TEST CIRCUITS



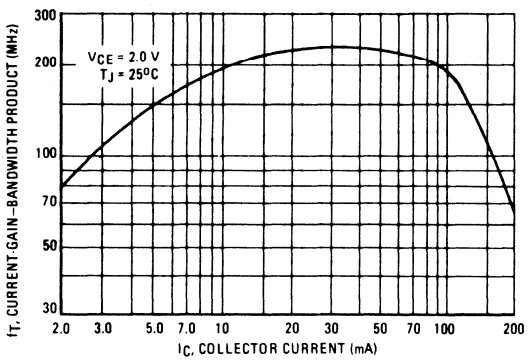
*Total Shunt Capacitance of Test Jig and Connectors
For PNP Test Circuits, Reverse All Voltage Polarities

4

NPN
MPS-A05, MPS-A06

PNP
MPS-A55, MPS-A56

FIGURE 2 – CURRENT-GAIN–BANDWIDTH PRODUCT



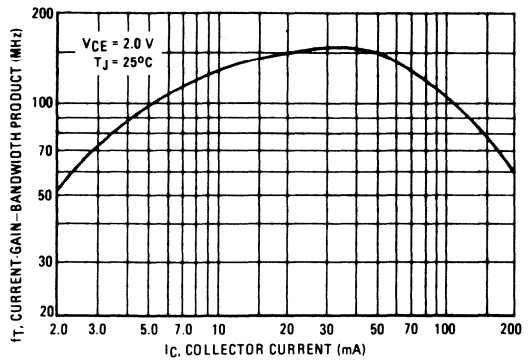
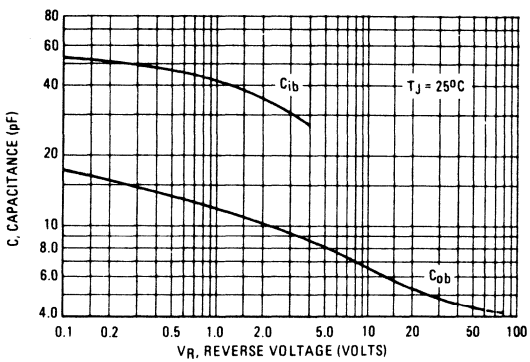


FIGURE 3 – CAPACITANCE



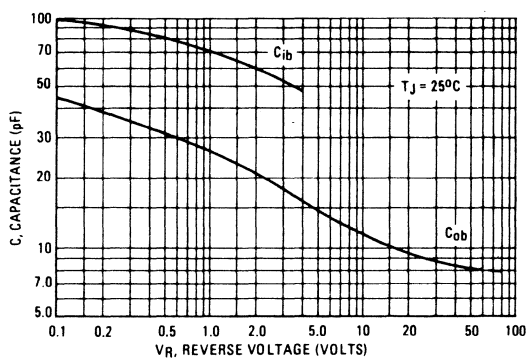
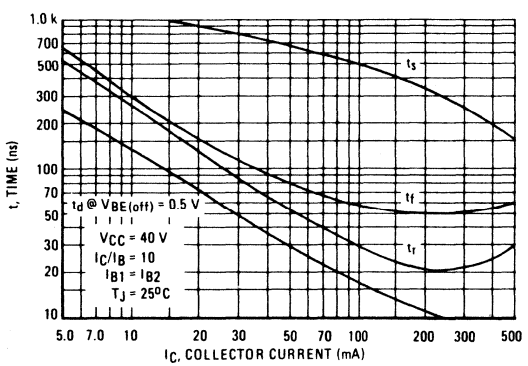


FIGURE 4 – SWITCHING TIME



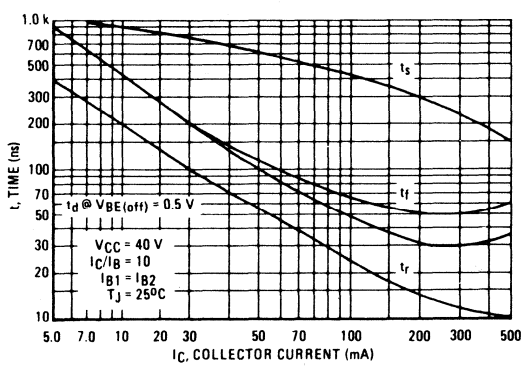


FIGURE 5 – THERMAL RESPONSE

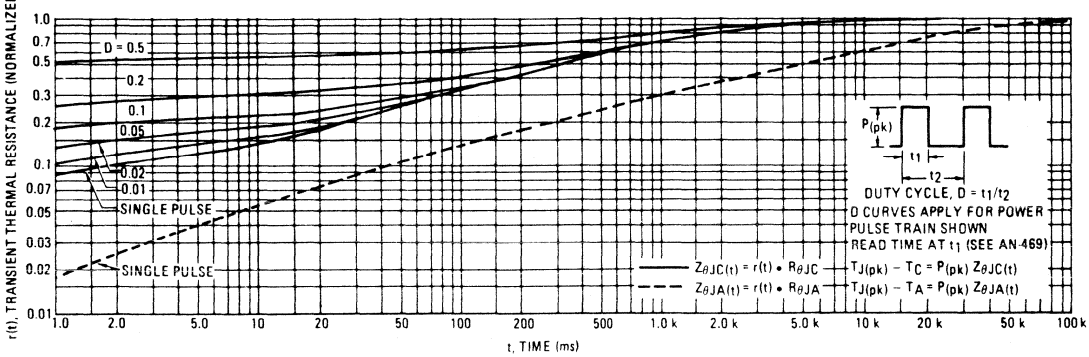
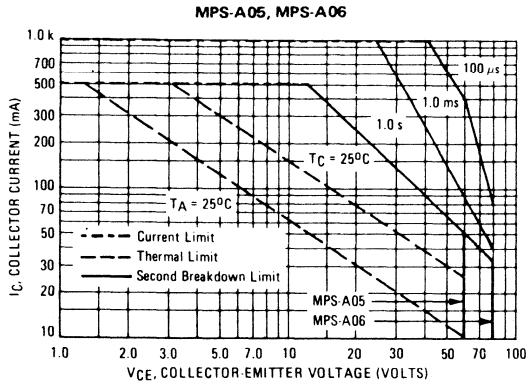
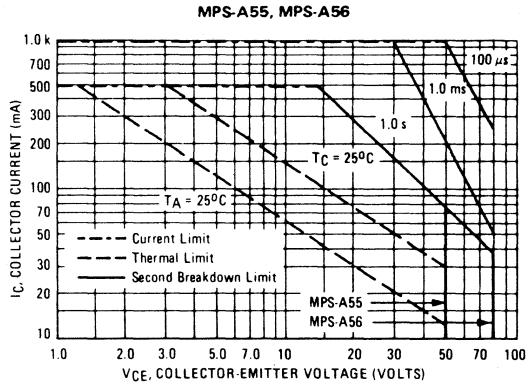


FIGURE 6 – ACTIVE – REGION SAFE OPERATING AREA





4

The safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 6 is based upon $T_{J(pk)} = 150^oC$; T_C or T_A is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case or ambient temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by the secondary breakdown. (See AN-415A)

NPN
MPS-A05, MPS-A06

FIGURE 7 – DC CURRENT GAIN

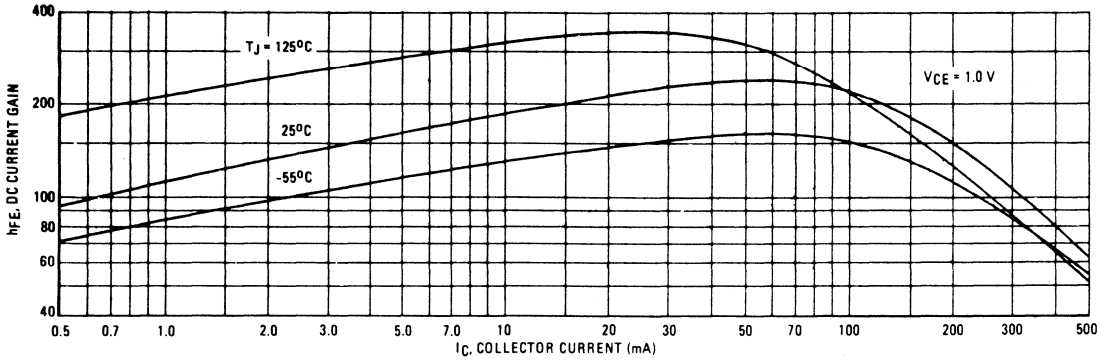


FIGURE 8 – "ON" VOLTAGES

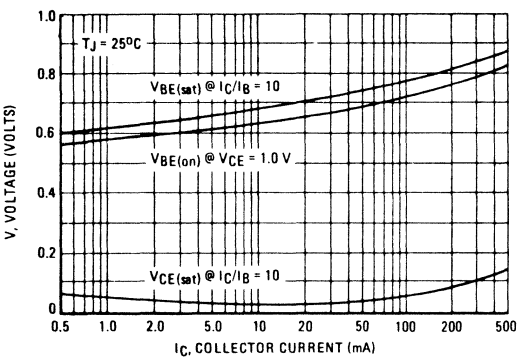


FIGURE 9 – COLLECTOR SATURATION REGION

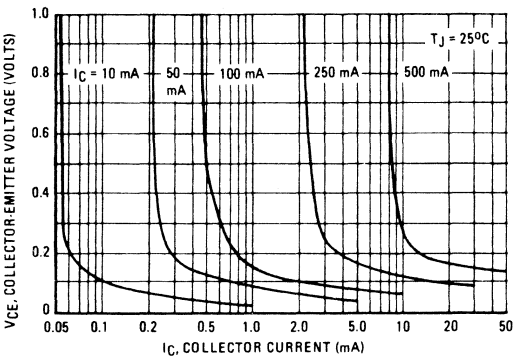
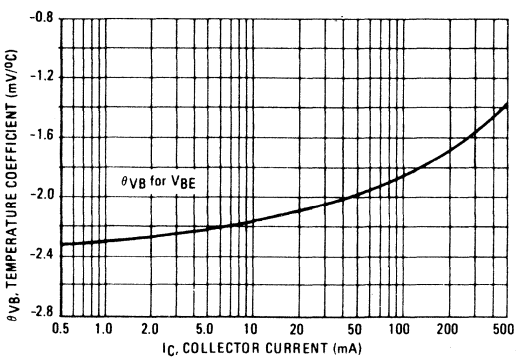


FIGURE 10 – BASE-EMITTER TEMPERATURE COEFFICIENT



PNP
MPS-A55, MPS-A56

FIGURE 11 – DC CURRENT GAIN

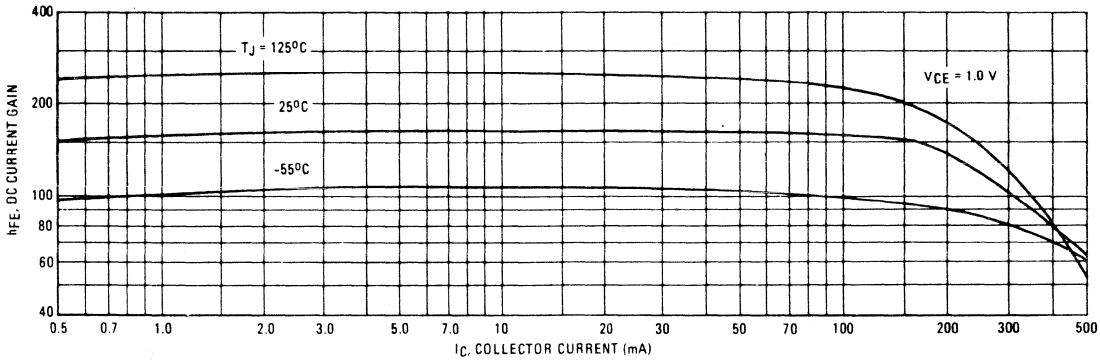


FIGURE 12 – "ON" VOLTAGES

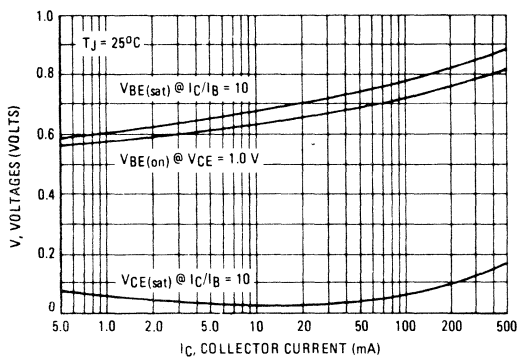


FIGURE 13 – COLLECTOR SATURATION REGION

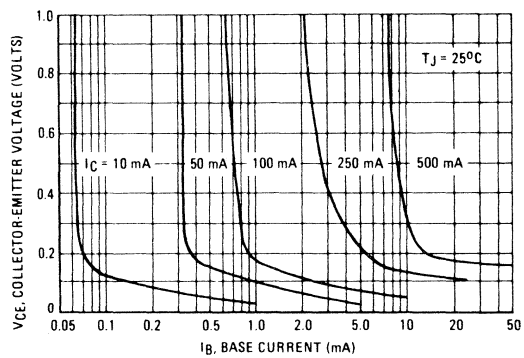
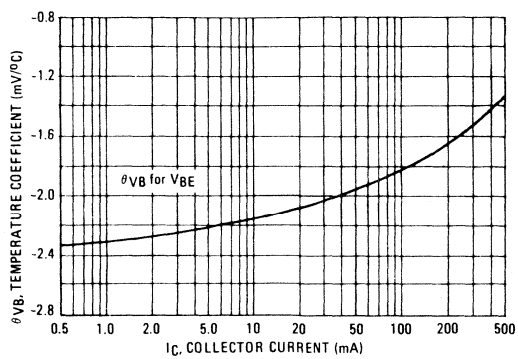


FIGURE 14 – BASE-EMITTER TEMPERATURE COEFFICIENT



4

MPS-A13
MPS-A14

NPN SILICON DARLINGTON AMPLIFIER TRANSISTORS

. . . designed for pre-amplifier input applications requiring high input impedance.

- High DC Current Gain –
  h_{FE} = 5,000 (Min) @ I_C = 10 mAdc (MPS-A13)
  10,000 (Min) @ I_C = 10 mAdc (MPS-A14)
- Collector-Emitter Breakdown Voltage –
  BV_{CES} = 30 Vdc (Min) @ I_C = 10 mAdc
- Low Noise Figure –
  NF = 2.0 dB (Typ) @ I_C = 1.0 mAdc
- Monolithic Construction for High Reliability

NPN SILICON DARLINGTON TRANSISTORS

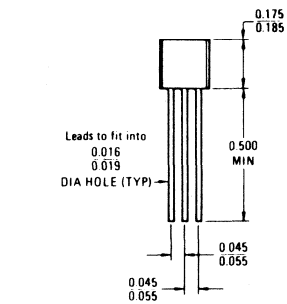
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}*	30	Vdc
Collector-Emitter Voltage	V_{CES}	30	Vdc
Collector-Base Voltage	V_{CB}	30	Vdc
Emitter-Base Voltage	V_{EB}	10	Vdc
Collector Current – Continuous	I_C	300	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	500 4.54	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +135	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	0.220	°C/mW

*Due to the monolithic construction of this device, breakdown voltages of both transistors are identical. BV_{CES} is tested in lieu of BV_{CEO} in order to avoid errors caused by noise pickup. The voltage measured during the BV_{CES} test is the BV_{CEO} of the output transistor.



CASE 29 (1)
TO-92

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 100 μAdc, I_B = 0)		BV_{CES}	30	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)		I_{CBO}	–	–	100	nAdc
Emitter Cutoff Current (V_{BE} = 10 Vdc, I_C = 0)		I_{EBO}	–	–	100	nAdc
ON CHARACTERISTICS						
DC Current Gain		h_{FE}				–
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)	MPS-A13		5000	–	–	
	MPS-A14		10,000	--	–	
(I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	MPS-A13		10,000	–	–	
	MPS-A14		20,000	–	–	
Collector-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 0.1 mAdc)		$V_{CE(sat)}$	–	0.8	1.5	Vdc
Base-Emitter On Voltage (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	–	1.25	2.0	Vdc
SMALL-SIGNAL CHARACTERISTICS						
Current-Gain–Bandwidth Product (I_C = 10 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)		f_T	125	200	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	5.0	–	pF
Noise Figure (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, R_S = 100 k ohms, f = 1.0 kHz)		NF	–	2.0	–	dB

4

FIGURE 1 – NORMALIZED DC CURRENT GAIN

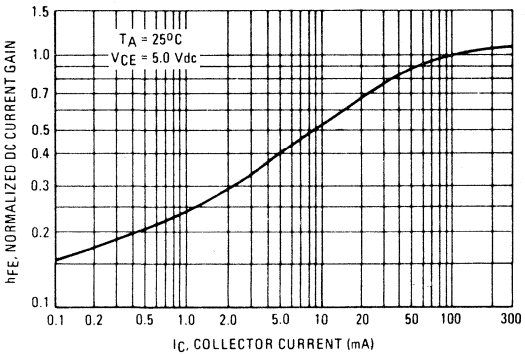


FIGURE 2 – BASE EMITTER "ON" VOLTAGE

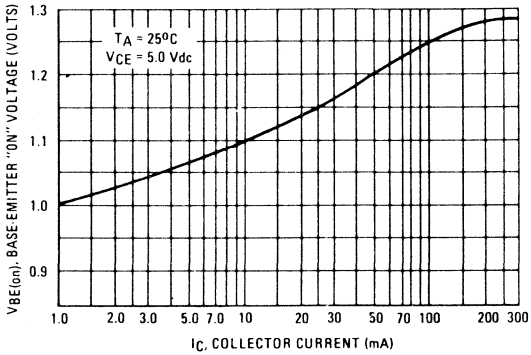


FIGURE 3 – TRANSCONDUCTANCE versus FREQUENCY

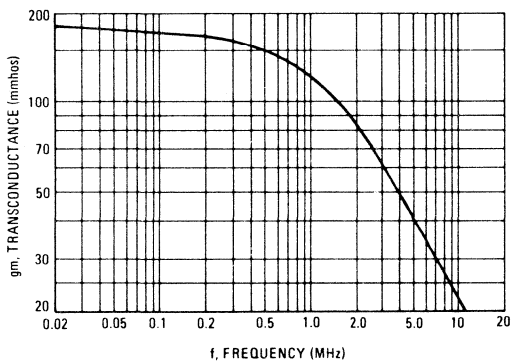


FIGURE 4 – NOISE FIGURE versus CURRENT

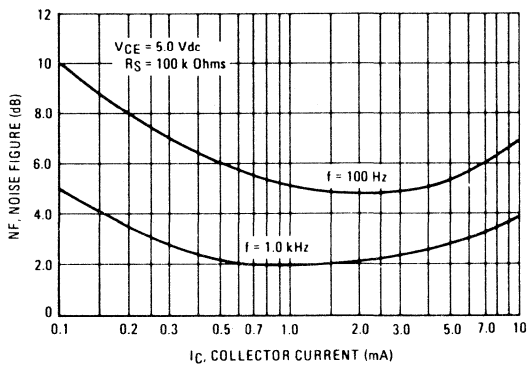


FIGURE 5 – NOISE FIGURE versus FREQUENCY

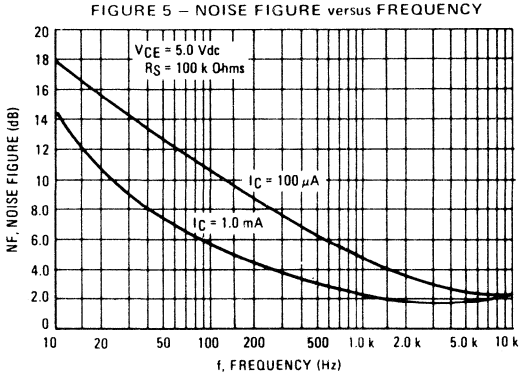
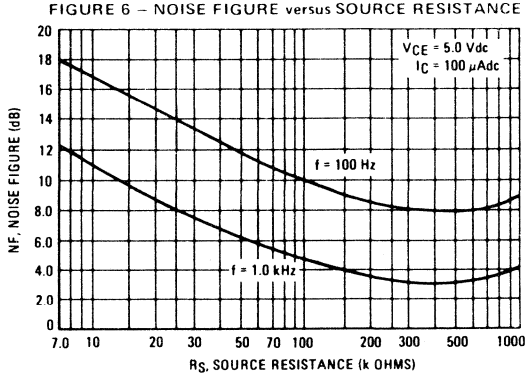


FIGURE 6 – NOISE FIGURE versus SOURCE RESISTANCE



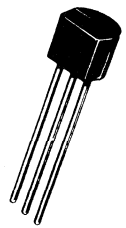
MPS-A16
MPS-A17

NPN SILICON ANNULAR♦ TRANSISTORS

. . . designed for use in moderate speed switching and clipping applications that require large input voltage capability.

- High-Emitter-Base Breakdown Voltage –
  BV_{EBO} = 12 Vdc (Min) @ I_E = 0.1 mAdc – MPS-A16
  = 15 Vdc (Min) @ I_E = 0.1 mAdc – MPS-A17

NPN SILICON TRANSISTORS



MAXIMUM RATINGS

Rating	Symbol	MPS-A16	MPS-A17	Unit
Collector-Emitter Voltage	V_{CEO}	40		Vdc
Emitter-Base Voltage	V_{EB}	12	15	Vdc
Collector Current – Continuous	I_C	100		mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 2.73		mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		°C

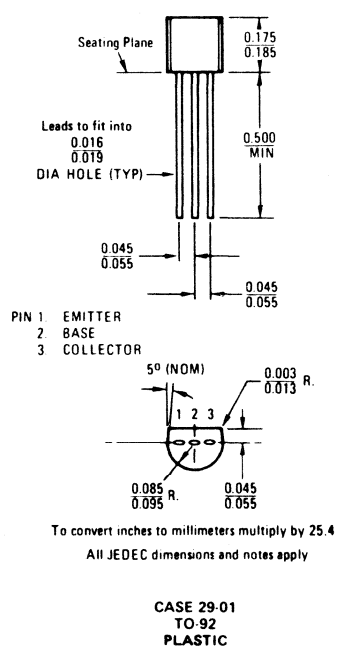
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	0.357	°C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	40	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0) MPS-A16 / MPS-A17	BV_{EBO}	12 15	– –	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	100	nAdc
Emitter Cutoff Current (V_{BE} = 10 Vdc, I_C = 0)	I_{EBO}	–	100	nAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 5.0 mAdc, V_{CE} = 10 Vdc)	h_{FE}	200	600	–
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{CE(sat)}$	–	0.25	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain–Bandwidth Product (I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 100 MHz) MPS-A16 / MPS-A17	f_T	100 80	– –	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	4.0	pF

♦Annular Semiconductors Patented by Motorola Inc.



To convert inches to millimeters multiply by 25.4

All JEDEC dimensions and notes apply

CASE 29-01
TO-92
PLASTIC

4

FIGURE 1 - DC CURRENT GAIN

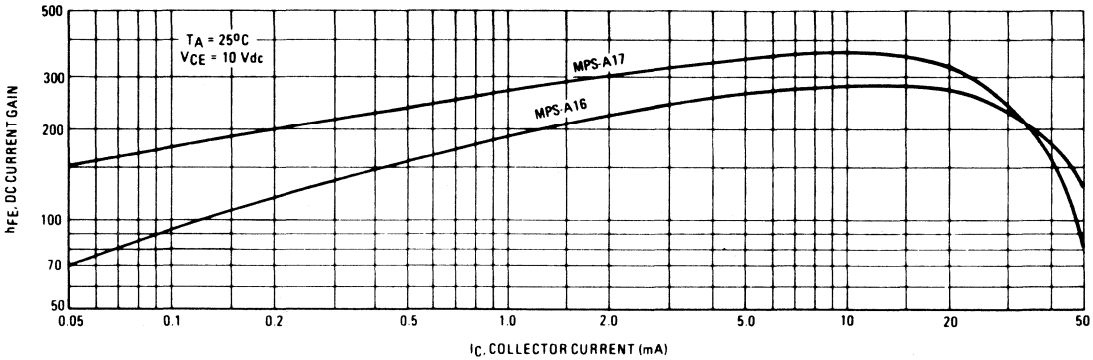


FIGURE 2 - SMALL SIGNAL CURRENT GAIN

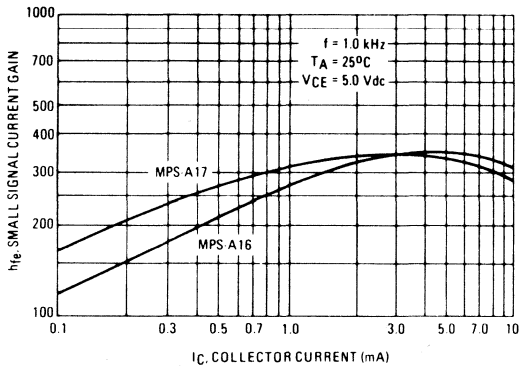


FIGURE 3 - SATURATION AND ON VOLTAGES

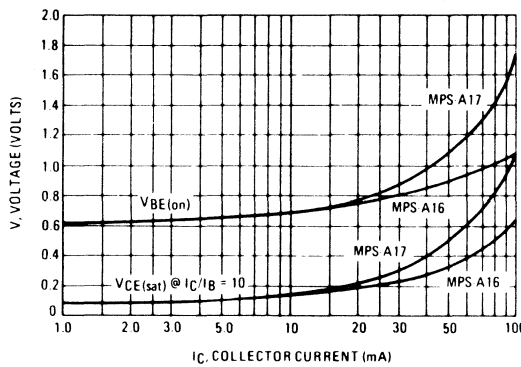


FIGURE 4 - CURRENT GAIN - BANDWIDTH PRODUCT

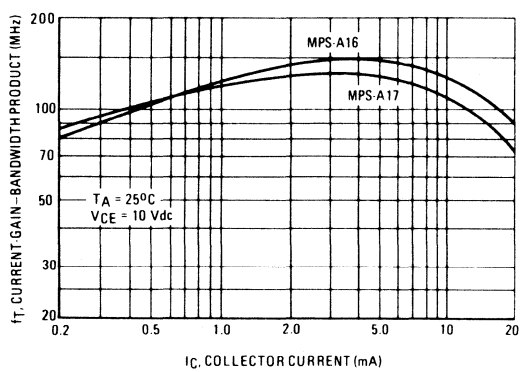
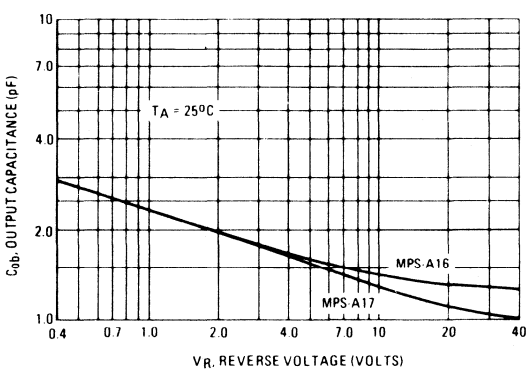


FIGURE 5 - OUTPUT CAPACITANCE



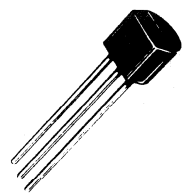
MPS-A62
MPS-A63 • MPS-A64

PNP SILICON DARLINGTON AMPLIFIER TRANSISTORS

. . . designed for pre-amplifier input applications requiring high input impedance.

- High DC Current Gain @ I_C = 10 mAdc –
  h_{FE} = 5,000 (Min) MPS-A63
  10,000 (Min) MPS-A64
  20,000 (Min) MPS-A62
- Collector-Emitter Breakdown Voltage –
  BV_{CES} = 30 Vdc (Min) @ I_C = 100 μAdc – MPS-A63, MPS-A64
- Low Noise Figure –
  NF = 2.0 dB (Typ) @ I_C = 1.0 mAdc – MPS-A63, MPS-A64
- Monolithic Construction
- Complements to NPN MPS-A12, MPS-A13, MPS-A14

PNP SILICON DARLINGTON TRANSISTORS

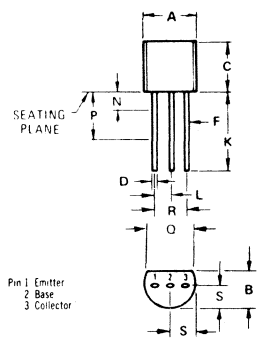


MAXIMUM RATINGS

Rating	Symbol	MPS-A62	MPS-A63 MPS-A64	Unit
Collector-Emitter Voltage	V_{CES}	20	30	Vdc
Collector-Base Voltage	V_{CB}	20	30	Vdc
Emitter-Base Voltage	V_{EB}	10		Vdc
Collector Current – Continuous	I_C	300		mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0		mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

4

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage		BV_{CES}				Vdc
(I_C = 100 μAdc, V_{BE} = 0)	MPS-A62		20	–	–	
	MPS-A63, MPS-A64		30	–	–	
Collector Cutoff Current		I_{CBO}				nAdc
(V_{CB} = 15 Vdc, I_E =0)	MPS-A62		–	–	100	
(V_{CB} = 30 Vdc, I_E =0)	MPS-A63, MPS-A64		–	–	100	
Emitter Cutoff Current		I_{EBO}	–	–	100	nAdc
(V_{BE} = 10 Vdc, I_C = 0)						
ON CHARACTERISTICS (1)						
DC Current Gain		h_{FE}				–
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)	MPS-A63		5000	–	–	
	MPS-A64		10,000	–	–	
	MPS-A62		20,000	–	–	
(I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	MPS-A63		10,000	–	–	
	MPS-A64		20,000	–	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 10 mAdc, I_B = 0.01 mAdc)	MPS-A62		–	–	1.0	
(I_C = 100 mAdc, I_B = 0.1 mAdc)	MPS-A63, MPS-A64		–	0.8	1.5	
Base-Emitter On Voltage		$V_{BE(on)}$				Vdc
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)	MPS-A62		–	–	1.4	
(I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	MPS-A63, MPS-A64		–	1.25	2.0	
SMALL-SIGNAL CHARACTERISTICS						
Current-Gain—Bandwidth Product (2)		f_T	125	–	–	MHz
(I_C = 100 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	MPS-A63, MPS-A64					
Output Capacitance		C_{ob}	–	4.0	–	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	MPS-A63, MPS-A64					
Small-Signal Current Gain		h_{fe}	–	35 k	–	–
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)						
Noise Figure		NF	–	2.0	–	dB
(I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, R_S = 100 kΩ, f = 1.0 kHz)						

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$.

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

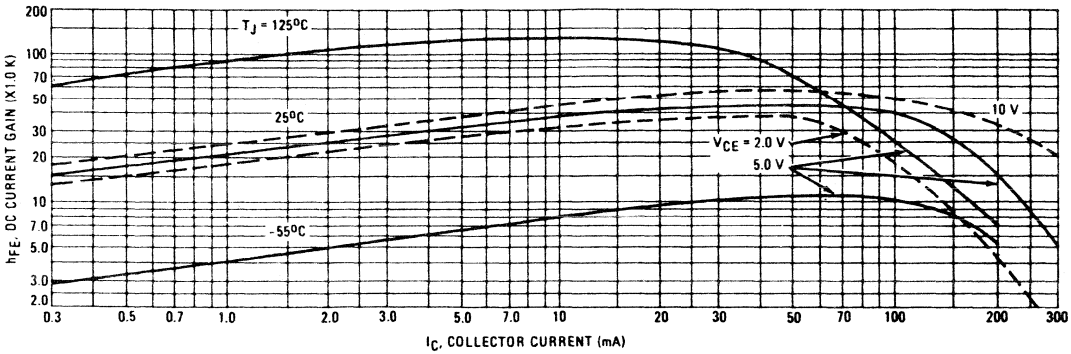


FIGURE 2 – "ON" VOLTAGE

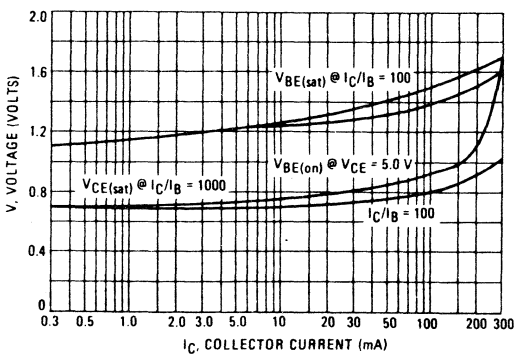


FIGURE 3 – COLLECTOR SATURATION REGION

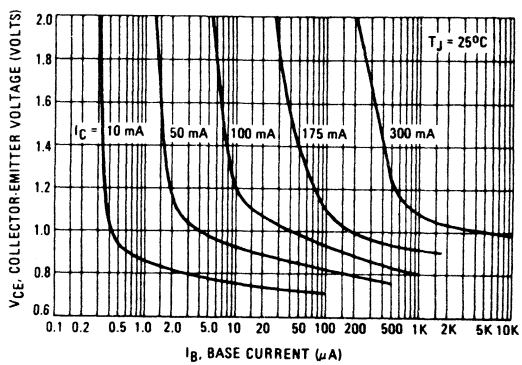


FIGURE 4 – TEMPERATURE COEFFICIENTS

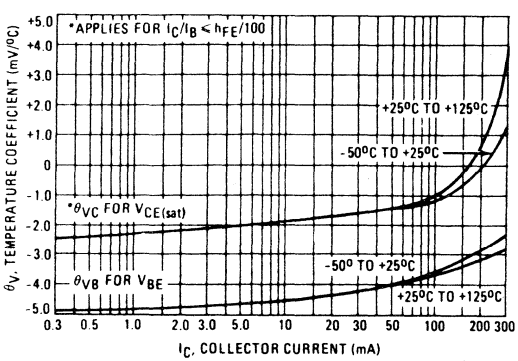
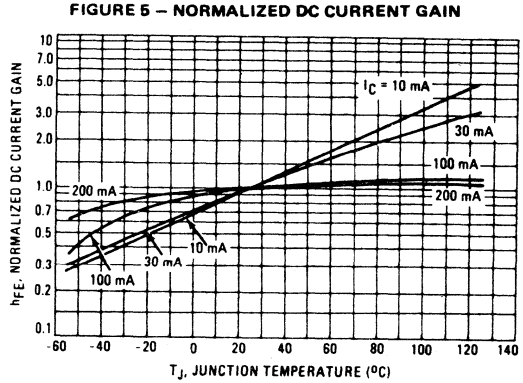


FIGURE 5 – NORMALIZED DC CURRENT GAIN



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TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 6 – CURRENT-GAIN–BANDWIDTH PRODUCT

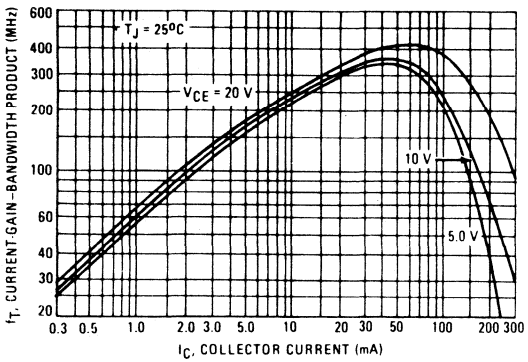


FIGURE 7 – CAPACITANCE

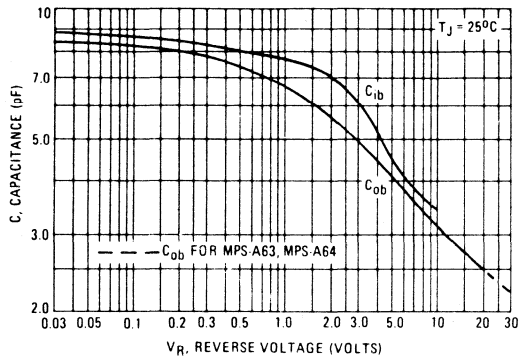


FIGURE 8 – ACTIVE-REGION SAFE OPERATING AREA

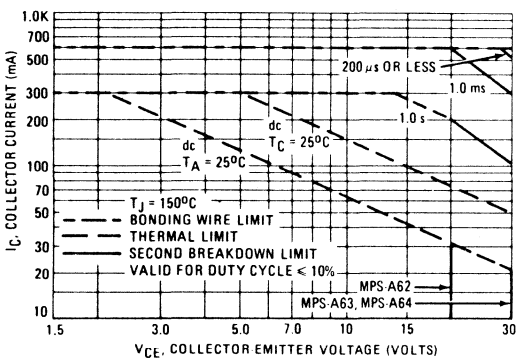


FIGURE 9 – WIDE-BAND NOISE FIGURE

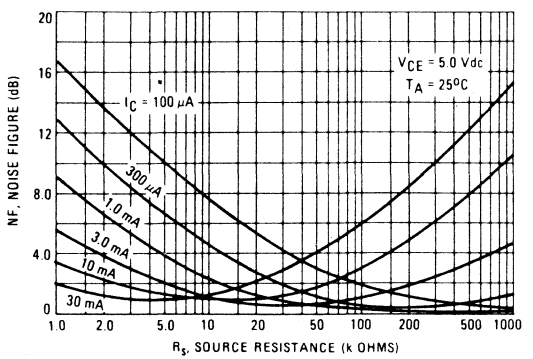


FIGURE 10 – NOISE FIGURE versus SOURCE RESISTANCE – 100 Hz

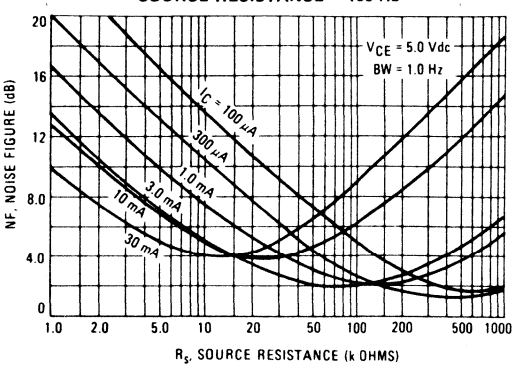
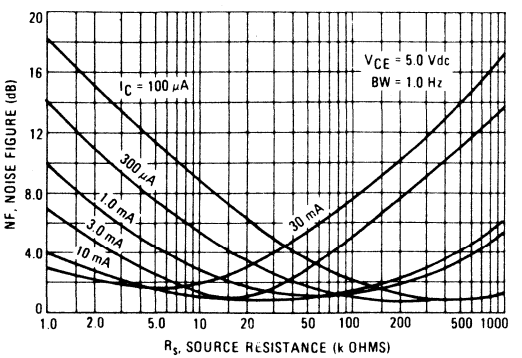


FIGURE 11 – NOISE FIGURE versus SOURCE RESISTANCE – 1000 Hz

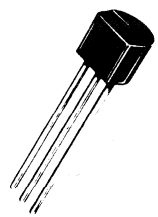


NPN SILICON ANNULAR♦ TRANSISTOR

. . . designed for general-purpose, high-voltage amplifier applications.

- High Breakdown Voltages –
  BV_{CEO} = 120 Vdc (Min), BV_{CBO} = 140 Vdc (Min)
- Low Saturation Voltage
  $V_{CE(sat)}$ = 0.30 V (Max) @ I_C = 50 mA

HIGH VOLTAGE
NPN SILICON AMPLIFIER TRANSISTOR



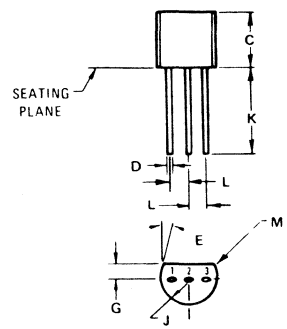
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	120	Vdc
Collector-Base Voltage	V_{CB}	140	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous	I_C	150	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient (1)	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
C	4.450	4.700	0.175	0.185
D	0.407	0.482	0.016	0.019
E	5° NOM		5° NOM	
G	1.150	1.390	0.045	0.055
J	2.160	2.420	0.085	0.095
K	12.700	–	0.500	–
L	1.270 TP		0.050 TP	
M	0.076	0.330	0.003	0.013

CASE 29-01

♦Annular Semiconductors Patented by Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	120	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	140	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	5.0	–	Vdc
Collector Cutoff Current (V_{CB} = 75 Vdc, I_E = 0)	I_{CBO}	–	1.0	μAdc
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	100	nAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 10 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	50	300	–
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{CE(sat)}$	–	0.20	Vdc
(I_C = 50 mAdc, I_B = 5.0 mAdc)		–	0.30	
Base-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{BE(sat)}$	–	1.2	Vdc
(I_C = 50 mAdc, I_B = 5.0 mAdc) (1)		–	1.4	
DYNAMIC CHARACTERISTICS				
Current-Gain–Bandwidth Product (1) (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	60	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	8.0	pF
Small-Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	30	–	–

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

FIGURE 1 – THERMAL RESPONSE

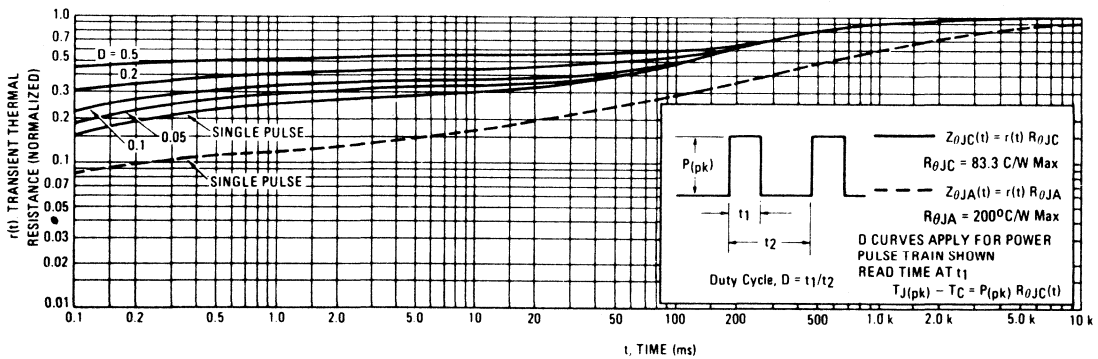


FIGURE 2 – DC CURRENT GAIN

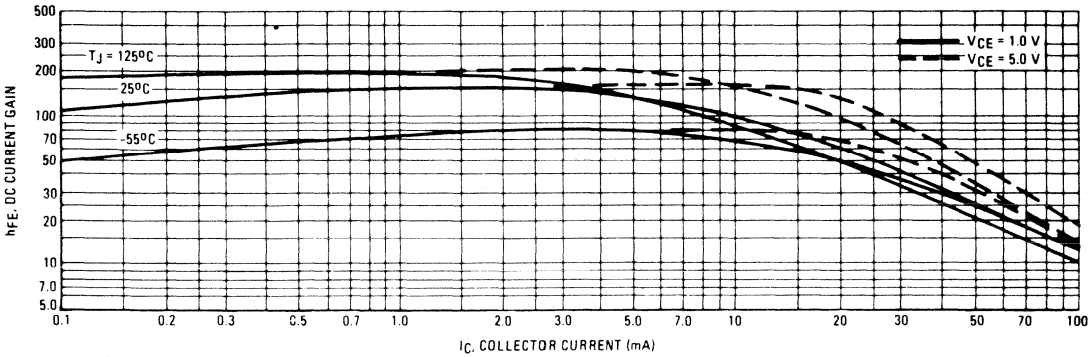


FIGURE 3 – COLLECTOR SATURATION REGION

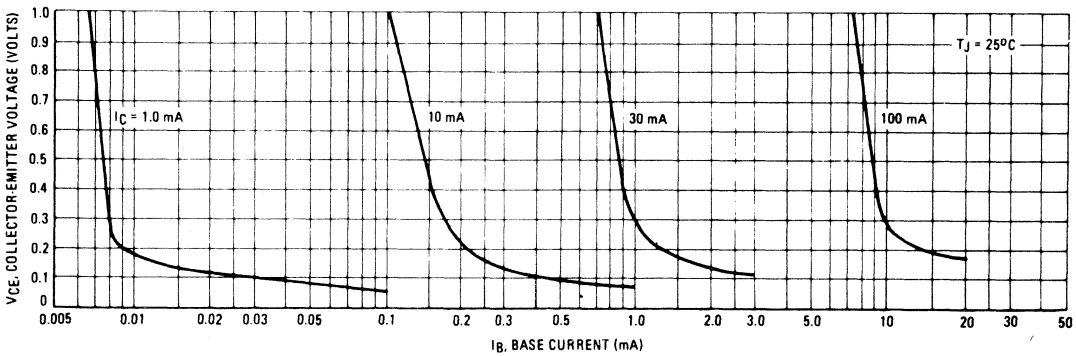
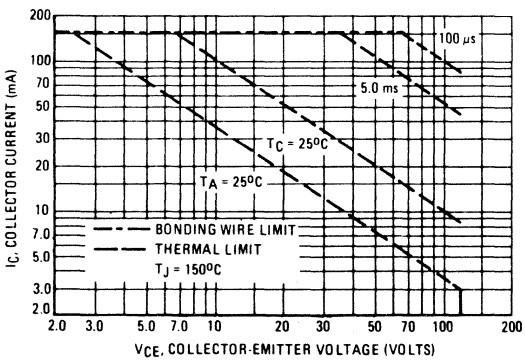


FIGURE 4 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)}$ = 150°C T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

4

FIGURE 5 – "ON" VOLTAGES

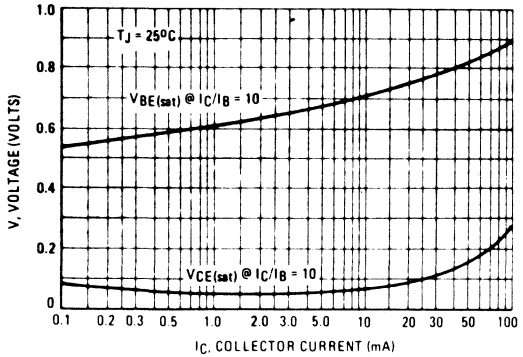


FIGURE 6 – TEMPERATURE COEFFICIENTS

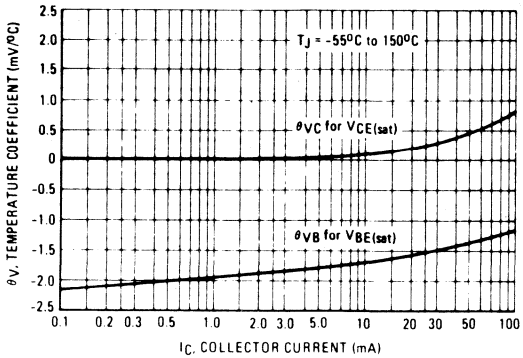


FIGURE 7 – SWITCHING TIME TEST CIRCUIT

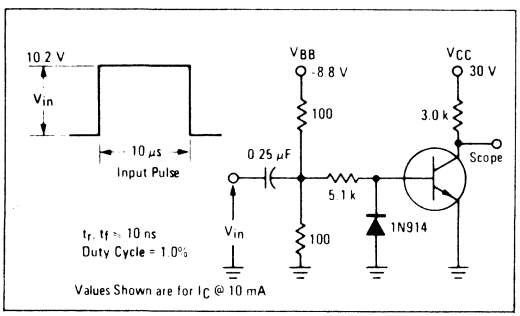


FIGURE 8 – CAPACITANCES

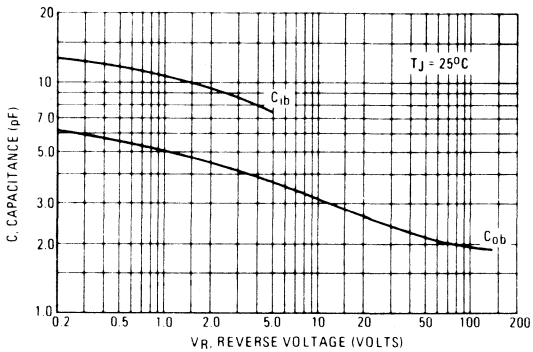


FIGURE 9 – TURN-ON TIME

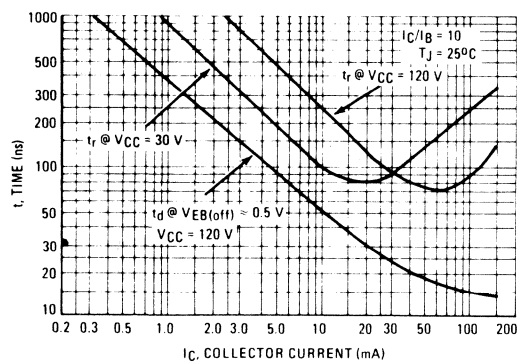
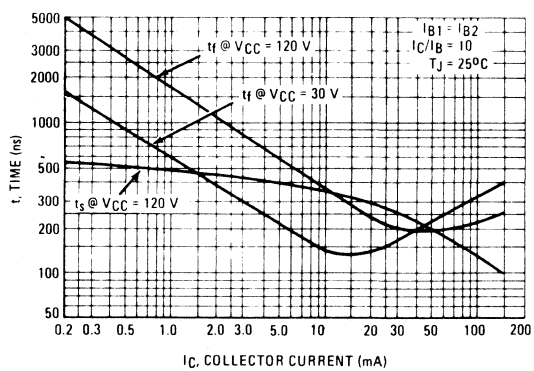


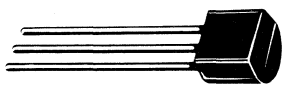
FIGURE 10 – TURN-OFF TIME



SECTION 5
FIELD EFFECT TRANSISTORS

— Metal and plastic encapsulated transistors for general purpose, switching and RF applications.

Section 5—Packages



TO 92

TO 72

5

5 FIELD EFFECT TRANSISTORS

General Purpose Transistors

Device	Designation	$\lvert Y_{fs}\rvert$ Min. mmho	$\lvert Y_{fs}\rvert$ Max. mmho	$V_{GS(off)}$ Min. V	$V_{GS(off)}$ Max. V	NF Max. dB	C_{RSS} Max. pF	BV_{GSS} Min. V	Technology	Package	Page
BF245	Wide Frequency Range from DC-VHF	3	6.5	0.4	7.5	1.5	1.1	30	N-ch. J	TO-92	5-3
MPF102	Amplifier and Mixers	2	7.5	–	8	–	3	25	N-ch. J	TO-92	5-23
2N4117	Low Input Current DC Amplifier	0.07	0.21	0.6	1.8	–	1.5	40	N-ch. J	TO-72	5-28
2N4118		0.08	0.25	1	3	–	1.5	40	N-ch. J	TO-72	5-28
2N4119		0.10	0.33	2	6	–	1.5	40	N-ch. J	TO-72	5-28
2N5457	Audio and Switching	1	5	0.5	6	–	3	25	N-ch. J	TO-92	5-44
2N5458		1.5	5.5	1	7	–	3	25	N-ch. J	TO-92	5-44
2N5459		2	6	2	8	–	3	25	N-ch. J	TO-92	5-44
2N5460	Amplifier Applications	1	4	0.75	6.0	2.5	2	40	P-ch. J	TO-92	5-45
2N5461		1.5	5	1.0	7.5	2.5	2	40	P-ch. J	TO-92	5-45
2N5462		2	6	1.8	9.0	2.5	2	40	P-ch. J	TO-92	5-45
2N5463		1	4	0.75	6.0	2.5	2	60	P-ch. J	TO-92	5-45
2N5464		1.5	5	1.0	7.5	2.5	2	60	P-ch. J	TO-92	5-45
2N5465		2	6	1.8	9	2.5	2	60	P-ch. J	TO-92	5-45

Switching Transistors

Device	Designation	$r_{DS(on)}$ Max. Ω	$V_{GS(off)}$ Min. V	$V_{GS(off)}$ Max. V	$I_{D(off)}$ Max. nA	I_{DSS} Min. mA	I_{DSS} Max. mA	C_{RSS} Max. pF	BV_{GSS} Min. V	Technology	Package	Page
MPF4391	Chopper and H Speed Switching	30	4	10	1	60	130	3.5	30	N-ch. J	TO-92	5-24
MPF4392		60	2	5	1	25	75	3.5	30	N-ch. J	TO-92	5-24
MPF4993		100	0.5	3	1	5	30	3.5	30	N-ch. J	TO-92	5-24
2N4351	Enhancement Mode, Low Power	300	1	5	10	3	–	1.3	25	N-ch. MOS	TO-72	5-30
2N4352		600	1	5	10	3	–	1.3	25	P-ch. MOS	TO-72	5-34
2N5457	Audio and Switching	–	0.5	6	–	1	5	3	25	N-ch. J	TO-92	5-44
2N5458		–	1	7	–	2	9	3	25	N-ch. J	TO-92	5-44
2N5459		–	2	8	–	4	16	3	25	N-ch. J	TO-92	5-44
2N5638	Chopper and H Speed Switching	30	–	12	1	50	–	4	30	N-ch. J	TO-92	5-50
2N5639		60	–	8	1	25	–	4	30	N-ch. J	TO-92	5-50
2N5640		100	–	6	1	5	–	4	30	N-ch. J	TO-92	5-50

High Frequency Transistors

Device	Designation	$\lvert Y_{fs}\rvert$ Min. mmho	$\lvert Y_{fs}\rvert$ Max. mmho	C_{RSS} Max. pF	NF Max. dB	@ F MHz	Technology	Package	Page
BF245	Wide Frequency Range to VHF	3	6.5	1.1	1.5	100	N-ch. J	TO-92	5-3
BF256	VHF/UHF Applications	4.5	–	0.7 (typ)	7.5 (typ)	800	N-ch. J	TO-92	5-7
J308	VHF/UHF Amplifier and Mixer	–	20	2.5	1.5 (typ)	100	N-ch. J	TO-92	5-11
J309		–	20	2.5	1.5 (typ)	100	N-ch. J	TO-92	5-11
J310		–	18	2.5	1.5 (typ)	100	N-ch. J	TO-92	5-11
MFE140	Dual Gate, FM Amplifiers and Mixers	10	20	0.05	3.5	100	N-ch. MOS	TO-72	5-17
MPF102	VHF Amplifiers and Mixers	1.6	–	3	–	–	N-ch. J	TO-92	5-23
2N4416	VHF/UHF Amplifiers	4.5	7.5	0.8	4	400	N-ch. J	TO-72	5-38
2N5484	VHF/UHF Amplifiers	3	6	1	3	100	N-ch. J	TO-92	5-48
2N5485		3.5	7	1	2	100	N-ch. J	TO-92	5-48
2N5486		4	8	1	4	400	N-ch. J	TO-92	5-48
3N201	Dual Gate, VHF Amplifiers and Mixers	8	20	0.03	4.5	200	N-ch. MOS	TO-72	5-52
3N202		8	20	0.03	–	–	N-ch. MOS	TO-72	5-52
3N203		7	15	0.03	6	45	N-ch. MOS	TO-72	5-52
3N211	Dual Gate, VHF Amplifiers and Mixers	17	40	0.05	4	45	N-ch. MOS	TO-72	5-58
3N212		17	40	0.05	–	–	N-ch. MOS	TO-72	5-58
3N213		15	35	0.05	4	45	N-ch. MOS	TO-72	5-58

BF245 • BF245A
BF245B • BF245C

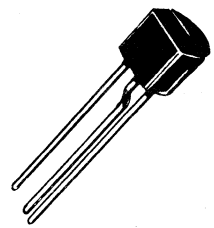
SILICON N-CHANNEL
JUNCTION FIELD-EFFECT TRANSISTOR

. . . designed for a wide range of fequency Applications from DC to VHF.

- Low cost TO-92 type package
- High forward transfer admittance, $|Y_{fs}| = 3$ mmhos (min.)
- Low transfer capacitance, $C_{rss} = 3$ pF (typ.)
- Low input capacitance, $C_{iss} = 0.7$ pF (typ.)
- Three I_{dss} subgroups available:
  BF245 A: $I_{dss} = 2$ mA to 6.5 mA
  BF245 B: $I_{dss} = 6$ mA to 15 mA
  BF245 C: $I_{dss} = 12$ mA to 25 mA

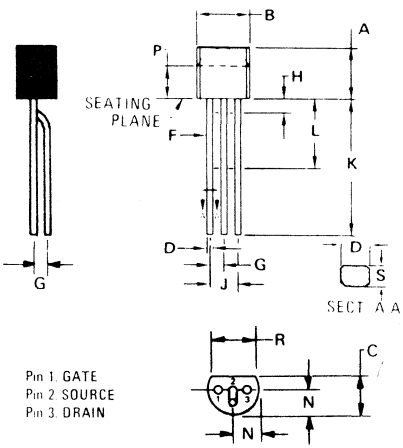
N-CHANNEL
JUNCTION FIELD-EFFECT
TRANSISTORS

(TYPE A)



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-source Voltage	V_{DS}	30	Vdc
Drain-Gate Voltage	V_{DG}	30	Vdc
Gate-Source Voltage	V_{GS}	30	Vdc
Forward Gate Current	$I_{G(f)}$	10	mAdc
Total Device Dissipation @ $T_A = 25$ °C Derate above 25 °C	P_D	360 2.88	mW mW/°C
Operating and Storage Channel Temperature Range	$T_{channel}$, T_{stg}	65 to +150	°C



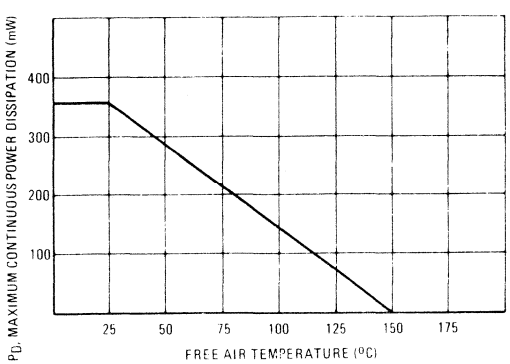
Pin 1. GATE
Pin 2. SOURCE
Pin 3. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

(TO-18 Pin configuration)

FIGURE 1 – POWER DERATING CURVE



5

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage ($-I_G$ = 1.0 μAdc, V_{DS} = 0)		$-V_{(BR)GSS}$	30	–	–	Vdc
Gate-Source Voltage (V_{DS} = 15 Vdc, I_D = 200 μA)	BF245[2]	$-V_{GS}$	0.4	–	7.5	Vdc
	BF245A		0.4	–	2.2	
	BF245B		1.6	–	3.8	
	BF245C		3.2	–	7.5	
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 10 nA)		$-V_{GS(Off)}$	0.5	–	8	Vdc
Gate Reverse Current ($-V_{GS}$ = 20 Vdc, V_{DS} = 0)		$-I_{GSS}$	–	–	5	nAdc
ON CHARACTERISTICS						
Zero-Gate Voltage Drain Current[1] (V_{DS} = 15 Vdc, V_{GS} = 0)	BF245[2]	I_{DSS}	2		25	mAdc
	BF245A		2		6.5	
	BF245B		6		15	
	BF245C		12		25	
SMALL SIGNAL CHARACTERISTICS						
Forward Transfer Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 KHz))		$\|Y_{fs}\|$	3.0		6.5	mmhos
Output Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 KHz)		$\|Y_{os}\|$		40		μmhos
Forward Transfer Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 200 MHz)		$\|Y_{fs}\|$		5.6		mmhos
Reverse Transfer Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 200 MHz)		$\|Y_{rs}\|$		1.0		mmhos
Input Capacitance (V_{DS} = 20 Vdc, $-V_{GS}$ = 1 Vdc)		C_{iss}		3		pf
Reverse Transfer Capacitance (V_{DS} = 20 Vdc, $-V_{GS}$ = 1 Vdc, f = 1 MHz)		C_{Rss}		0.7		pf
Output Capacitance (V_{DS} = 20 Vdc, $-V_{GS}$ = 1 Vdc, f = 1 MHz)		C_{oss}		0.9		pf
Noise Figure (V_{DS} = 15 Vdc, V_{GS} = 0, R_G = 1 KΩ, f = 100 MHz)		N_F		1.5		db
Cut-off Frequency[3] (V_{DS} = 15 Vdc, V_{GS} = 0)		f_{gfs}		700		MHz

[1] Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.
[2] On orders against the BF245, any or all subgroups might be shipped.
[3] The frequency at which gfs is 0.7 of its value at 1 KHz.

TYPICAL CHARACTERISTICS

FIGURE 2 – CORRELATION BETWEEN $-V_{GS(off)}$ AND I_{DSS}

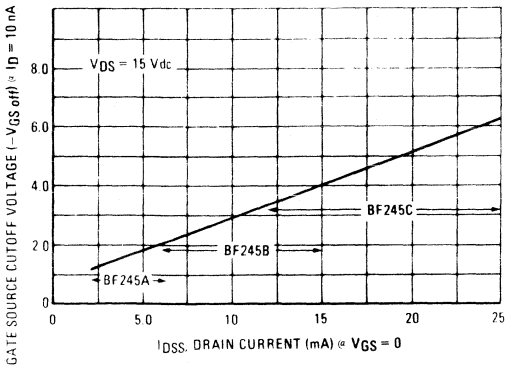


FIGURE 3 – DRAIN CURRENT VERSUS DRAIN TO SOURCE VOLTAGE

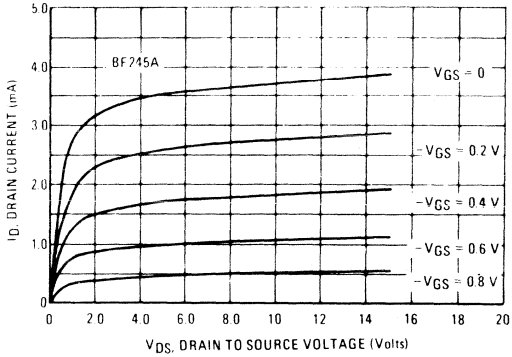
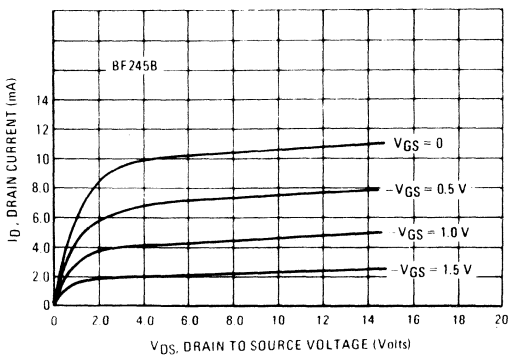


FIGURE 4 – DRAIN CURRENT VERSUS DRAIN TO SOURCE VOLTAGE



FIGUR 5 – DRAIN CURRENT VERSUS DRAIN TO SOURCE VOLTAGE

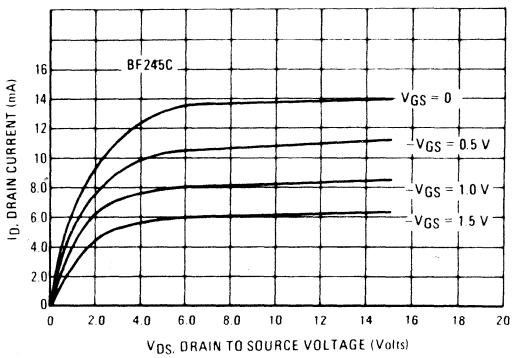


FIGURE 6 – INPUT ADMITTANCE VERSUS FREQUENCY

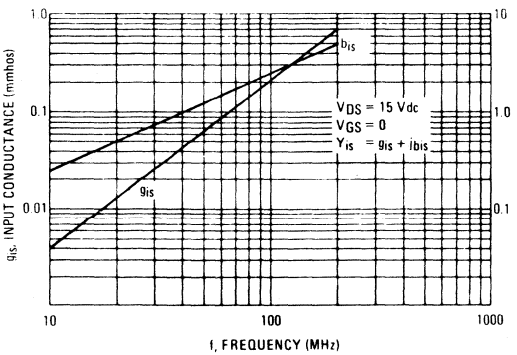
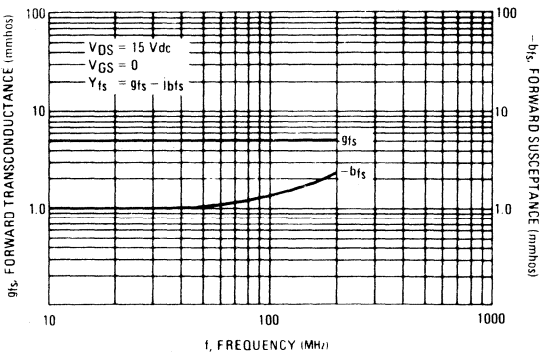


FIGURE 7 – FORWARD TRANSFER ADMITTANCE VERSUS FREQUENCY



5

TYPICAL CHARACTERISTICS

FIGURE 8 – REVERSE TRANSFER ADMITTANCE VERSUS FREQUENCY

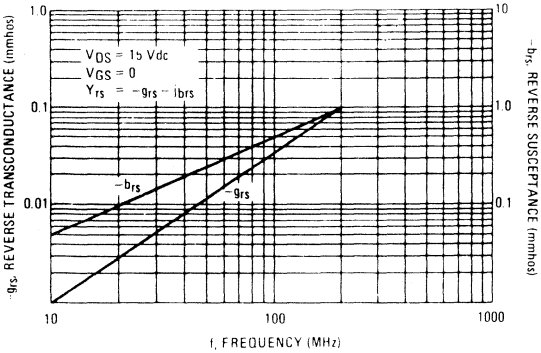


FIGURE 9 – OUTPUT ADMITTANCE VERSUS FREQUENCY

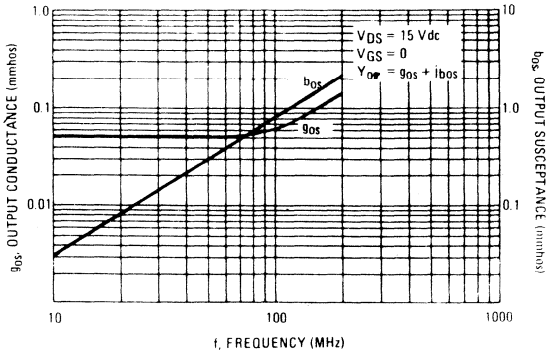


FIGURE 10 – INPUT CAPACITANCE VERSUS GATE-SOURCE VOLTAHE

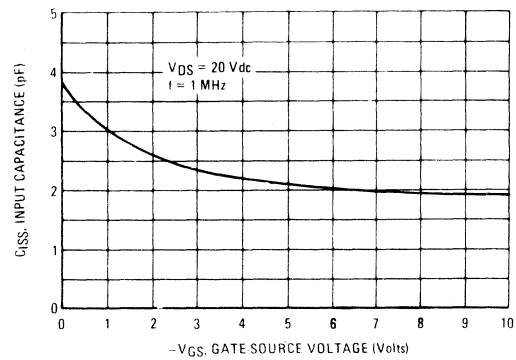
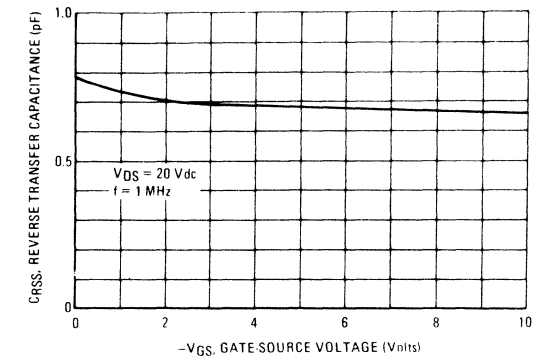


FIGURE 11 – REVERSE TRANSFER CAPACITANCE VERSUS GATE-SOURCE VOLTAGE



BF256 • BF256A
BF256B • BF256C

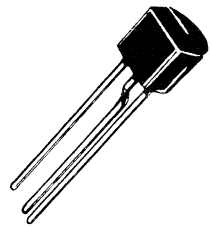
SILICON N-CHANNEL
JUNCTION FIELD-EFFECT TRANSISTOR

. . . designed for VHF and UHF Applications.

- Low cost TO-92 type package
- Forward transfer admittance, Y_{fs} = 4,5 mmhos (min.)
- Transfer capacitance, C_{rss} = 0,7 (typ.)
- Power gain at f = 800 MHz, typ. = 11dB
- Three I_{dss} subgroups available:
  BF256A : I_{dss} = 3 mA to 7 mA
  BF256B : I_{dss} = 6 mA to 13 mA
  BF256C : I_{dss} = 11 mA to 18 mA

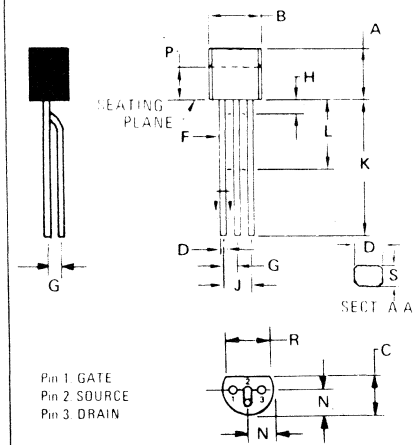
N-CHANNEL
JUNCTION FIELD-EFFECT
TRANSISTORS

(TYPE A)



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-source Voltage	V_{DS}	30	Vdc
Drain-Gate Voltage	V_{DG}	30	Vdc
Gate-Source Voltage	V_{GS}	30	Vdc
Forward Gate Current	$I_{G(f)}$	10	mAdc
Total Device Dissipation @ T_A = 25 °C Derate above 25 °C	P_D	360 2 88	mW mW/°C
Operating and Storage Channel Temperature Range	$T_{channel}$, T_{stg}	−65 to +150	°C

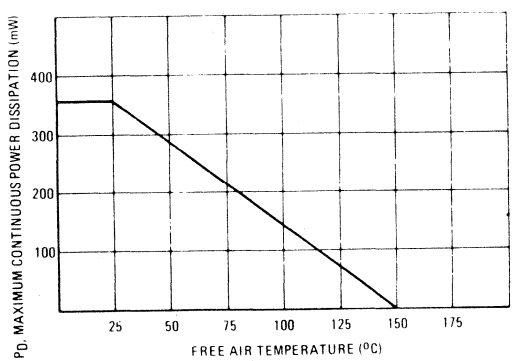


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4 32	5 33	0 170	0 210
B	4 44	5 21	0 175	0 205
C	3 18	4 19	0 125	0 165
D	0 41	0 56	0 016	0 022
F	0 41	0 48	0 016	0 019
G	1 14	1 40	0 045	0 055
H		2 54		0 100
J	2 41	2 67	0 095	0 105
K	12 70		0 500	
L	6 35		0 250	
N	2 03	2 92	0 080	0 115
P	2 92		0 115	
R	3 43		0 135	
S	0 36	0 41	0 014	0 016

All JEDEC dimensions and notes apply

(TO-18 Pin configuration)

FIGURE 1 – POWER DERATING CURVE



5

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage ($-I_G$ = 1.0 μAdc, V_{DS} = 0)		$-V_{(BR)GSS}$	30	--	–	Vdc
Gate-Source Voltage (V_{DS} = 15 Vdc, I_D = 200 μA)		$-V_{GS}$	0.5	–	7.5	Vdc
Gate Reverse Current ($-V_{GS}$ = 20 Vdc, V_{DS} = 0)		$-I_{GSS}$	–	--	5	nAdc
ON CHARACTERISTICS						
Zero-Gate Voltage Drain Current[1] (V_{DS} = 15 Vdc, V_{GS} = 0)	BF256[2]	I_{DSS}	3	–	18	mAdc
	BF256A		3	–	7	
	BF256B		6	–	13	
	BF256C		11	–	18	
SMALL SIGNAL CHARACTERISTICS						
Forward Transfer Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 KHz)		$\|Y_{fs}\|$	4.5	5	–	mmhos
Reverse Transfer Capacitance (V_{DS} = 20 Vdc, $-V_{GS}$ = 1 Vdc, f = 1 MHz)		C_{rss}	–	0.7	–	pf
Output Capacitance (V_{DS} = 20 Vdc, V_{GS} = 0, f = 1 MHz)		C_{oss}	–	1.0	–	pf
Noise Figure (V_{DS} = 10 Vdc, Rs = 47 Ω, f = 800 MHz)		N_F	–	7.5	–	db
Cut-off Frequency[3] (V_{DS} = 15 Vdc, V_{GS} = 0)		f_{gfs}	–	1000	–	MHz
Power Gain (V_{DS} = 15 Vdc, Rs = 47 Ω, f = 800 MHz)		Gp	–	11	–	dB

1 Pulse Test: Pluse Width = 300 μs, Duty Cycle = 2.0%

2 On orders against the BF256, any or all subgroups might be shipped

3 The frequency at which gfs is 0.7 of its value at 1 KHz

TYPICAL CHARACTERISTICS

FIGURE 2 – CORRELATION BETWEEN $-V_{GS(off)}$ AND I_{DSS}

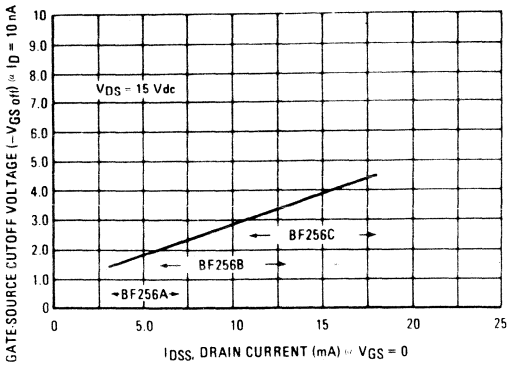


FIGURE 3 – DRAIN CURRENT VERSUS DRAIN TO SOURCE VOLTAGE

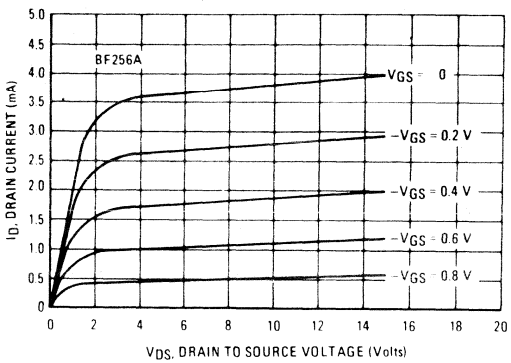


FIGURE 4 – DRAIN CURRENT VERSUS DRAIN TO SOURCE VOLTAGE

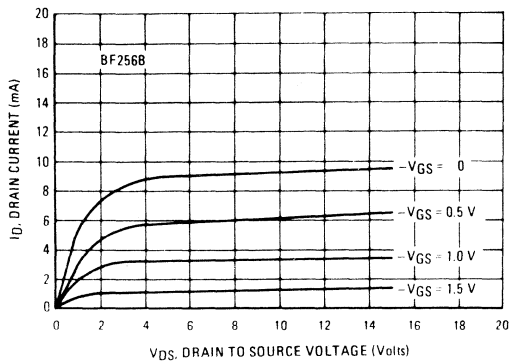


FIGURE 5 – DRAIN CURRENT VERSUS DRAIN TO SOURCE VOLTAGE

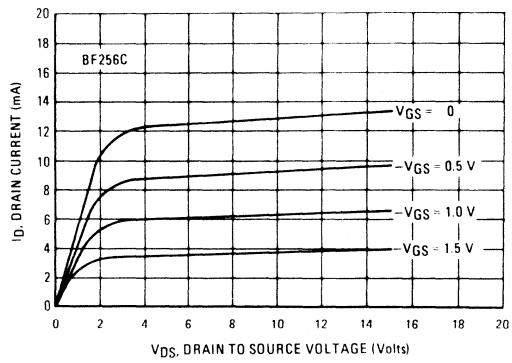


FIGURE 6 – INPUT ADMITTANCE VERSUS FREQUENCY

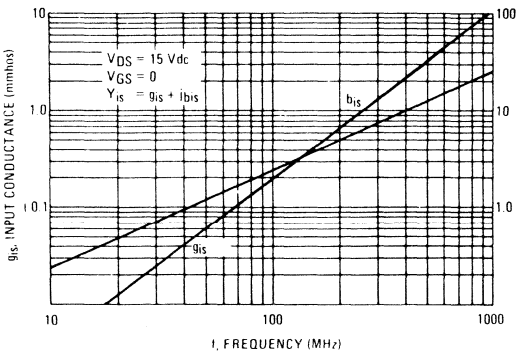
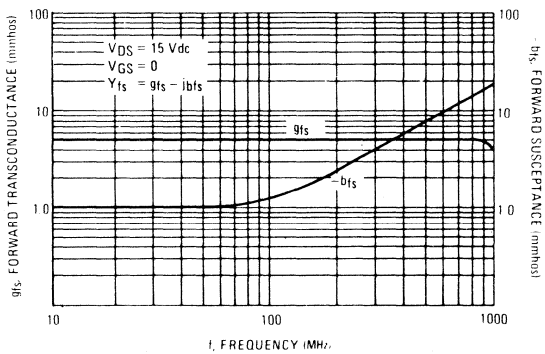


FIGURE 7 – FORWARD TRANSFER ADMITTANCE VERSUS FREQUENCY



5

TYPICAL CHARACTERISTICS

FIGURE 8 – REVERSE TRANSFER ADMITTANCE VERSUS FREQUENCY

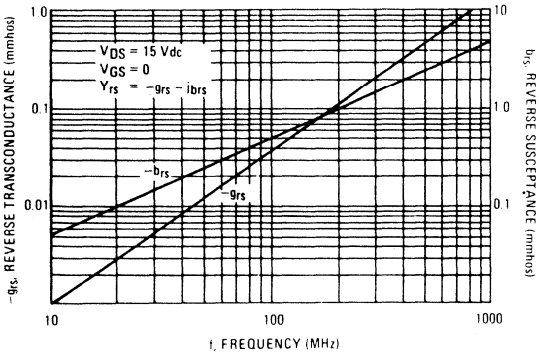


FIGURE 9 – OUTPUT ADMITTANCE VERSUS FREQUENCY

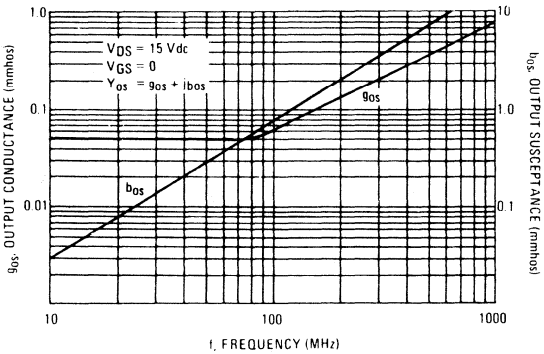


FIGURE 10 – INPUT CAPACITANCE VERSUS GATE-SOURCE VOLTAGE

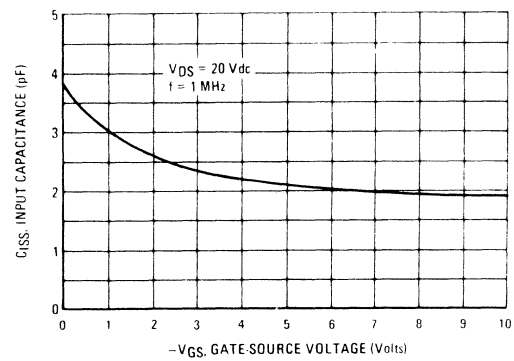
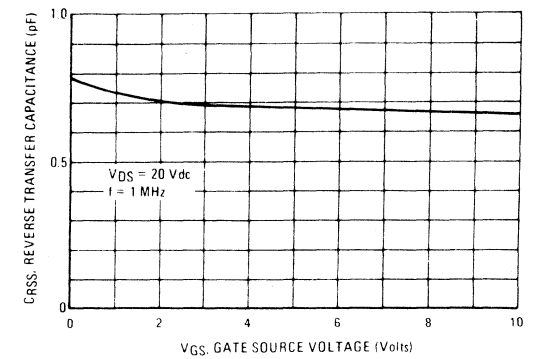


FIGURE 11 – REVERSE TRANSFER CAPACITANCE VERSUS GATE-SOURCE VOLTAGE



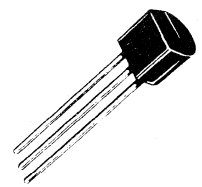
J308
J309 • J310

SILICON N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS

. . . designed for VHF/UHF amplifier, mixer and oscillator applications.

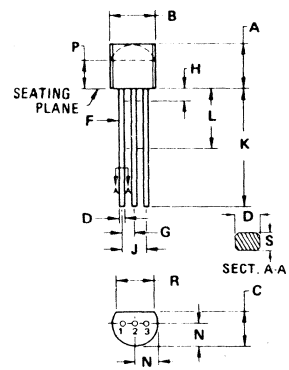
- High Power Gain –
  G_{pg} = 16 dB (Typ) @ f = 100 MHz
- Low Noise Figure –
  NF = 1.5 dB (Typ) @ 100 MHz
- High Forward Transfer Admittance
  $|g_{fs}|$ 8–20 mmhos – J308
  10–20 mmhos – J309
  8–18 mmhos – J310

SILICON N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Gate Voltage	V_{DG}	25	Vdc
Gate-Source Voltage	V_{GS}	25	Vdc
Forward Gate Current	I_{GF}	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 3.5	mW mW/°C
Junction Temperature Range	T_J	-55 to +125	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

CASE 29-02
TO-92

5

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Gate-Source Breakdown Voltage (I_G = -1.0 μA, V_{DS} = 0)	BV_{GSS}	-25	–	–	Vdc
Gate Reverse Current	I_{GSS}				
(V_{GS} = -15 V, V_{DS} = 0, T_A = 25°C)		–	–	-1.0	nA
(V_{GS} = -15 V, V_{DS} = 0, T_A = +125°C)		–	–	-1.0	μA
Gate-Source Cutoff Voltage	$V_{GS(off)}$				Vdc
(V_{DS} = 10 V, I_D = 1.0 nA) J308		-1.0	–	-6.5	
J309		-1.0	–	-4.0	
J310		-2.0	–	-6.5	
ON CHARACTERISTICS					
Saturation Drain Current (1)	I_{DSS}				mA
(V_{DS} = 10 V, V_{GS} = 0) J308		12	–	60	
J309		12	–	30	
J310		24	–	60	
Gate-Source Forward Voltage (V_{DS} = 0, I_G = 1.0 mA)	$V_{GS(f)}$	–	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Common-Source Forward Transconductance	g_{fs}				μmhos
(V_{DS} = 10 V, I_D = 10 mA, f = 1.0 kHz)					
J308		8,000	–	20,000	
J309		10,000	–	20,000	
J310		8,000	–	18,000	
Common-Source Output Conductance	g_{os}				μmhos
(V_{DS} = 10 V, I_D = 10 mA, f = 1.0 kHz)					
J308		–	–	200	
J309		–	–	150	
J310		–	–	200	
Common-Gate Forward Transconductance	g_{fg}				μmhos
(V_{DS} = 10 V, I_D = 10 mA, f = 1.0 kHz)					
J308		–	13,000	–	
J309		–	13,000	–	
J310		–	12,000	–	
Common-Gate Output Conductance	g_{og}				μmhos
(V_{DS} = 10 V, I_D = 10 mA, f = 1.0 kHz)					
J308		–	150	–	
J309		–	100	–	
J310		–	150	–	
Gate-Drain Capacitance (V_{DS} = 0, V_{GS} = -10 V, f = 1.0 MHz)	C_{gd}	–	1.8	2.5	pF
Gate-Source Capacitance (V_{DS} = 0, V_{GS} = -10 V, f = 1.0 MHz)	C_{gs}	–	4.3	5.0	pF
Equivalent Short-Circuit Input Noise Voltage (V_{DS} = 10 V, I_D = 10 mA, f = 100 Hz)	$\bar{e}_n$	–	10	–	$nV/\sqrt{Hz}$
FUNCTIONAL CHARACTERISTICS					
Common-Source Forward Transconductance (V_{DS} = 10 V, I_D = 10 mA, f = 100 MHz)	$Re_{(yfs)}$	–	12	–	mmhos
Common-Gate Input Conductance (V_{DS} = 10 V, I_D = 10 mA, f = 100 MHz)	$Re_{(yig)}$	–	12	–	mmhos
Common-Source Input Conductance	$Re_{(yis)}$				mmhos
(V_{DS} = 10 V, I_D = 10 mA, f = 100 MHz)					
J308		–	0.7	–	
J309		–	0.7	–	
J310		–	0.5	–	
Common-Source Output Conductance (V_{DS} = 10 V, I_D = 10 mA, f = 100 MHz)	$Re_{(yos)}$	–	0.25	–	mmhos
Common-Gate Power Gain (V_{DS} = 10 V, I_D = 10 mA, f = 100 MHz)	G_{pg}	–	16	–	dB
Noise Figure (V_{DS} = 10 V, I_D = 10 mA)	NF	–	1.5	–	dB

Note:
(1) Pulse test PW 300 μs, duty cycle ≤ 3%.

MPF130 • MPF131 • MPF132
MFE130 • MFE131 • MFE132

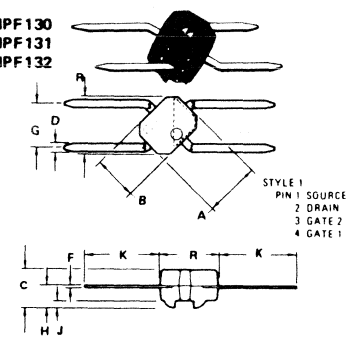
N-CHANNEL DUAL-GATE SILICON-NITRIDE PASSIVATED MOS FIELD-EFFECT TRANSISTORS

. . . depletion mode (Type B) dual gate transistors designed for VHF amplifier and mixer applications. These types are specified as follows:

- MPF130/MFE130 – RF Amplifier @ 105 MHz
  MPF131/MFE131 – RF Amplifier @ 60 and 200 MHz
  MPF132/MFE132 – Mixer @ 60 and 200 MHz
- Silicon Nitride Passivation for Excellent Long Term Stability
- Diode Protected Gates
- Supplied in Metal Can or Plastic Packages –
  MFE130 Series – TO-72
  MPF130 Series – Case 262

N-CHANNEL
DUAL GATE
MOS FIELD – EFFECT
TRANSISTORS

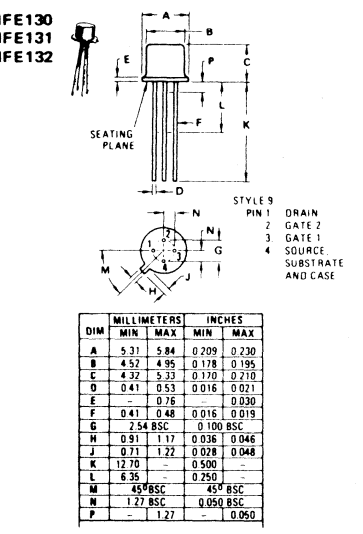
MPF130
MPF131
MPF132



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	4.95	5.21	0.195	0.205
B	3.94	4.19	0.155	0.165
C	2.67	2.92	0.105	0.115
D	0.64	0.89	0.025	0.035
F	0.20	0.30	0.008	0.012
G	4.06 BSC		0.160 BSC	
H	1.57	1.83	0.062	0.072
J	0.51	0.76	0.020	0.030
K	6.35	7.62	0.250	0.300
R	5.21	5.46	0.205	0.215

CASE 262-02

MFE130
MFE131
MFE132



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

CASE 20-03
TO-72

MAXIMUM RATINGS

Rating	Symbol	Value		Unit
Drain-Source Voltage	V_{DS}	25		Vdc
Drain Current	I_D	30		mAdc
		MPF130 Series	MFE130 Series	
Total Power Dissipation @ $T_A = 25^oC$ (Package Limitation)	P_D	350	300	mW
Derate above 25°C		2.33	1.71	mW/°C
Operating and Storage Channel Temperature Range	$T_{channel}$, T_{stg}	-65 to +175	-65 to +200	°C

5

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) Substrate Connected to Source

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (I_D = 10 μAdc, V_S = 0, V_{G1} = V_{G2} = -4.0 Vdc)	$V_{(BR)DSX}$	25	–	–	Vdc
Gate 1 – Source Breakdown Voltage (I_{G1} = ±10 μAdc, V_{G2S} = 0)	$V_{(BR)G1SO}$	±7.0	–	±20	Vdc
Gate 2 – Source Breakdown Voltage (I_{G2} = ±10 μAdc, V_{G2S} = 0)	$V_{(BR)G2SO}$	±7.0	–	±20	Vdc
Gate 1 to Source Cutoff Voltage (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 200 μAdc)	$V_{G1S(off)}$	–	–	-4.0	Vdc
Gate 2 to Source Cutoff Voltage (V_{DS} = 15 Vdc, V_{G1S} = 0, I_D = 200 μAdc)	$V_{G2S(off)}$	–	–	-4.0	Vdc
Gate 1 Reverse Leakage Current (V_{G1S} = ±6.0 Vdc, V_{G2S} = 0, V_{DS} = 0)	I_{G1SS}	–	–	20	nAdc
Gate 2 Reverse Leakage Current (V_{G2S} = ±6.0 Vdc, V_{G1S} = 0, V_{DS} = 0)	I_{G2SS}	–	–	20	nAdc
ON CHARACTERISTICS					
Zero-Gate Voltage Drain Current (V_{DS} = 15 Vdc, V_{G1S} = 0, V_{G2S} = 4.0 Vdc)	I_{DSS}	3.0	10	30	mAdc
SMALL-SIGNAL CHARACTERISTICS					
Forward Transfer Admittance (Gate 1 connected to Drain) (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 10 mAdc, f = 1.0 kHz)	Y_{fs}	8000	–	20,000	μmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = I_{DSS}, f = 1.0 MHz)	C_{iss}	–	4.5	7.0	pF
Output Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = I_{DSS}, f = 1.0 MHz)	C_{oss}	–	2.5	4.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 6.0 mAdc, f = 1.0 MHz)	C_{rss}	–	0.023	0.05	pF
Common-Source Noise Figure (Figure 7) (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 6.0 mAdc, Z_S is optimized for NF)	NF				dB
(f = 105 MHz) MPF/MFE130		–	2.9	5.0	
(f = 60 MHz) MPF/MFE131		–	2.5	5.0	
(f = 200 MHz) MPF/MFE131		–	3.0	5.0	
Common-Source Power Gain (Figure 7) (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 6.0 mAdc, Z_S is optimized for NF)	G_{ps}				dB
(f = 105 MHz) MPF/MFE130		17	23	–	
(f = 60 MHz) MPF/MFE131		20	27	–	
(f = 200 MHz) MPF/MFE131		17	20	–	
Level of Unwanted Signal for 1.0% Cross Modulation (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 6.0 mAdc)	–	–	100	–	mV
Common-Source Conversion Power Gain (Gate 1 Injection, Figure 8). (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, Local Oscillator Voltage = 925 mVrms)	G_c				dB
(Signal Frequency = 60 MHz, Local Oscillator Frequency = 104 MHz) MPF/MFE132		15	16.5	–	
(Signal Frequency = 200 MHz, Local Oscillator Frequency = 244 MHz) MPF/MFE132		12	14	–	

COMMON-SOURCE ADMITTANCE PARAMETERS

(V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 6.0 mAdc)

FIGURE 1 – INPUT ADMITTANCE

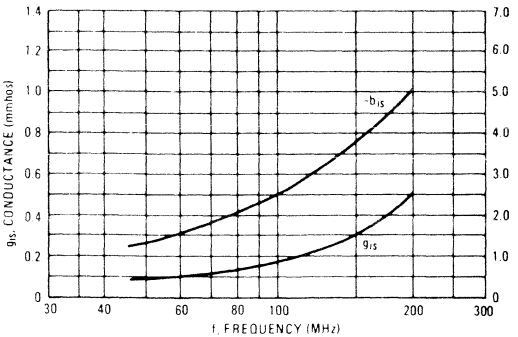


FIGURE 2 – REVERSE TRANSFER ADMITTANCE

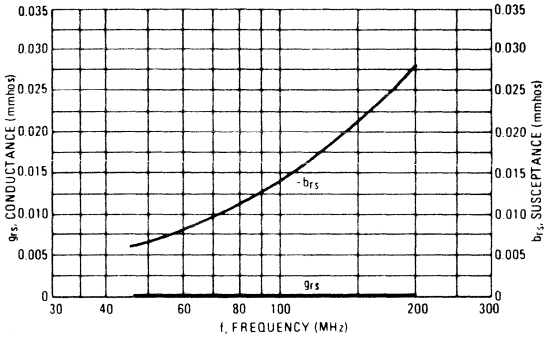


FIGURE 3 – FORWARD TRANSFER ADMITTANCE

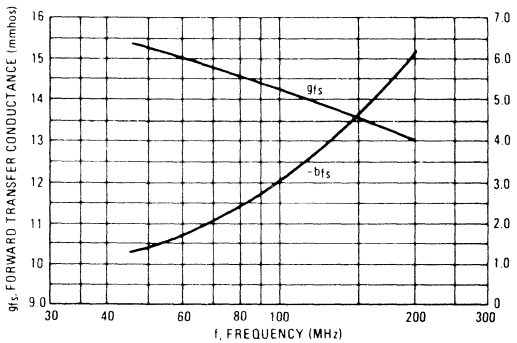


FIGURE 4 – OUTPUT ADMITTANCE

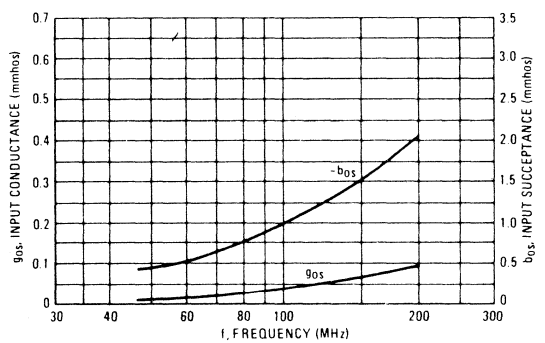


FIGURE 5 – GAIN REDUCTION

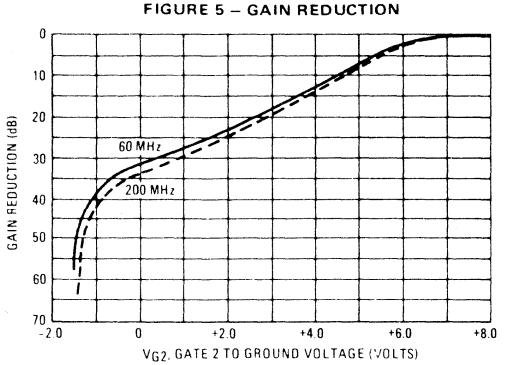


FIGURE 6 – CONVERSION POWER GAIN

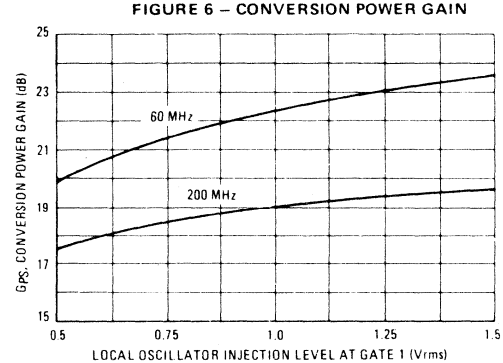


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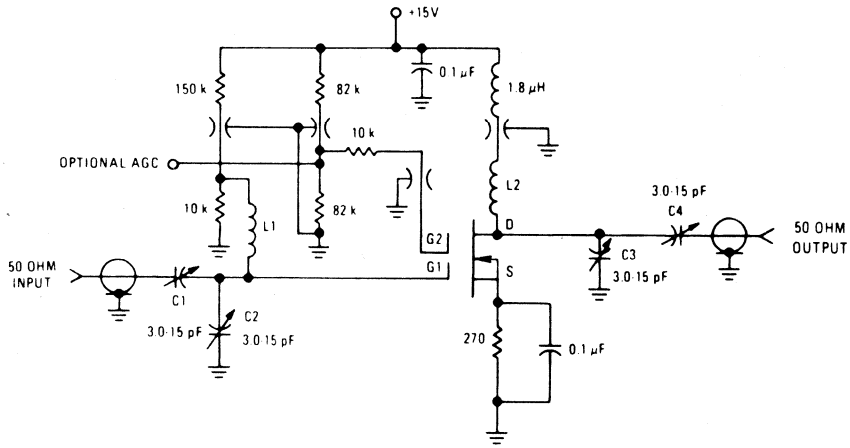
FIGURE 7 – 60, 105 AND 200 MHz POWER GAIN AND NOISE FIGURE TEST CIRCUIT

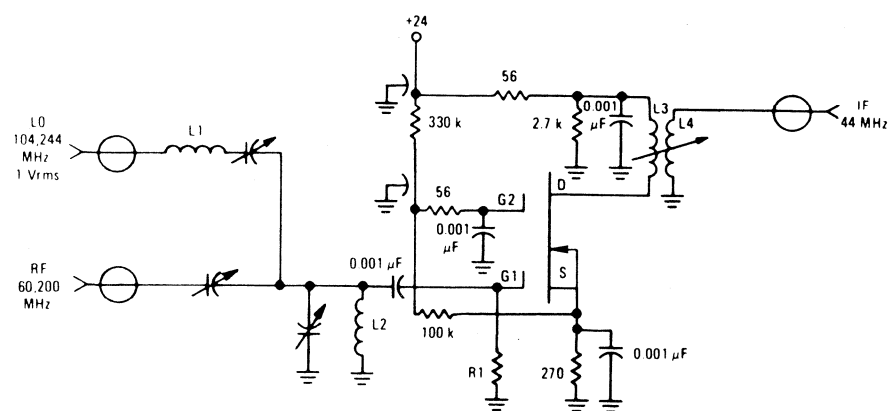


	L1	L2
60 MHz	0.33 μH	0.47 μH
105 MHz	#16 AWG, 6 1/2 Turns, 1" Long, 1/4" Dia.	#16 AWG, 5 1/4 Turns, 1" Long, 7/16" Dia.
200 MHz	#16 AWG, 3 1/2 Turns, 0.7" Long, 0.2" Dia.	#16 AWG, 4 1/2 Turns, 0.65" Long, 0.2" Dia.

All Feedthrough Capacitors 1000 pF

All Variable Capacitors JOHANSON JMC2951, 3.0-15 pF

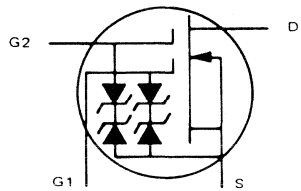
FIGURE 8 – 60 AND 200 MHz CONVERSION GAIN TEST CIRCUIT



	R1	L1	L2	L3	L4
60 MHz	10 k	10 Turns #22 Enameled on MILLER 4500-4 Core	0.33 μH DELEVAN	15 Turns #26 Enameled on MILLER 4500-1 Core	4 Turns #26 Enameled on Same Core as L3
200 MHz	1.0 k	3 1/2 Turns #18, 1/4" Dia., 1/2" Long	2 1/2 Turns #18, 3/8" Dia., 1/2" Long	15 Turns #26 Enameled on MILLER 4500-1 Core	4 Turns #26 Enameled on Same Core as L3

All Feedthrough Capacitors 1000 pF.

All Variable Capacitors JOHANSON JMC2951, 3.0-15 pF.



N-CHANNEL
DUAL GATE
MOS FIELD – EFFECT
TRANSISTOR

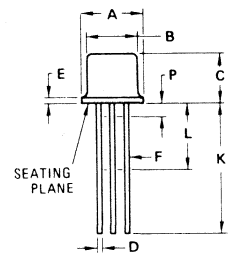
N-CHANNEL DUAL-GATE SILICON-NITRIDE PASSIVATED MOS FIELD-EFFECT TRANSISTOR

. . . depletion mode dual gate MOS FET transistor designed for FM amplifier and mixer applications.

- Silicon Nitride Passivation for Excellent Long Term Stability
- Diode Protected Gates
- Supplied in Metal Can – TO-72

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain Current	I_D	30	mAdc
Total Power Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D	300	mW
Operating and Storage Channel Temperature Range	$T_{channel}$, T_{stg}	-65 to +200	^oC
Gate Current	I_{GS}	10	mAdc
Gate-Source Voltage	V_{GS}	±7.0	Vdc



STYLE 9
PIN 1. DRAIN
2. GATE 2
3. GATE 1
4. SOURCE, SUBSTRATE AND CASE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03
TO-72

5

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted). Substrate Connected to Source

Characteristisc	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage (I_D = 10 μAdc, V_S = 0, V_{G1} = -4.0 Vdc, V_{G2} = +4.0 Vdc)	$V_{(BR)DSX}$	25	–	–	Vdc
Gate 1 – Source Breakdown Voltage (I_{G1} = ±10 μAdc, V_{G2S} = 0)	$V_{(BR)G1SO}$	±7.0	–	±20	Vdc
Gate 2 – Source Breakdown Voltage (I_{G2} = ±10 μAdc, V_{G2S} = 0)	$V_{(BR)G2S0}$	±7.0	–	±20	Vdc
Gate 1 to Source Cutoff Voltage (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 200 μAdc)	$V_{G2S(off)}$	–	–	-4.0	Vdc
Gate 2 to Source Cutoff Voltage (V_{DS} = 15 Vdc, V_{G1S} = 0, I_D = 200 μAdc)	$V_{G2S(off)}$	–	–	-4.0	Vdc
Gate 1 Reverse Leakage Current (V_{G1S} = ±6.0 Vdc, V_{G2S} = 0, V_{DS} = 0)	I_{G1SS}	–	–	20	nAdc
Gate 2 Reverse Leakage Current (V_{G2S} = ±6.0 Vdc, V_{G1S} = 0, V_{DS} = 0)	I_{G2SS}	–	–	20	nAdc
ON CHARACTERISTICS					
Zero-Gate Voltage Drain Current (V_{DS} = 15 Vdc, V_{G2S} = 0, V_{G2S} = 4.0 Vdc)	I_{DSS}	3.0	10	30	mAdc
SMALL-SIGNAL CHARACTERISTICS					
Forward Transfer Admittance (Gate 1 connected to Drain) (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 10 mAdc, f = 1.0 kHz)	$\lvert Y_{fs1}\rvert$	10	–	20	mmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = I_{DSS}, f - 1.0 MHz)	C_{iss}	–	4.5	7.0	pF
Output Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = I_{DSS}, f = 1.0 MHz)	C_{oss}	–	2.5	4.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = I_{DSS}, f = 1.0 MHz)	C_{rss}	–	0.023	0.05	pF
Common-Source Noise Figure (Figure 8) (See Test Circuit in Figure 11)	NF	–	2.5	3.5	dB
Common-Source Power Gain (Figure 7) (See Test Circuit in Figure 11)	G_{ps}	20	23	–	dB
Level of Unwanted Signal for 1.0% Cross Modulation (Figure 10) (See Test Circuit in Figure 11)	–	–	45	–	mV
Common-Source Conversion Power Gain (Gate 1 or Gate 2 Injection, Figure 12) (See Test Circuit in Figure 13) (Signal Frequency = 100 MHz, Local Oscillator Frequency = 110.7 MHz)	G_c	15	18.5	–	dB
1/2 I. F. Rejection (See Test Circuit in Figure 13)	1/2 I_{FREJ}	–	50	–	dB

COMMON-SOURCE ADMITTANCE PARAMETERS

(V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 6.0 mAdc)

FIGURE 1 – INPUT ADMITTANCE

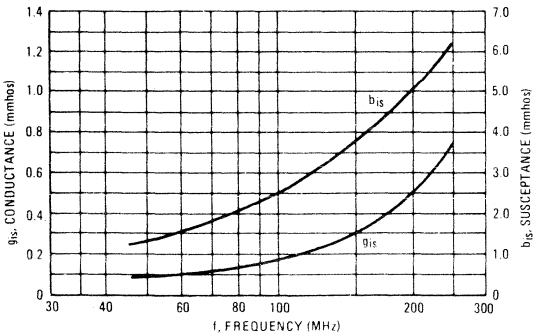


FIGURE 2 – REVERSE TRANSFER ADMITTANCE

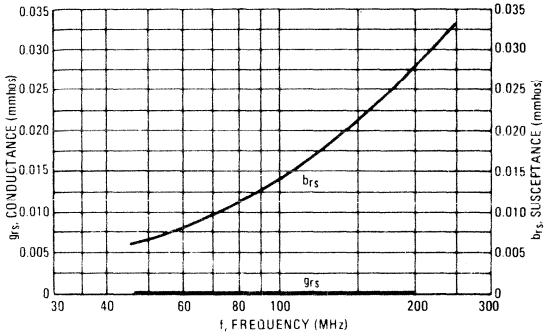


FIGURE 3 – FORWARD TRANSFER ADMITTANCE

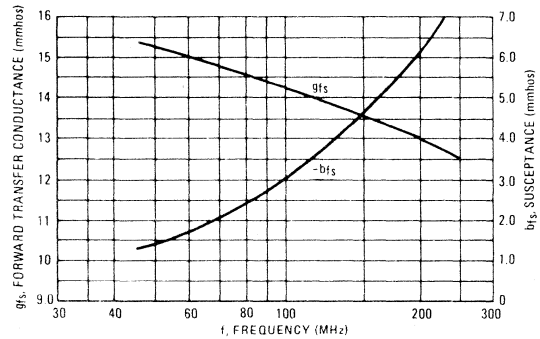
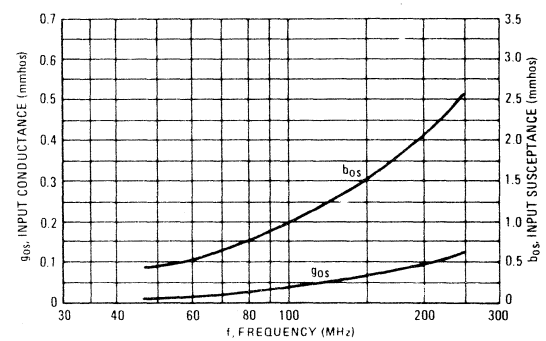


FIGURE 4 – OUTPUT ADMITTANCE



FORWARD TRANSFER ADMITTANCE

(V_{DS} = 15 Vdc, f = 1.0 kHz)

FIGURE 5 – GATE 1

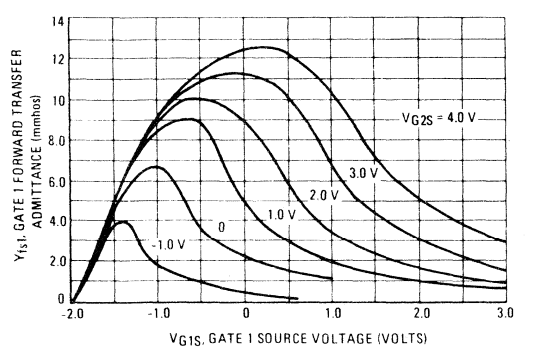


FIGURE 6 – GATE 2

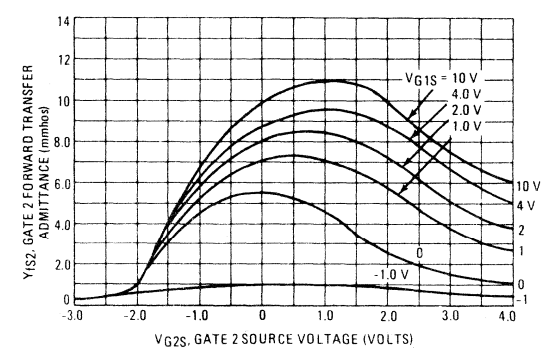


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FIGURE 7 – POWER GAIN

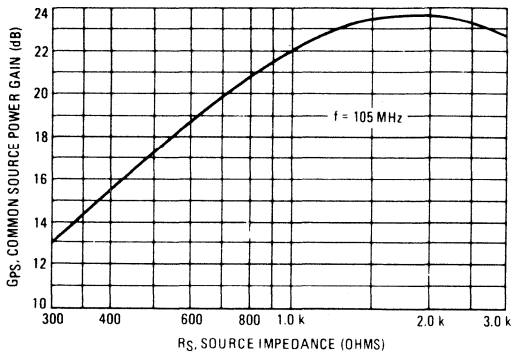


FIGURE 8 – NOISE FIGURE

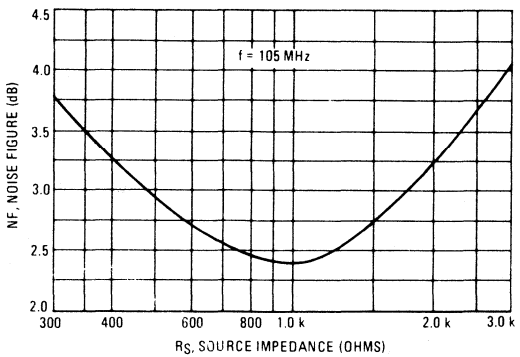


FIGURE 9 – GAIN REDUCTION

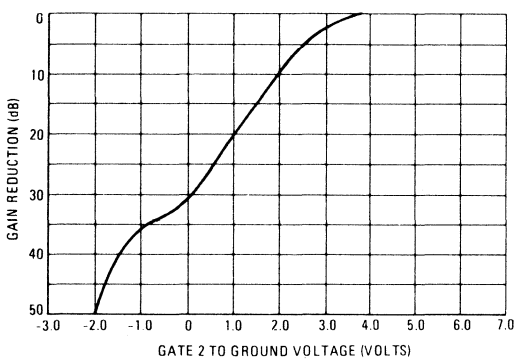


FIGURE 10 – CROSS MODULATION

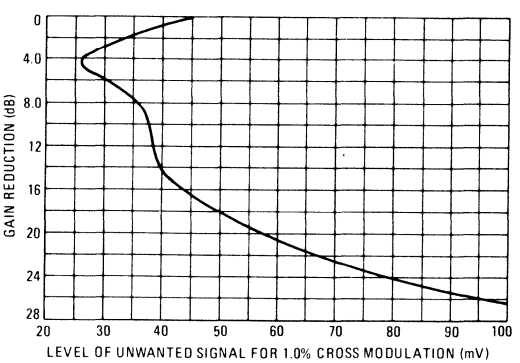
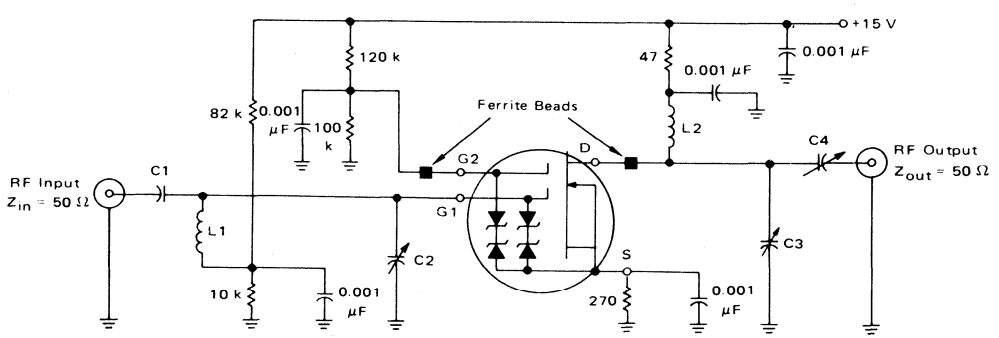


FIGURE 11 – 105 MHz POWER GAIN AND NOISE FIGURE TEST CIRCUIT



The fo lowing component values are for a stern stability factor = 2.0.

L1,L2 126 nH PAUL SMITH CO. SK-138-1
4-½ Turns (yellow)

C1 Nominal 7.0 pF Adjusted for source impedance of approximately 1000 Ω, JOHANSON JMC2951

C2 Nominal 4.0 pF ARCO 402

C3 Nominal 13.73 pF ARCO 403

C4 Nominal 4.36 pF JOHANSON JMC2951

All Decoupling Capacitors are Ceramic Discs.

FIGURE 12 – CONVERSION GAIN

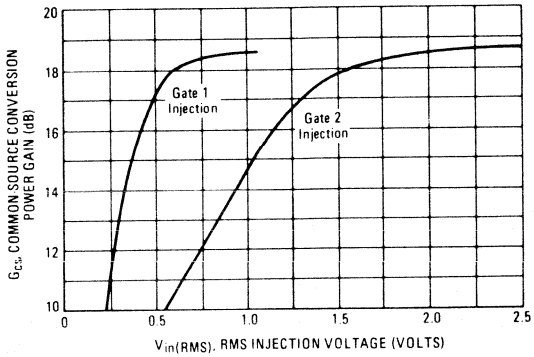
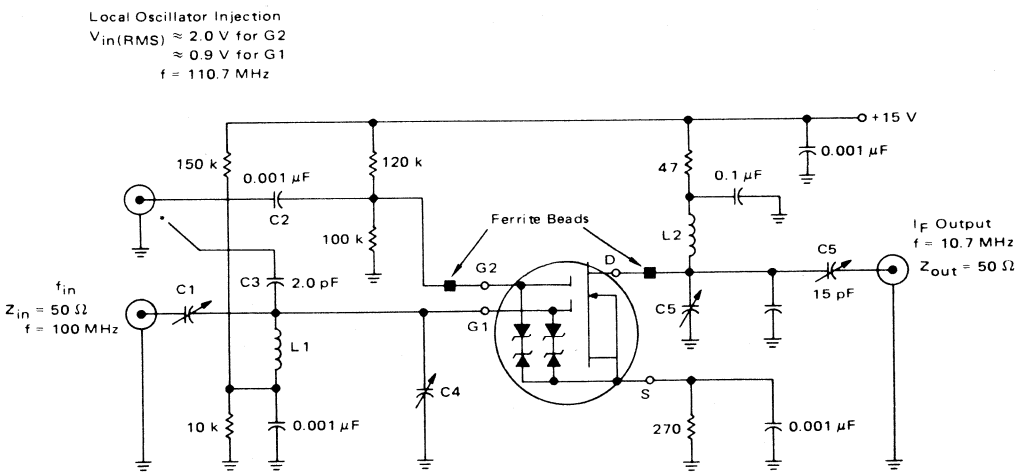


FIGURE 13 – CONVERSION GAIN TEST CIRCUIT



L1 126 nH PAUL SMITH CO. SK-138-1
4-½ Turns (yellow)
L2 2.73 µH High Unloaded Q
C1 JOHANSON JMC2951
C4,C5,C6 ARCO 402

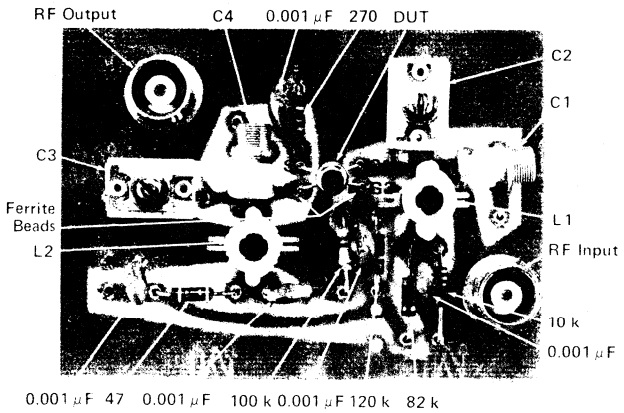
*For G1 injection, C2 is changed to bypass G2 to ground and C3 is added to connect G1 to the injection input.

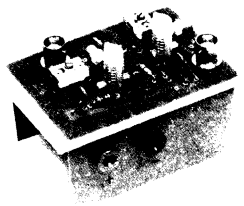
5

PRINTED CIRCUIT BOARD LAYOUT INFORMATION

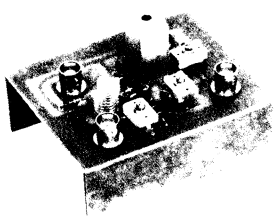
FIGURE 14 – TEST FIXTURES

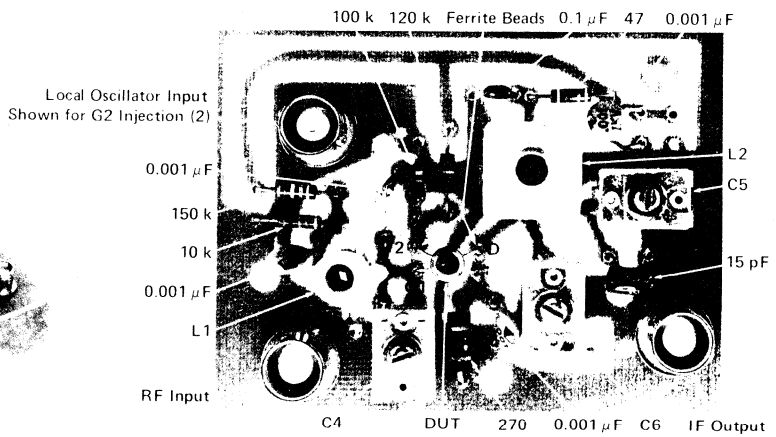
105 MHz POWER GAIN AND NOISE
FIGURE TEST CIRCUIT





100 MHz to 10.7 MHz CONVERSION
GAIN TEST CIRCUIT

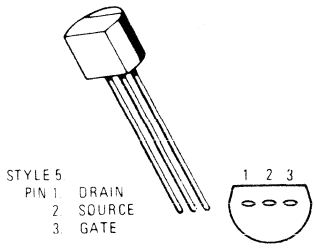




Notes:
1. C1 is on the bottom side of the board.
2. For G1 Injection, C2 is changed to bypass G2 to ground and C3 is added to connect G1 to the injection input. See Figure 13.

MPF102

Silicon N-channel junction field-effect transistor designed for VHF amplifier and mixer applications.



CASE 29
(TO-92)

Drain and Source may be interchanged

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	25	Vdc
Gate-Source Voltage	V_{GS}	25	Vdc
Gate Current	I_G	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D (1)	310 2.82	mW mW/°C
Operating Junction Temperature	T_J (1)	125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Gate-Source Breakdown Voltage (I_G = 10 μAdc, V_{DS} = 0)	BV_{GSS}	25	—	Vdc
Gate Reverse Current (V_{GS} = 15 Vdc, V_{DS} = 0) (V_{GS} = 15 Vdc, V_{DS} = 0, T_A = 100 C)	I_{GSS}	— —	2.0 2.0	nAdc μAdc
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 2.0 nAdc)	$V_{GS(off)}$	—	8.0	Vdc
Gate-Source Voltage (V_{DS} = 15 Vdc, I_D = 0.2 mAdc)	V_{GS}	0.5	7.5	Vdc
ON CHARACTERISTICS				
Zero-Gate-Voltage Drain Current (1) (V_{DS} = 15 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	2.0	20	mAdc
DYNAMIC CHARACTERISTICS				
Forward Transfer Admittance (1) (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 kHz)	$\lvert y_{fs} \rvert$	2000	7500	μmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	7.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	3.0	pF
Forward Transfer Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)	$\lvert y_{fs} \rvert$	1600	—	μmhos
Input Conductance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)	$Re(y_{is})$	—	800	μmhos
Output Conductance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)	$Re(y_{os})$	—	200	μmhos

*Pulse Test: Pulse Width ≤ 630 ms; Duty Cycle ≤ 10%

(1) Continuous package improvements have enhanced these guaranteed Maximum Ratings as follows P_D = 1.0 W @ T_C = 25°C, Derate above 25°C = 8.0 mW/°C, T_J = -65 to +150°C, θ_{JC} = 125° C/W

5

MPF4391
MPF4392 • MPF4393

SILICON N-CHANNEL
JUNCTION FIELD–EFFECT TRANSISTORS

Depletion Mode (Type A) Junction Field-Effect Transistors designed for chopper and high-speed switching applications.

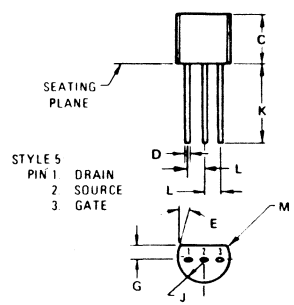
- Low Drain-Source "ON" Resistance –
  $r_{ds(on)}$ = 30 Ohms (Max) – MPF4391
  = 60 Ohms (Max) – MPF4392
  = 100 Ohms (Max) – MPF4393
- Low Reverse Transfer Capacitance –
  C_{rss} = 3.5 pF (Max)
- Guaranteed Fast Switching Times –
  t_{on} = 15 ns (Max) – All Types
  t_{off} = 20 ns (Max) – MPF4391
  = 35 ns (Max) – MPF4392
  = 55 ns (Max) – MPF4393

N-CHANNEL

JUNCTION FIELD-EFFECT TRANSISTORS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	30	Vdc
Drain-Gate Voltage	V_{DG}	30	Vdc
Gate-Source Voltage	V_{GS}	30	Vdc
Forward Gate Current	$I_{G(f)}$	50	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Operating and Storage Channel Temperature Range	$T_{channel}$, T_{stg}	-65 to +150	°C



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
C	0.175	0.185	4.450	4.700
D	0.016	0.019	0.407	0.482
E	5° NOM		5° NOM	
G	0.045	0.055	1.150	1.390
J	0.085	0.095	2.160	2.420
K	0.500	–	12.700	–
L	0.050 TP		1.270 TP	
M	0.003	0.013	0.076	0.330

CASE 29(5)
TO-92

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage (I_G = 1.0 μAdc, V_{DS} = 0)		$V_{(BR)GSS}$	30	–	–	Vdc
Gate-Source Voltage (V_{DS} = 15 Vdc, I_D = 10 nAdc)	MPF4391	V_{GS}	4.0	–	10	Vdc
	MPF4392		2.0	–	5.0	
	MPF4393		0.5	–	3.0	
Gate Reverse Current		I_{GSS}				
(V_{GS} = 15 Vdc, V_{DS} = 0)			–	–	1.0	nAdc
(V_{GS} = 15 Vdc, V_{DS} = 0, T_A = 100°C)			–	–	0.2	μAdc
Drain-Cutoff Current		$I_{D(off)}$				
(V_{DS} = 15 Vdc, V_{GS} = 12 Vdc)			–	–	1.0	nAdc
(V_{DS} = 15 Vdc, V_{GS} = 12 Vdc, T_A = 100°C)			–	–	0.1	μAdc
ON CHARACTERISTICS						
Zero-Gate Voltage Drain Current (1) (V_{DS} = 15 Vdc, V_{GS} = 0)	MPF4391	I_{DSS}	60	–	130	mAdc
	MPF4392		25	–	75	
	MPF4393		5.0	–	30	
Drain-Source "ON" Voltage		$V_{DS(on)}$				Vdc
(I_D = 12 mAdc, V_{GS} = 0)	MPF4391		–	–	0.4	
(I_D = 6.0 mAdc, V_{GS} = 0)	MPF4392		–	–	0.4	
(I_D = 3.0 mAdc, V_{GS} = 0)	MPF4393		–	–	0.4	
Static Drain-Source "ON" Resistance (I_D = 1.0 mAdc, V_{GS} = 0)	MPF4391	$r_{DS(on)}$	–	–	30	Ohms
	MPF4392		–	–	60	
	MPF4393		–	–	100	
SMALL-SIGNAL CHARACTERISTICS						
Forward Transfer Admittance		$\lvert y_{fs} \rvert$				mmhos
(V_{DS} = 15 Vdc, I_D = 60 mAdc, f = 1.0 kHz)	MPF4391		–	20	–	
(V_{DS} = 15 Vdc, I_D = 25 mAdc, f = 1.0 kHz)	MPF4392		–	17	–	
(V_{DS} = 15 Vdc, I_D = 5.0 mAdc, f = 1.0 kHz)	MPF4393		–	12	–	
Drain-Source "ON" Resistance		$r_{ds(on)}$				Ohms
(V_{GS} = 0, I_D = 0, f = 1.0 kHz)	MPF4391		–	–	30	
	MPF4392		–	–	60	
	MPF4393		–	–	100	
Input Capacitance (V_{GS} = 15 Vdc, V_{DS} = 0, f = 1.0 MHz)		C_{iss}	–	6.0	10	pF
Reverse Transfer Capacitance		C_{rss}				pF
(V_{GS} = 12 Vdc, V_{DS} = 0, f = 1.0 MHz)			–	2.5	3.5	
(V_{DS} = 15 Vdc, I_D = 10 mAdc, f = 1.0 MHz)			–	3.2	–	
SWITCHING CHARACTERISTICS (See Figure 5, R_K = 0)						
Turn-On Time (See Figures 1 and 2)		t_{on}				ns
($I_{D(on)}$ = 12 mAdc)	MPF4391		–	3.0	15	
($I_{D(on)}$ = 6.0 mAdc)	MPF4392		–	4.0	15	
($I_{D(on)}$ = 3.0 mAdc)	MPF4393		–	6.5	15	
Rise Time (See Figure 2)		t_r				ns
($I_{D(on)}$ = 12 mAdc)	MPF4391		–	1.2	5.0	
($I_{D(on)}$ = 6.0 mAdc)	MPF4392		–	2.0	5.0	
($I_{D(on)}$ = 3.0 mAdc)	MPF4393		–	2.5	5.0	
Turn-Off Time (See Figures 3 and 4)		t_{off}				ns
($V_{GS(off)}$ = 12 Vdc)	MPF4391		–	10	20	
($V_{GS(off)}$ = 7.0 Vdc)	MPF4392		–	20	35	
($V_{GS(off)}$ = 5.0 Vdc)	MPF4393		–	37	55	
Fall Time (See Figure 4)		t_f				ns
($V_{GS(off)}$ = 12 Vdc)	MPF4391		–	7.0	15	
($V_{GS(off)}$ = 7.0 Vdc)	MPF4392		–	15	20	
($V_{GS(off)}$ = 5.0 Vdc)	MPF4393		–	29	35	

(1) Pulse Test: Pulse Width ≤ 100 μs, Duty Cycle ≤ 1.0%.

5

TYPICAL SWITCHING CHARACTERISTICS

FIGURE 1 – TURN-ON DELAY TIME

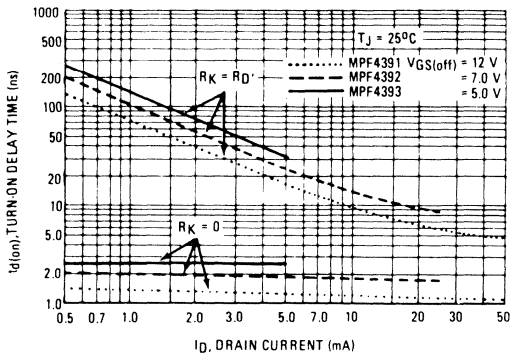


FIGURE 2 – RISE TIME

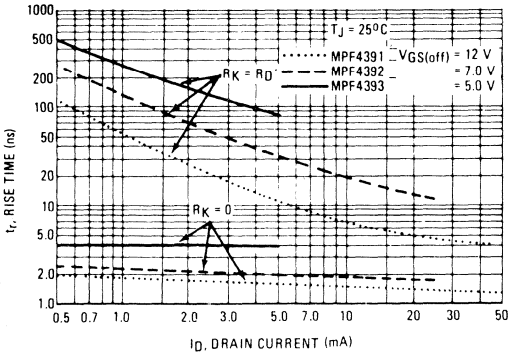


FIGURE 3 – TURN-OFF DELAY TIME

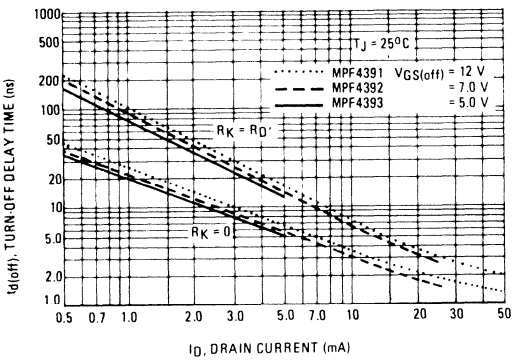


FIGURE 4 – FALL TIME

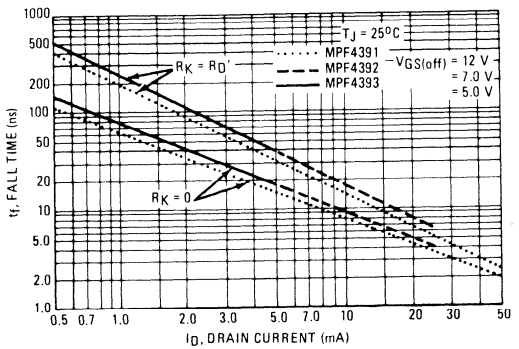
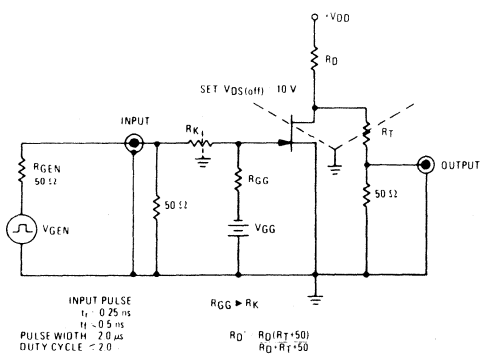


FIGURE 5 – SWITCHING TIME TEST CIRCUIT



NOTE 1

The switching characteristics shown above were measured using a test circuit similar to Figure 5. At the beginning of the switching interval, the gate voltage is at Gate Supply Voltage ($-V_{GG}$). The Drain-Source Voltage (V_{DS}) is slightly lower than Drain Supply Voltage (V_{DD}) due to the voltage divider. Thus Reverse Transfer Capacitance (C_{rss}) or Gate-Drain Capacitance (C_{gd}) is charged to $V_{GG} + V_{DS}$.

During the turn-on interval, Gate-Source Capacitance (C_{gs}) discharges through the series combination of R_{Gen} and R_K. C_{gd} must discharge to $V_{DS(on)}$ through R_G and R_K in series with the parallel combination of effective load impedance (R'_D) and Drain-Source Resistance (r_{ds}). During the turn-off, this charge flow is reversed.

Predicting turn-on time is somewhat difficult as the channel resistance r_{ds} is a function of the gate-source voltage. While C_{gs} discharges, V_{GS} approaches zero and r_{ds} decreases. Since C_{gd} discharges through r_{ds}, turn-on time is non-linear. During turn-off, the situation is reversed with r_{ds} increasing as C_{gd} charges.

The above switching curves show two impedance conditions; 1) R_K is equal to $R_{D'}$ which simulates the switching behavior of cascaded stages where the driving source impedance is normally the load impedance of the previous stage, and 2) $R_K = 0$ (low impedance) the driving source impedance is that of the generator.

FIGURE 6 – TYPICAL FORWARD TRANSFER ADMITTANCE

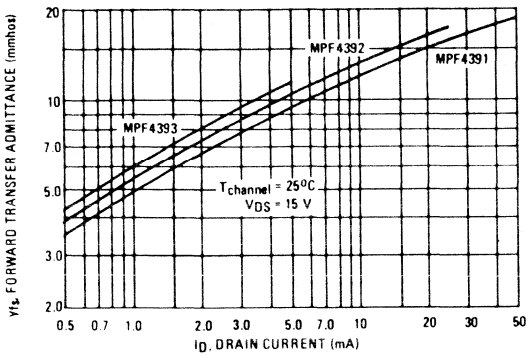


FIGURE 7 – TYPICAL CAPACITANCE

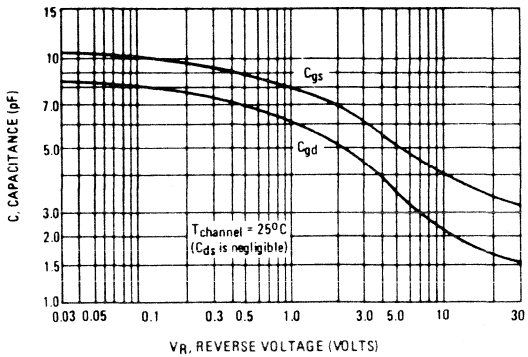


FIGURE 8 – EFFECT OF GATE-SOURCE VOLTAGE ON DRAIN-SOURCE RESISTANCE

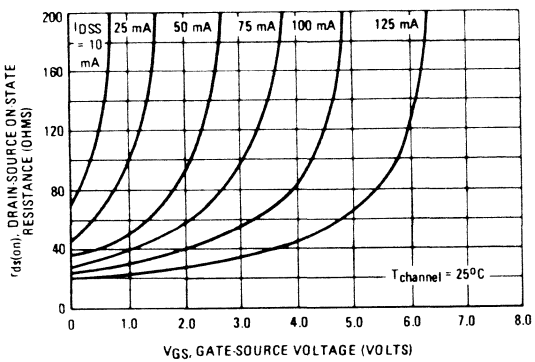


FIGURE 9 – EFFECT OF TEMPERATURE ON DRAIN–SOURCE ON-STATE RESISTANCE

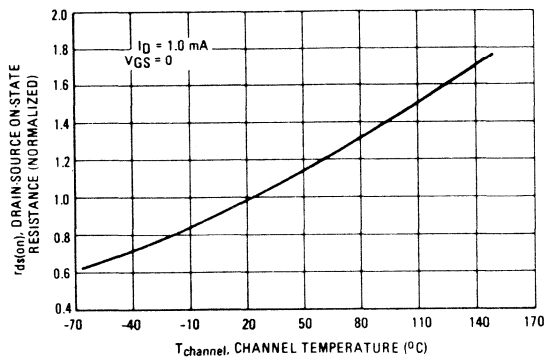
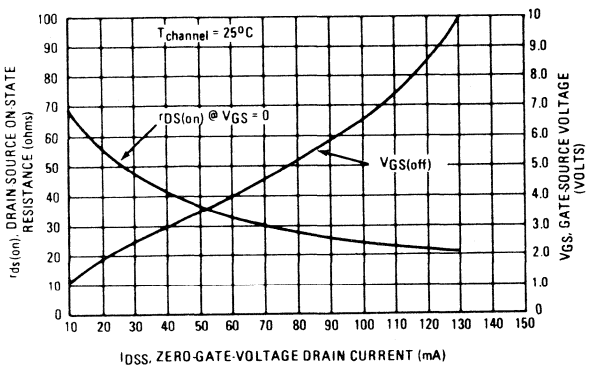


FIGURE 10 – EFFECT OF IDSS ON DRAIN-SOURCE RESISTANCE AND GATE SOURCE VOLTAGE



NOTE 2

The Zero-Gate-Voltage Drain Current (I_{DSS}), is the principle determinant of other J-FET characteristics. Figure 10 shows the relationship of Gate-Source Off Voltage ($V_{GS(off)}$) and Drain-Source On Resistance ($r_{ds(on)}$) to I_{DSS}. Most of the devices will be within ±10% of the values shown in Figure 10. This data will be useful in predicting the characteristic variations for a given part number.

For example:

Unknown

$r_{ds(on)}$ and V_{GS} range for an MPF4392

The electrical characteristics table indicates that an MPF4392 has an I_{DSS} range of 25 to 75 mA. Figure 10, shows $r_{ds(on)}$ = 52 Ohms for I_{DSS} = 25 mA and 30 Ohms for I_{DSS} = 75 mA. The corresponding V_{GS} values are 2.2 volts and 4.8 volts.

5

2N4117,A
2N4118,A • 2N4119,A

N-CHANNEL SILICON JUNCTION FIELD-EFFECT TRANSISTORS

These devices are designed for very low input current DC amplifier applications.

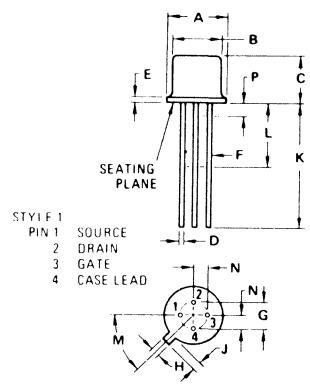
- Ultra-Low Input Leakage Current –
  I_{GSS} = 1.0 pAdc (Max) – 2N4117A, 18A, 19A
  = 10 pAdc (Max) – 2N4117, 18, 19

N-CHANNEL SILICON JUNCTION FIELD-EFFECT TRANSISTORS

***MAXIMUM RATINGS**

Rating	Symbol	Max	Unit
Gate-Source Voltage	V_{DS}	-40	Vdc
Gate-Drain Voltage	V_{DG}	-40	Vdc
Gate Current	I_G	50	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 2.0	mW mW/°C
Storage Temperature Range	T_{stg}	-65 to +175	°C
Lead Temperature (1/16" from case for 10 s)	T_{LEAD}	255	°C

*Indicates JEDEC Registered Data.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03
TO-72

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted)

Characteristics		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Gate-Source Breakdown Voltage (I_G = -1.0 μAdc, V_{DS} = 0)		BV_{GSS}	-40	–	Vdc
Gate Reverse Current		I_{GSS}			
(V_{GS} = 20 Vdc, V_{DS} = 0)	2N4117, 4118, 4119		–	-10	pAdc
	2N4117A, 4118A, 4119A		–	-1.0	
(V_{GS} = 20 Vdc, V_{DS} = 0, T_A = 150°C)	2N4117, 4118, 4119		–	-25	nAdc
	2N4117A, 4118A, 4119A		–	-2.5	
Gate-Source Cutoff Voltage		$V_{GS(off)}$			Vdc
(I_D = 1.0 nAdc, V_{DS} = 10 Vdc)	2N4117, A		-0.6	-1.8	
	2N4118, A		-1.0	-3.0	
	2N4119, A		-2.0	-6.0	
ON CHARACTERISTICS					
Zero-Gate Voltage Drain Current		I_{DSS}			mAdc
(V_{DS} = 10 Vdc, V_{GS} = 0)	2N4117, A		0.03	0.09	
	2N4118, A		0.08	0.24	
	2N4119, A		0.20	0.60	
DYNAMIC CHARACTERISTICS					
Small-Signal Common-Source Forward Transconductance		g_{fs}			μmhos
(V_{DS} = 10 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N4117, A		70	210	
	2N4118, A		80	250	
	2N4119, A		100	330	
Small-Signal Common-Source Output Conductance		g_{os}			μmhos
(V_{DS} = 10 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N4117, A		–	3.0	
	2N4118, A		–	5.0	
	2N4119, A		–	10	
Input Capacitance (V_{DS} = 10 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	–	3.0	pF
Reverse Transfer Capacitance (V_{DS} = 10 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	–	1.5	pF

*Indicates JEDEC Registered Data.

(1) I_{DSS} is measured during a 2.0-ms interval 100 ms after power is applied. (NOT a JEDEC condition.)

FIGURE 1 – TRANSFER CHARACTERISTICS

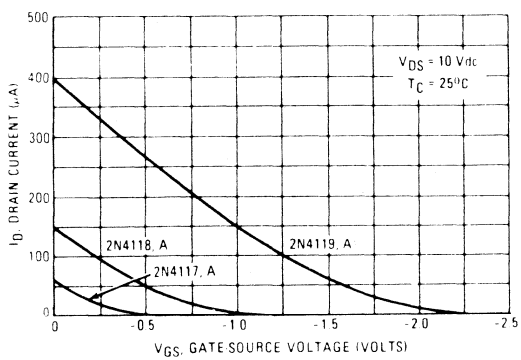
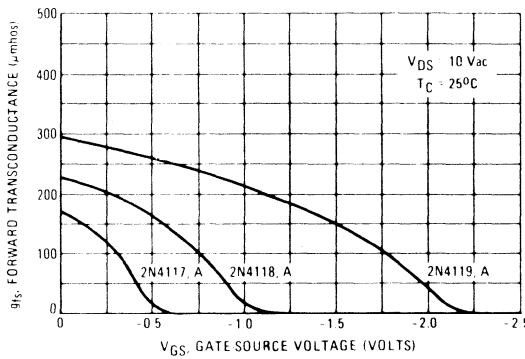


FIGURE 2 – TRANSCONDUCTANCE CHARACTERISTICS



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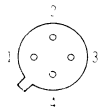
2N4351

CASE 20-02
(TO-72)



STYLE 2
PIN 1 SOURCE
2 GATE
3 DRAIN
4 SUBSTRATE AND CASE LEAD

Silicon N-channel MOS field effect transistors, designed for enhancement-mode operation in low power switching applications. The 2N4351 is complementary with type 2N4352 .

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	30	Vdc
Gate-Source Voltage	V_{GS}	± 30	Vdc
Drain Current	I_D	30	mAdc
Power Dissipation at T_A = 25°C Derate above 25°C	P_D	300 1.7	mW mW/°C
Power Dissipation at T_C = 25°C Derate about 25°C	P_D	800 4.56	mW mW/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

HANDLING PRECAUTIONS:

MOS field-effect transistors have extremely high input resistance. They can be damaged by the accumulation of excess static charge. Avoid possible damage to the devices while handling, testing, or in actual operation, by following the procedures outlined below:

1. To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used.
2. Avoid unnecessary handling. Pick up devices by the case instead of the leads.
3. Do not insert or remove devices from circuits with the power on because transient voltages may cause permanent damage to the devices.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Substrate connected to source.

Characteristic	Figure No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (I_D = 10 μA, V_{GS} = 0)	—	$V_{(BR)DSS}$	25	—	Vdc
Gate Leakage Current (V_{GS} = ±30 Vdc, V_{DS} = 0)	—	I_{GSS}	—	10	pAdc
Zero-Gate-Voltage Drain Current (V_{DS} = 10 V, V_{GS} = 0)	—	I_{DSS}	—	10	nAdc
ON CHARACTERISTICS					
Gate-Source Threshold Voltage (V_{DS} = 10 V, I_D = 10 μA)	—	$V_{GS(TH)}$	1.0	5.0	Vdc
"ON" Drain Current (V_{GS} = 10 V, V_{DS} = 10 V)	3	$I_{D(on)}$	3.0	—	mAdc
Drain-Source "ON" Voltage (I_D = 2 mA, V_{GS} = 10 V)	—	$V_{DS(on)}$	—	1.0	Vdc
SMALL SIGNAL CHARACTERISTICS					
Drain-Source Resistance (V_{GS} = 10 V, I_D = 0, f = 1 kHz)	4	$r_{ds(on)}$	—	300	ohms
Forward Transfer Admittance (V_{DS} = 10 V, I_D = 2 mA, f = 1 kHz)	1	$\lvert y_{fs} \rvert$	1000	—	μmho
Reverse Transfer Capacitance (V_{DS} = 0, V_{GS} = 0, f = 140 kHz)	2	C_{rss}	—	1.3	pF
Input Capacitance (V_{DS} = 10 V, V_{GS} = 0, f = 140 kHz)	2	C_{iss}	—	5.0	pF
Drain-Substrate Capacitance ($V_{D(SUB)}$ = 10 V, f = 140 kHz)	—	$C_{d(sub)}$	—	5.0	pF
SWITCHING CHARACTERISTICS					
Turn-On Delay	I_D = 2.0 mAdc, V_{DS} = 10 Vdc, V_{GS} = 10 Vdc (See Figure 10; Times Circuit Determined)	6, 10	t_{d1}	—	45	ns
Rise Time		7, 10	t_r	—	65	ns
Turn-Off Delay		8, 10	t_{d2}	—	60	ns
Fall Time		9, 10	t_f	—	100	ns

FIGURE 1 — FORWARD TRANSFER ADMITTANCE

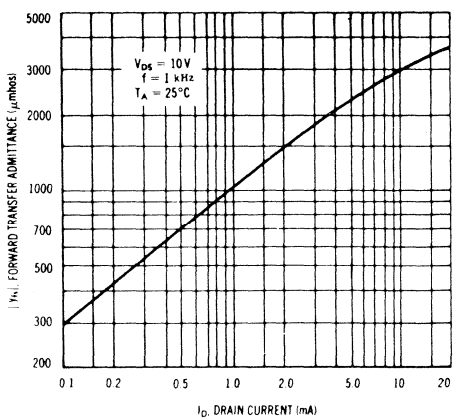


FIGURE 2 — CAPACITANCE

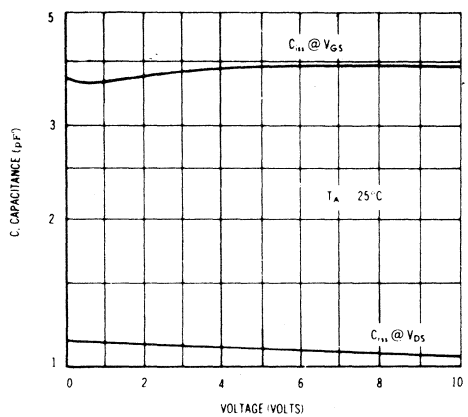


FIGURE 3 — TRANSFER CHARACTERISTICS

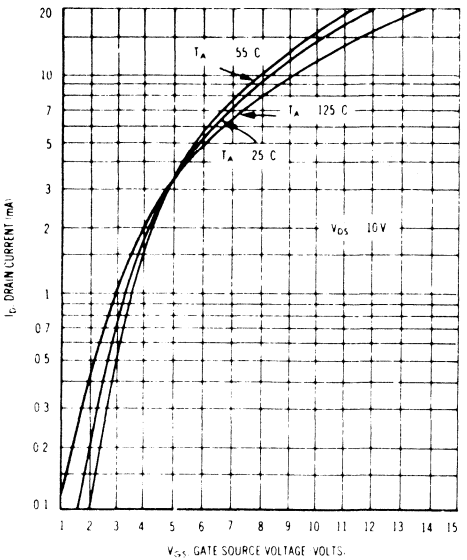


FIGURE 4 — DRAIN SOURCE "ON" RESISTANCE

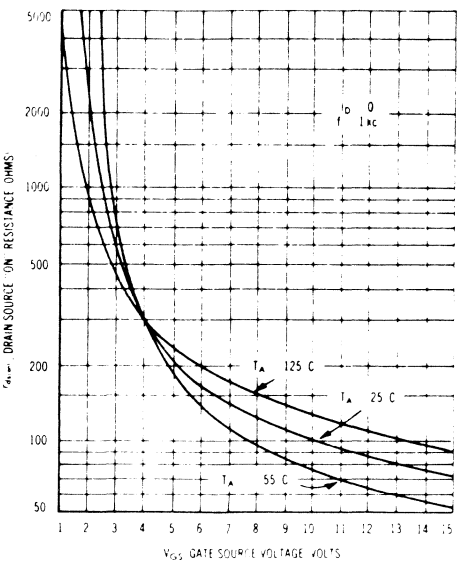
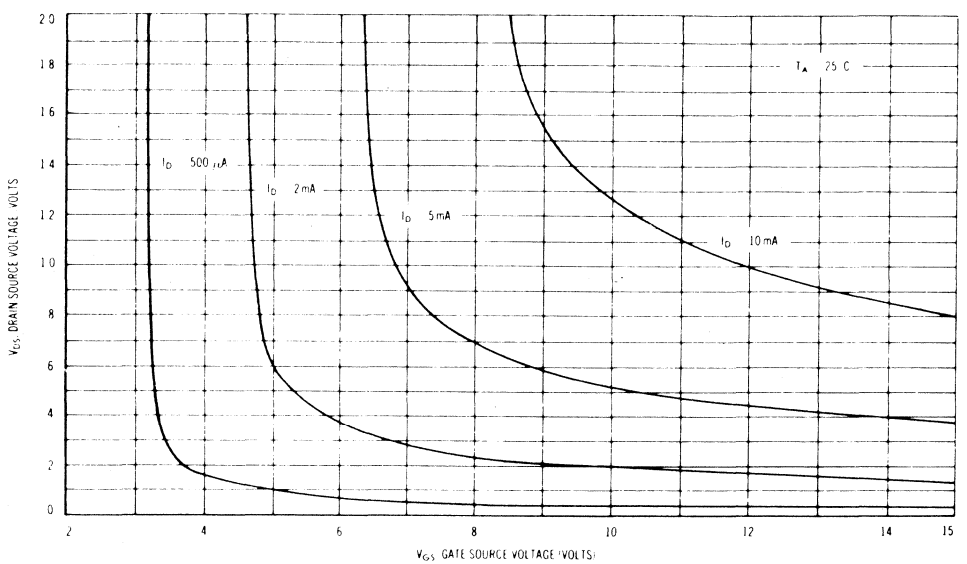


FIGURE 5 — "ON" DRAIN-SOURCE VOLTAGE



SWITCHING CHARACTERISTICS

(T_A = 25°C)

FIGURE 6 — TURN-ON DELAY TIME

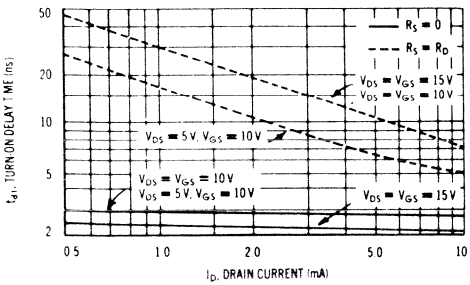


FIGURE 7 — RISE TIME

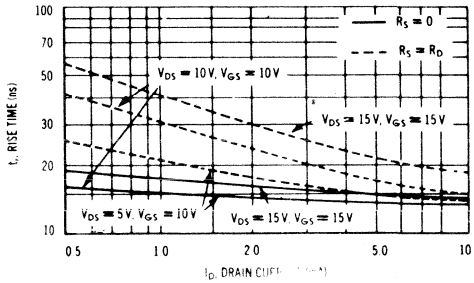


FIGURE 8 — TURN-OFF DELAY TIME

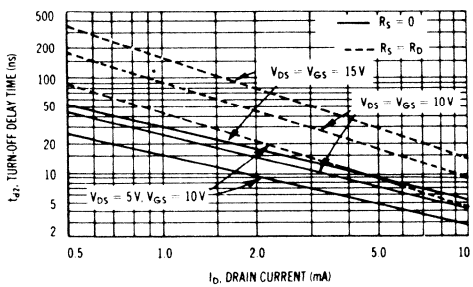


FIGURE 9 — FALL TIME

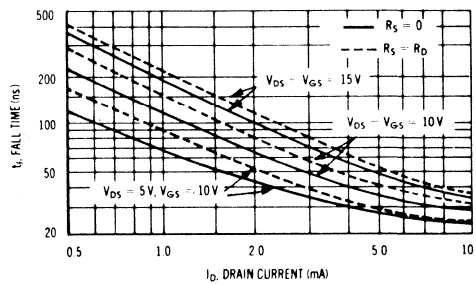
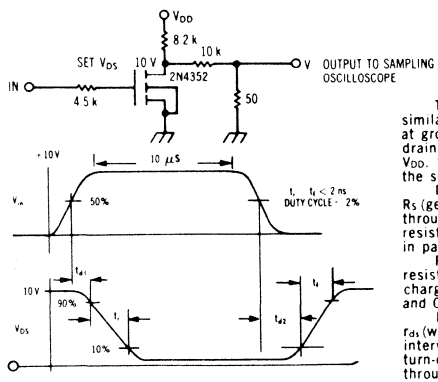


FIGURE 10 — SWITCHING CIRCUIT and WAVEFORMS



The switching characteristics shown above were measured in a test circuit similar to Figure 10. At the beginning of the switching interval, the gate voltage is at ground and the gate-source capacitance ($C_{gs} = C_{rss} - C_{rss}$) has no charge. The drain voltage is at V_{DD}, and thus the feedback capacitance (C_{rss}) is charged to V_{DD}. Similarly, the drain-substrate capacitance ($C_{d(sub)}$) is charged to V_{DD} since the substrate and source are connected to ground.

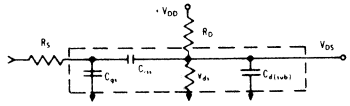
During the turn-on interval, C_{gs} is charged to V_{GS} (the input voltage) through R_S (generator impedance) (Figure 11). C_{rss} must be discharged to $V_{GS} - V_{D(on)}$ through R_S and the parallel combination of the load resistor (R_D) and the channel resistance (r_{ds}). In addition, $C_{d(sub)}$ is discharged to a low value ($V_{D(on)}$) through R_D in parallel with r_{ds}. During turn-off this charge flow is reversed.

Predicting turn-on time proves to be somewhat difficult since the channel resistance (r_{ds}) is a function of the gate-source voltage (V_{GS}). As C_{gs} becomes charged V_{GS} is approaching V_{in} and r_{ds} decreases (see Figure 4) and since C_{rss} and $C_{d(sub)}$ are charged through r_{ds}, turn-on time is quite non-linear.

If the charging time of C_{gs} is short compared to that of C_{rss} and $C_{d(sub)}$, then r_{ds} (which is in parallel with R_D) will be low compared to R_D during the switching interval and will largely determine the turn-on time. On the other hand, during turn-off r_{ds} will be almost an open circuit requiring C_{rss} and $C_{d(sub)}$ to be charged through R_D and resulting in a turn-off time that is long compared to the turn-on time. This is especially noticeable for the curves where $R_S = 0$ and C_{gs} is charged through the pulse generator impedance only.

The switching curves shown with $R_S = R_D$ simulate the switching behavior of cascaded stages where the driving source impedance is normally the same as the load impedance. The set of curves with $R_S = 0$ simulates a low source impedance drive such as might occur in complementary logic circuits.

FIGURE 11 — SWITCHING CIRCUIT with MOSFET EQUIVALENT MODEL



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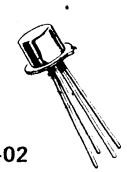
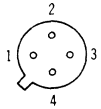
2N4352



CASE 20-02
(TO-72)



STYLE 2
PIN 1. SOURCE
2. GATE
3. DRAIN
4. SUBSTRATE AND CASE LEAD

Silicon P-channel MOS field-effect transistor designed for enhancement-mode operation in low-power switching applications. The 2N4352 is complementary with type 2N4351.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	30	Vdc
Gate-Source Voltage	V_{GS}	± 30	Vdc
Drain Current	I_D	30	mAdc
Power Dissipation at T_A = 25°C Derate above 25°C	P_D	300 1.7	mW mW/°C
Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	800 4.56	mW mW/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

HANDLING PRECAUTIONS:

MOS field-effect transistors have extremely high input resistance. They can be damaged by the accumulation of excess static charge. Avoid possible damage to the devices while handling, testing, or in actual operation, by following the procedures outlined below:

1. To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used.
2. Avoid unnecessary handling. Pick up devices by the case instead of the leads.
3. Do not insert or remove devices from circuits with the power on because transient voltages may cause permanent damage to the devices.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Substrate connected to source.

Characteristic	Figure No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (I_D = -10 μA, V_{GS} = 0)	—	$V_{(BR)DSS}$	25	—	Vdc
Gate Leakage Current (V_{GS} = ±30 V, V_{DS} = 0)	—	I_{GSS}	—	10	pAdc
Zero-Gate Voltage Drain Current (V_{DS} = -10 V, V_{GS} = 0)	—	I_{DSS}	—	10	nAdc
ON CHARACTERISTICS					
Gate-Source Threshold Voltage (V_{DS} = -10 V, I_D = -10 μA)	—	$V_{GS(TH)}$	1.0	5.0	Vdc
"ON" Drain Current (V_{GS} = -10 V_{DS} = -10 V)	3	$I_{D(on)}$	3.0	—	mA
Drain-Source "ON" Voltage (I_D = -2.0 mA, V_{GS} = -10 V)	5	$V_{DS(on)}$	—	1.0	V
SMALL SIGNAL CHARACTERISTICS					
Drain-Source Resistance (V_{GS} = -10 V, I_D = 0, f = 1 kHz)	4	$r_{ds(on)}$	—	600	ohms
Forward Transfer Admittance (V_{DS} = -10 V, I_D = 2 mA, f = 1 kHz)	1	$\lvert y_{fs} \rvert$	1000	—	μmho
Reverse Transfer Capacitance (V_{DS} = 0, V_{GS} = 0, f = 140 kHz)	2	C_{rss}	—	1.3	pF
Input Capacitance (V_{DS} = -10 V, V_{GS} = 0, f=140 kHz)	2	C_{iss}	—	5.0	pF
Drain-Substrate Capacitance ($V_{D(SUB)}$= -10 V, f=140 kHz)	—	$C_{d(sub)}$	—	4.0	pF
SWITCHING CHARACTERISTICS					
Turn-On Delay	I_D = -2.0 mAdc, V_{DS} = -10 Vdc, V_{GS} = -10 V (See Figure 10, Times Circuit Determined)	6, 10	t_{d1}	—	45	ns
Rise Time		7, 10	t_r	—	65	ns
Turn-Off Delay		8, 10	t_{d2}	—	60	ns
Fall Time		9, 10	t_f	—	100	ns

FIGURE 1 — FORWARD TRANSFER ADMITTANCE

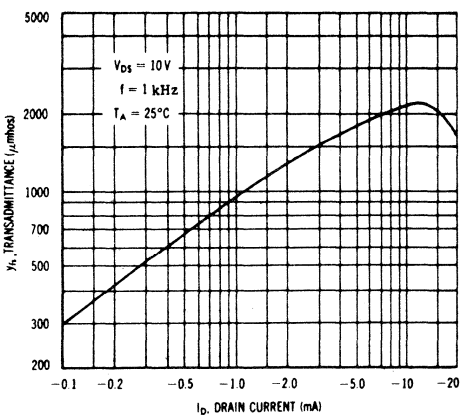


FIGURE 2 — CAPACITANCE

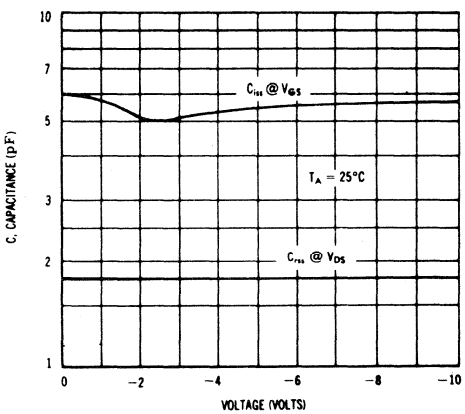


FIGURE 3 — TRANSFER CHARACTERISTICS

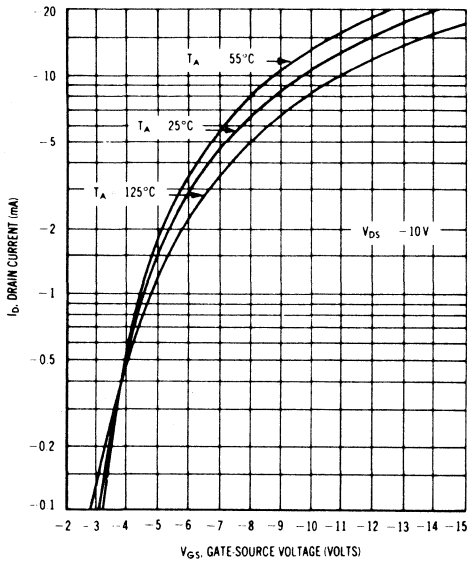


FIGURE 4 — DRAIN SOURCE "ON" RESISTANCE

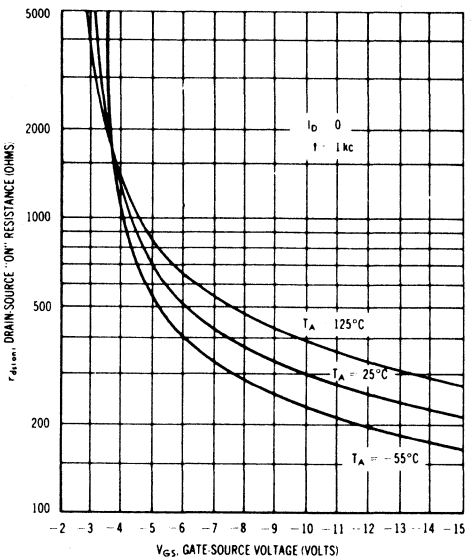
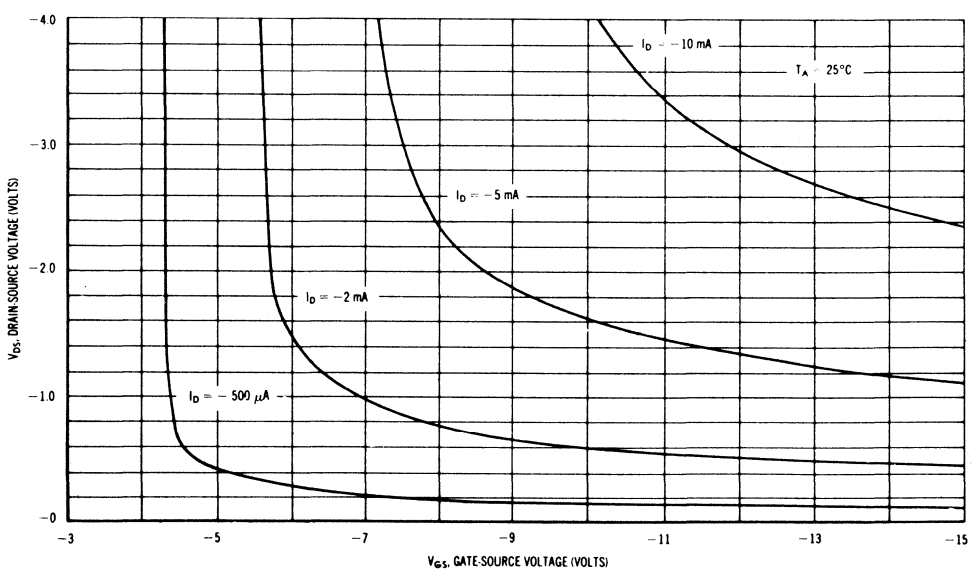


FIGURE 5 — "ON" DRAIN-SOURCE VOLTAGE



SWITCHING CHARACTERISTICS

($T_A = 25°C$)

FIGURE 6 — TURN-ON DELAY TIME

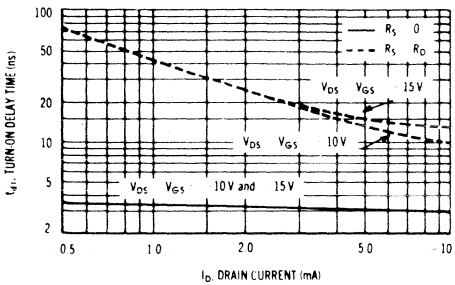


FIGURE 7 — RISE TIME

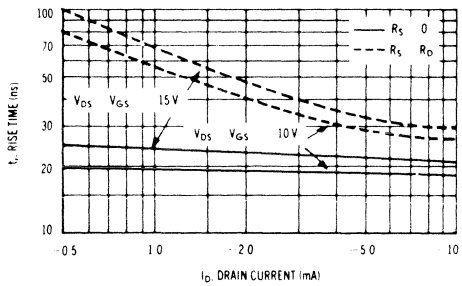


FIGURE 8 — TURN-OFF DELAY TIME

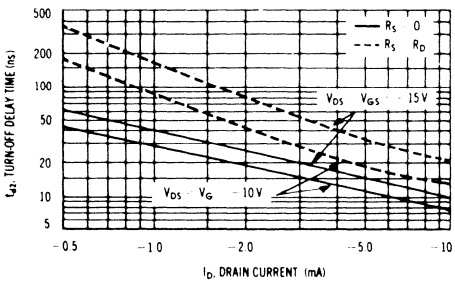


FIGURE 9 — FALL TIME

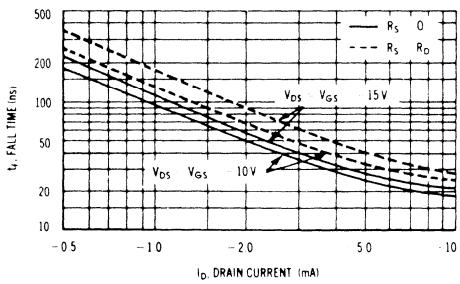
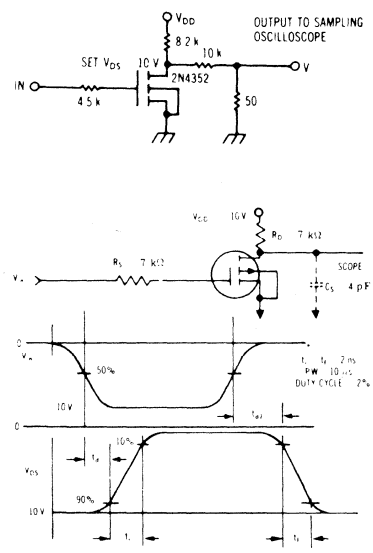


FIGURE 10 — SWITCHING CIRCUIT and WAVEFORMS



The switching characteristics shown above were measured in a test circuit similar to Figure 10. At the beginning of the switching interval, the gate voltage is at ground and the gate-source capacitance ($C_{gs} = C_{rss} + C_{rss}$) has no charge. The drain voltage is at V_{DD}, and thus the feedback capacitance (C_{rss}) is charged to V_{DD}. Similarly, the drain-substrate capacitance ($C_{d(sub)}$) is charged to V_{DD} since the substrate and source are connected to ground.

During the turn-on interval, C_{gs} is charged to V_{GS} (the input voltage) through R_S (generator impedance) (Figure 11). C_{rss} must be discharged to $V_{GS} = V_{D(on)}$ through R_S and the parallel combination of the load resistor (R_D) and the channel resistance (r_{ds}). In addition, $C_{d(sub)}$ is discharged to a low value ($V_{D(on)}$) through R_D in parallel with r_{ds}. During turn-off this charge flow is reversed.

Predicting turn-on time proves to be somewhat difficult since the channel resistance (r_{ds}) is a function of the gate-source voltage (V_{GS}). As C_{gs} becomes charged V_{GS} is approaching V_{in} and r_{ds} decreases (see Figure 4) and since C_{rss} and $C_{d(sub)}$ are charged through r_{ds}, turn-on time is quite non-linear.

If the charging time of C_{gs} is short compared to that of C_{rss} and $C_{d(sub)}$, then r_{ds} (which is in parallel with R_D) will be low compared to R_D during the switching interval and will largely determine the turn-on time. On the other hand, during turn-off r_{ds} will be almost an open circuit requiring C_{rss} and $C_{d(sub)}$ to be charged through R_D and resulting in a turn-off time that is long compared to the turn-on time. This is especially noticeable for the curves where $R_S = 0$ and C_{gs} is charged through the pulse generator impedance only.

The switching curves shown with $R_S = R_D$ simulate the switching behavior of cascaded stages where the driving source impedance is normally the same as the load impedance. The set of curves with $R_S = 0$ simulates a low source impedance drive such as might occur in complementary logic circuits.

FIGURE 11 — SWITCHING CIRCUIT with MOSFET EQUIVALENT MODEL

2N4416

SILICON N-CHANNEL
JUNCTION FIELD-EFFECT TRANSISTOR

. . . designed for VHF/UHF amplifier applications.

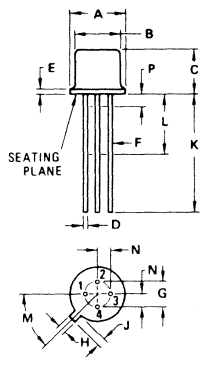
- Low Noise Figure –
  NF = 2.0 dB (Max) @ 100 MHz
  = 4.0 dB (Max) @ 400 MHz
- Low Feedback Capacitance –
  C_{rss} = 0.8 pF (Max)
- Low Output Capacitance –
  C_{oss} = 2.0 pF (Max)
- High Transfer Admittance –
  $Y_{fs(real)}$ = 4000 μmho (Min)
- High Power Gain –
  G_{ps} = 18 dB (Min) @ 100 MHz
  = 10 dB (Min) @ 400 MHz
- S and Y Parameter Curves Provided

***MAXIMUM RATINGS** (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Drain Source Voltage	V_{DS}	30	Vdc
Drain-Gate Voltage	V_{DG}	30	Vdc
Gate-Source Voltage	V_{GS}	30	Vdc
Gate Current	I_G	10	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 1.71	mW mW/°C
Operating and Storage Channel Temperature Range	$T_{channel}$, T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.

N-CHANNEL
JUNCTION
FIELD-EFFECT
TRANSISTOR



STYLE 1
PIN 1. SOURCE
2. DRAIN
3. GATE
4. CASE LEAD

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03
TO-72

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTIC				
Gate-Source Breakdown Voltage (I_G = 1.0 μAdc, V_{DS} = 0)	$V_{(BR)GSS}$	30	–	Vdc
Gate-Source Cutoff Voltage (I_D = 1.0 nAdc, V_{DS} = 15 Vdc)	$V_{GS(off)}$	–	6.0	Vdc
Gate-Source Voltage (I_D = 0.5 mAdc, V_{DS} = 15 Vdc)	V_{GS}	1.0	5.5	Vdc
Gate-Source Forward Voltage (I_G = 1.0 mAdc, V_{DS} = 0)	$V_{GS(F)}$	–	1.0	Vdc
Gate Reverse Current	I_{GSS}			pAdc
(V_{GS} = 20 Vdc, V_{DS} = 0)		–	100	
(V_{GS} = 20 Vdc, V_{DS} = 0, T_A = +150°C)		–	200	
ON CHARACTERISTICS				
Zero-Gate Voltage Drain Current (1) (V_{DS} = 15 Vdc, V_{GS} = 0)	I_{DSS}	5.0	15	mAdc
SMALL-SIGNAL CHARACTERISTICS				
Forward Transfer Admittance (1) (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	$\|y_{fs}\|$	4500	7500	μmhos
Real Part of Forward Transfer Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 400 MHz)	$y_{fs(real)}$	4000	–	μmhos
Real Part of Input Admittance	$y_{is(real)}$			μmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)		–	100	
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 400 MHz)		–	1000	
Output Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	$\|y_{os}\|$	–	50	μmhos
Real Part of Output Admittance	$y_{os(real)}$			μmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)		–	75	
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 400 MHz)		–	100	
Imaginary Part of Input Admittance	$y_{is(imag)}$			μmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)		–	2500	
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 400 MHz)		–	10,000	
Imaginary Part of Output Admittance	$y_{os(imag)}$			μmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)		–	1000	
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 400 MHz)		–	4000	
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	–	4.0	pF
Common-Source Output Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	–	2.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	–	0.8	pF
Common-Source Spot Noise (Figures 3 and 4)	NF			dB
(V_{DS} = 15 Vdc, I_D = 5.0 mAdc, $R_g \approx$ 1000 Ohms, f = 100 MHz)		–	2.0	
(V_{DS} = 15 Vdc, I_D = 5.0 mAdc, $R_g \approx$ 1000 Ohms, f = 400 MHz)		–	4.0	
Small-Signal Power Gain (Figure 1)	G_{ps}			dB
(V_{DS} = 15 Vdc, I_D = 5.0 mAdc, f = 100 MHz)		18	–	
(V_{DS} = 15 Vdc, I_D = 5.0 mAdc, f = 400 MHz)		10	–	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 1.0%.

*Indicates JEDEC Registered Data.

5

POWER GAIN

FIGURE 1 – EFFECTS OF DRAIN CURRENT

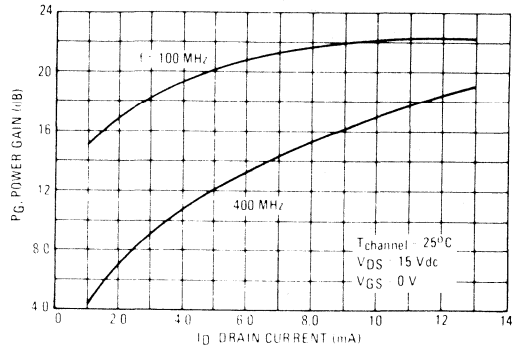
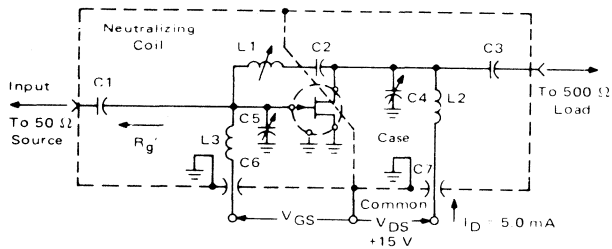


FIGURE 2 – 100 MHz and 400 MHz NEUTRALIZED TEST CIRCUIT



Adjust V_{GS} for I_D = 50 mA
V_{GS} < 0 Volts

NOTE: The noise source is a hot cold body (AIL type 70 or equivalent) with a test receiver (AIL type 136 or equivalent).

Reference Designation	VALUE	
	100 MHz	400 MHz
C1	7.0 pF	1.8 pF
C2	1000 pF	17 pF
C3	3.0 pF	1.0 pF
C4	1.12 pF	0.8-8.0 pF
C5	1.12 pF	0.8-8.0 pF
C6	0.0015 μF	0.001 μF
C7	0.0015 μF	0.001 μF
L1	3.0 μH*	0.2 μH**
L2	0.15 μH*	0.03 μH**
L3	0.14 μH*	0.022 μH**

*L1 17 turns, (approx. – depends upon circuit layout) AWG #28 enameled copper wire, close wound on 9/32" ceramic coil form. Tuning provided by a powdered iron slug.

L2 4-1/2 turns, AWG #18 enameled copper wire, 5/16" long, 3/8" I.D. (AIR CORE).

L3 3-1/2 turns, AWG #18 enameled copper wire, 1/4" long, 3/8" I.D. (AIR CORE).

**L1 6 turns, (approx. – depends upon circuit layout) AWG #24 enameled copper wire, close wound on 7/32" ceramic coil form. Tuning provided by an aluminum slug.

L2 1 turn, AWG #16 enameled copper wire, 3/8" I.D. (AIR CORE).

L3 1/2 turn, AWG #16 enameled copper wire, 1/4" I.D. (AIR CORE).

NOISE FIGURE

($T_{channel}$ = 25°C)

FIGURE 3 – EFFECTS OF DRAIN SOURCE VOLTAGE

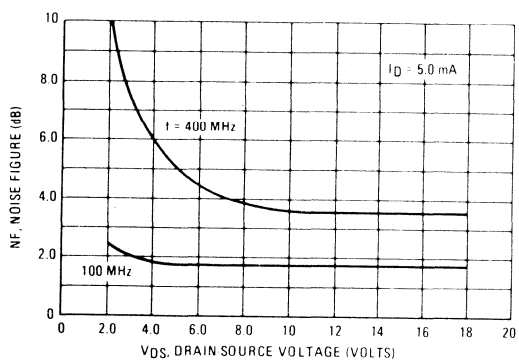
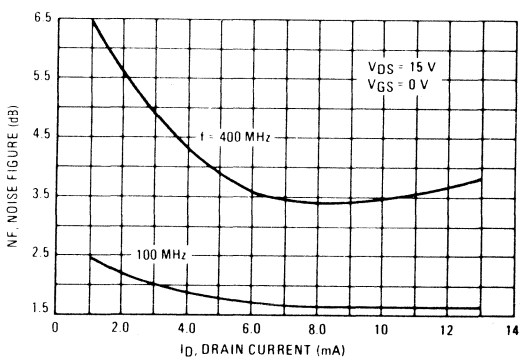
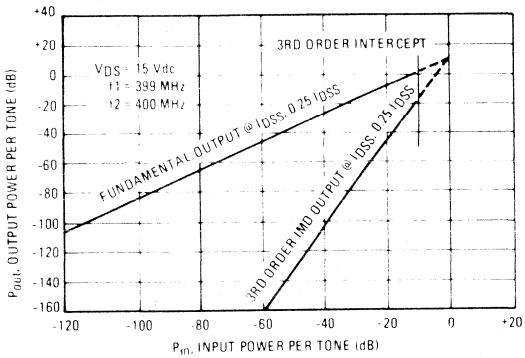


FIGURE 4 – EFFECTS OF DRAIN CURRENT



INTERMODULATION CHARACTERISTICS

FIGURE 5 – THIRD ORDER INTERMODULATION DISTORTION



COMMON SOURCE CHARACTERISTICS

ADMITTANCE PARAMETERS

(V_{DS} = 15 Vdc, $T_{channel}$ = 25°C)

FIGURE 6 – INPUT ADMITTANCE (y_{is})

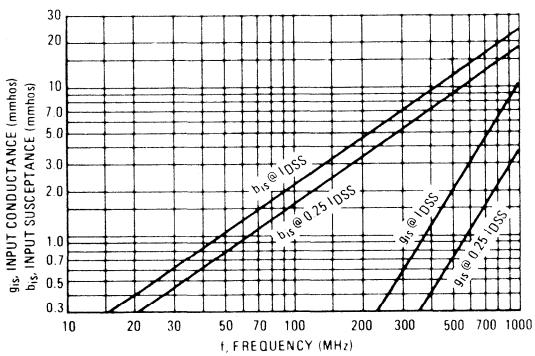


FIGURE 7 – REVERSE TRANSFER ADMITTANCE (y_{rs})

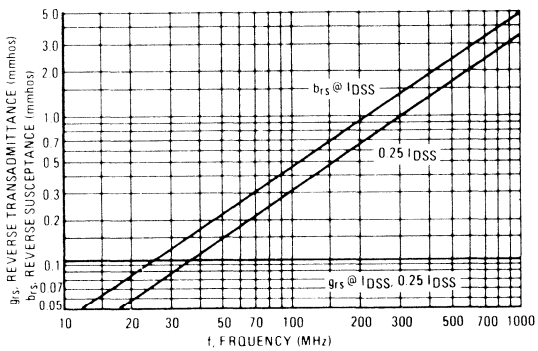


FIGURE 8 – FORWARD TRANSADMITTANCE (y_{fs})

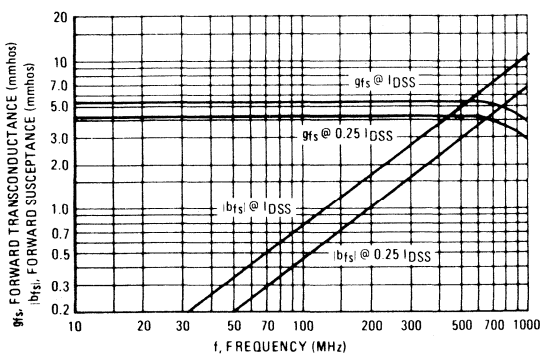
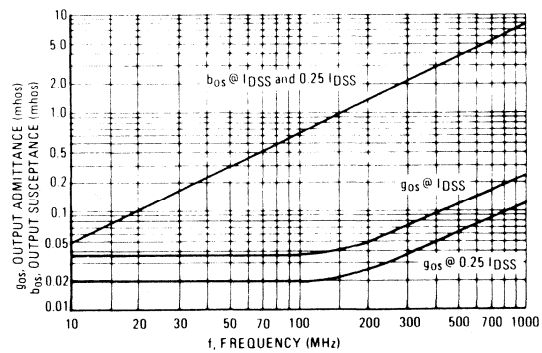


FIGURE 9 – OUTPUT ADMITTANCE (y_{os})



5

COMMON SOURCE CHARACTERISTICS

S-PARAMETERS

(V_{DS} = 15 Vdc, $T_{channel}$ = 25°C, Data Points in MHz)

FIGURE 10 – S_{11s}

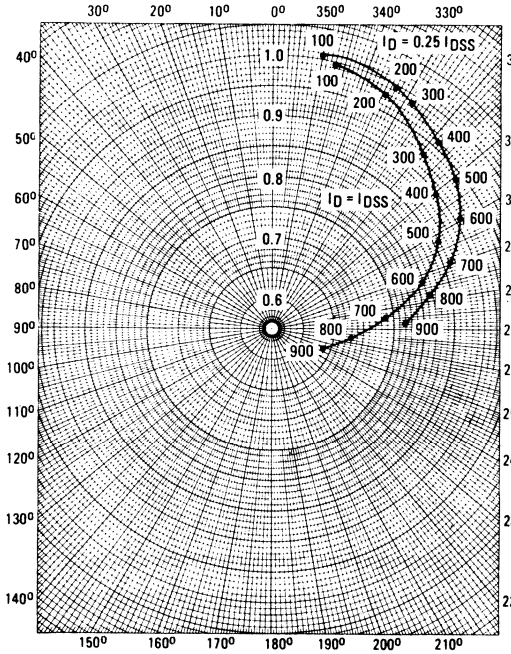


FIGURE 11 – S_{12s}

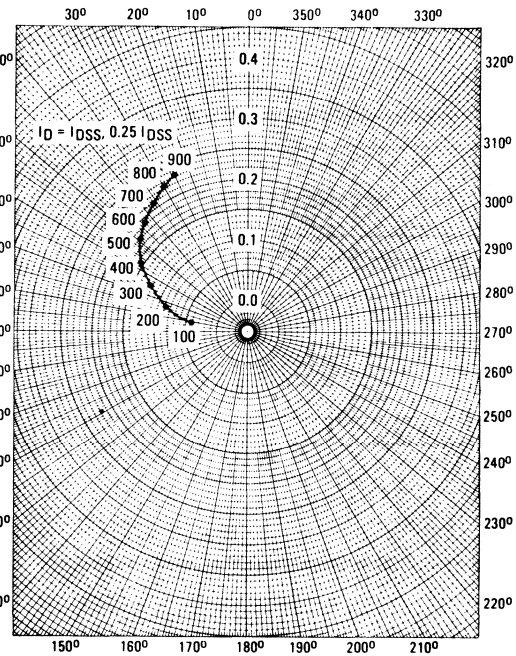


FIGURE 12 – S_{21s}

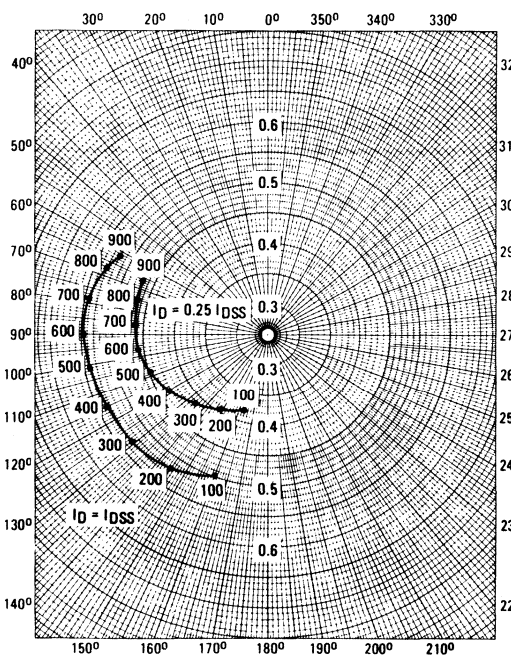
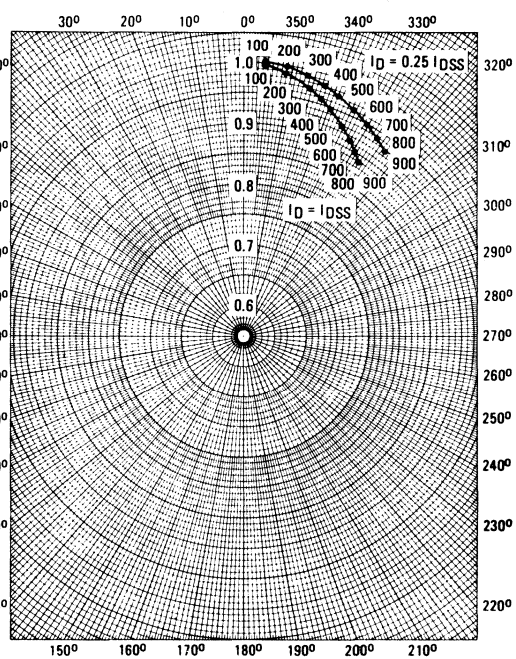


FIGURE 13 – S_{22s}



COMMON GATE CHARACTERISTICS

ADMITTANCE PARAMETERS

(V_{DG} = 15 Vdc, $T_{channel}$ = 25°C)

FIGURE 14 – INPUT ADMITTANCE (y_{ig})

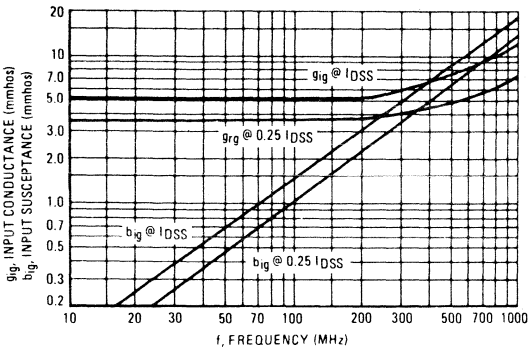


FIGURE 15 – REVERSE TRANSFER ADMITTANCE (y_{rg})

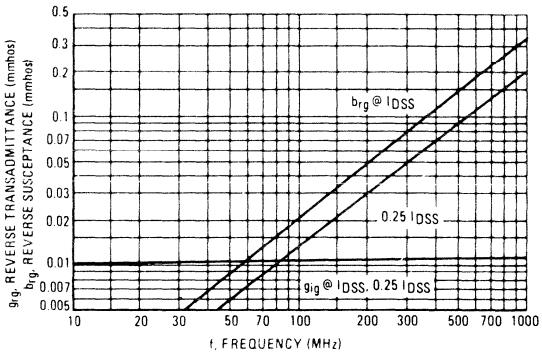


FIGURE 16 – FORWARD TRANSFER ADMITTANCE (y_{fg})

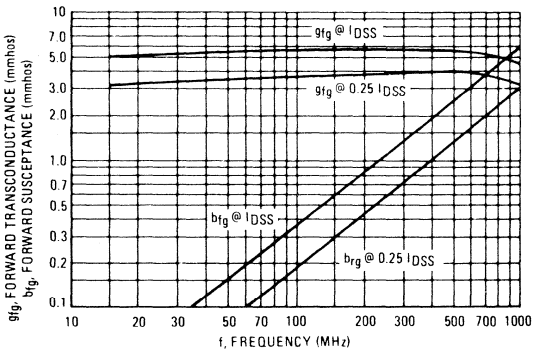
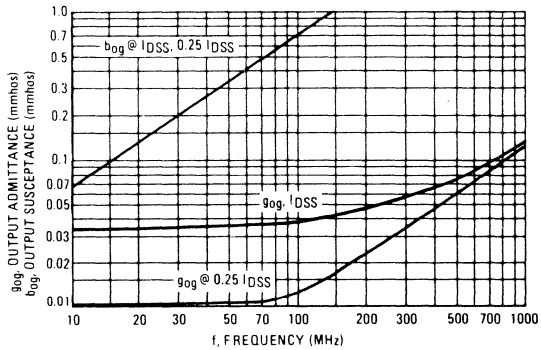


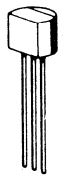
FIGURE 17 – OUTPUT ADMITTANCE (y_{og})



5

2N5457
2N5458 • 2N5459

Silicon N-channel junction field-effect transistors depletion mode (Type A) designed for general-purpose audio and switching applications.



CASE 29
(TO-92)

Drain and source may be interchanged.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	25	Vdc
Reverse Gate-Source Voltage	$V_{GS(r)}$	25	Vdc
Gate Current	I_G	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D (2)	310 2.82	mW mW/°C
Operating Junction Temperature	T_J (2)	135	°C
Storage Temperature Range	T_{stg} (2)	-65 to +150	°C

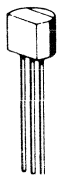
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage (I_G = -10 μAdc, V_{DS} = 0)		BV_{GSS}	25	—	—	Vdc
Gate Reverse Current (V_{GS} = -15 Vdc, V_{DS} = 0)		I_{GSS}	—	—	1.0	nAdc
(V_{GS} = -15 Vdc, V_{DS} = 0, T_A = 100°C)			—	—	200	
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 10 nAdc)	2N5457	$V_{GS(off)}$	0.5	—	6.0	Vdc
	2N5458		1.0	—	7.0	
	2N5459		2.0	—	8.0	
Gate-Source Voltage (V_{DS} = 15 Vdc, I_D = 100 μAdc)	2N5457	V_{GS}	—	2.5	—	Vdc
(V_{DS} = 15 Vdc, I_D = 200 μAdc)	2N5458		—	3.5	—	
(V_{DS} = 15 Vdc, I_D = 400 μAdc)	2N5459		—	4.5	—	
ON CHARACTERISTICS						
Zero-Gate-Voltage Drain Current (1) (V_{DS} = 15 Vdc, V_{GS} = 0)	2N5457	I_{DSS}	1.0	3.0	5.0	mAdc
	2N5458		2.0	6.0	9.0	
	2N5459		4.0	9.0	16	
DYNAMIC CHARACTERISTICS						
Forward Transfer Admittance (1) (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 kHz)	2N5457	$\|y_{fs}\|$	1000	3000	5000	μmhos
	2N5458		1500	4000	5500	
	2N5459		2000	4500	6000	
Output Admittance (1) (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 kHz)		$\|y_{os}\|$	—	10	50	μmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 MHz)		C_{iss}	—	4.5	7.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 MHz)		C_{rss}	—	1.5	3.0	pF

(1) **Pulse Test: Pulse Width ≤ 630 ms; Duty Cycle ≤ 10%**

(2) Continuous package improvements have enhanced these guaranteed Maximum Ratings as follows: P_D = 1.0 W @ T_C = 25°C. Derate above 25°C = 8.0 mW/°C, T_J = -65 to +150°C, θ_{JC} = 125° C/W.

P-channel depletion mode (Type A) junction field-effect transistors designed for use in general-purpose amplifier applications.



CASE 29
(TO-92)

MAXIMUM RATINGS

Rating	Symbol	2N5460 2N5461 2N5462	2N5463 2N5464 2N5465	Unit
Drain-Gate Voltage	V_{DG}	40	60	Vdc
Reverse Gate-Source Voltage	$V_{GS(r)}$	40	60	Vdc
Forward Gate Current	$I_{G(f)}$	10		mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D (1)	310 2.82		mW mW/°C
Storage Temperature Range	T_{stg} (1)	-65 to +150		°C
Operating Junction Temperature Range	T_J (1)	-65 to +135		°C

(1) Continuous package improvements have enhanced these guaranteed Maximum Ratings as follows: P_D = 1.0 W @ T_C = 25°C. Derate above 25°C – 8.0 mW/°C. T_J = -65 to +150°C. θ_{JC} = 125°C/W.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage (I_G = 10 μAdc, V_{DS} = 0)	2N5460, 2N5461, 2N5462 2N5463, 2N5464, 2N5465	$V_{(BR)GSS}$	40 60	- -	- -	Vdc
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 1.0 μAdc)	2N5460, 2N5463 2N5461, 2N5464 2N5462, 2N5465	$V_{GS(off)}$	0.75 1.0 1.8	- - -	6.0 7.5 9.0	Vdc
Gate Reverse Current (V_{GS} = 20 Vdc, V_{DS} = 0)	2N5460, 2N5461, 2N5462	I_{GSS}	-	-	5.0	nAdc
(V_{GS} = 30 Vdc, V_{DS} = 0)	2N5463, 2N5464, 2N5465		-	-	5.0	
(V_{GS} = 20 Vdc, V_{DS} = 0, T_A = 100°C)	2N5460, 2N5461, 2N5462		-	-	1.0	μAdc
(V_{GS} = 30 Vdc, V_{DS} = 0, T_A = 100°C)	2N5463, 2N5464, 2N5465		-	-	1.0	
ON CHARACTERISTICS						
Zero-Gate Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0)	2N5460, 2N5463 2N5461, 2N5464 2N5462, 2N5465	I_{DSS}	1.0 2.0 4.0	- - -	5.0 9.0 16	mAdc
Gate-Source Voltage (V_{DS} = 15 Vdc, I_D = 0.1 mAdc)	2N5460, 2N5463	V_{GS}	0.5	-	4.0	Vdc
(V_{DS} = 15 Vdc, I_D = 0.2 mAdc)	2N5461, 2N5464		0.8	-	4.5	
(V_{DS} = 15 Vdc, I_D = 0.4 mAdc)	2N5462, 2N5465		1.5	-	6.0	
SMALL-SIGNAL CHARACTERISTICS						
Forward Transadmittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5460, 2N5463 2N5461, 2N5464 2N5462, 2N5465	$\lvert y_{fs} \rvert$	1000 1500 2000	- - -	4000 5000 6000	μmhos
Output Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)		$\lvert y_{os} \rvert$	-	-	75	μmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	-	5.0	7.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	-	1.0	2.0	pF
Common-Source Noise Figure (V_{DS} = 15 Vdc, V_{GS} = 0, R_G = 1.0 Megohm, f = 100 Hz, BW = 1.0 Hz)		NF	-	1.0	2.5	dB
Equivalent Short-Circuit Input Noise Voltage (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 Hz, BW = 1.0 Hz)		e_n	-	60	115	nV/√Hz

5

DRAIN CURRENT versus GATE SOURCE VOLTAGE

FIGURE 1 – 2N5460 and 2N5463

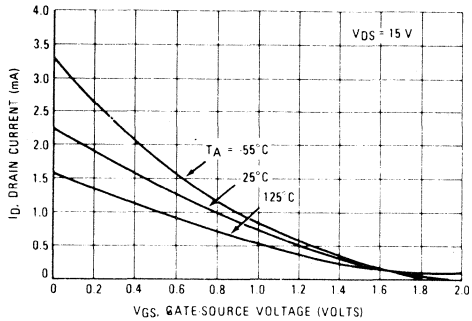


FIGURE 2 – 2N5461 and 2N5464

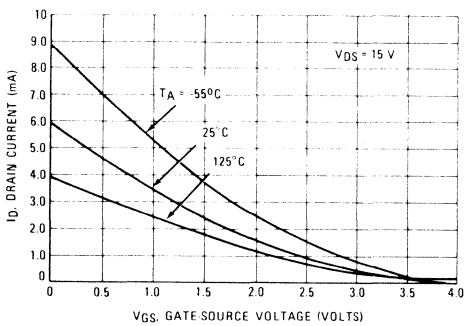
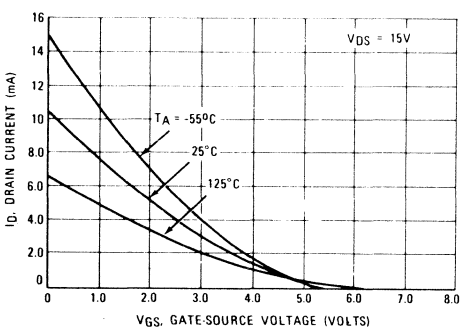


FIGURE 3 – 2N5462 and 2N5465



FORWARD TRANSFER ADMITTANCE versus DRAIN CURRENT

FIGURE 4 – 2N5460 and 2N5463

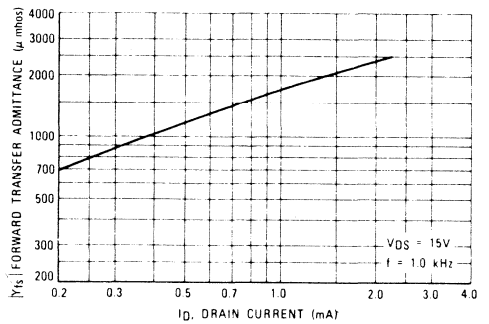


FIGURE 5 – 2N5461 and 2N5464

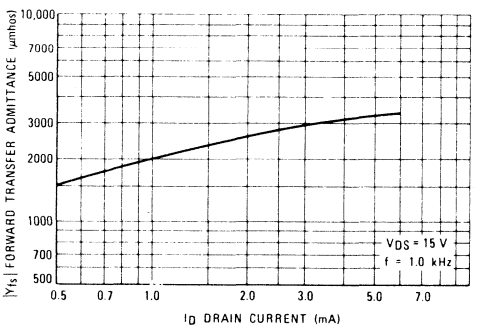


FIGURE 6 – 2N5462 and 2N5465

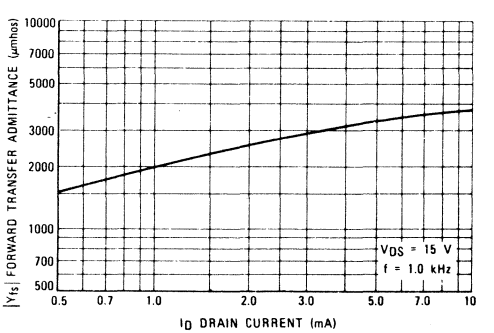


FIGURE 7 – OUTPUT RESISTANCE VERSUS DRAIN CURRENT

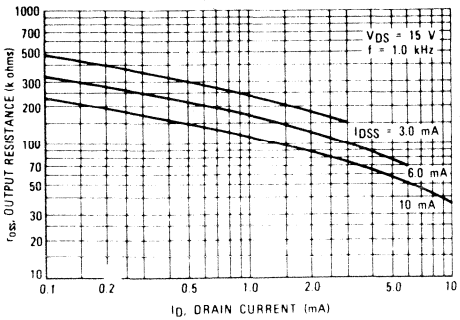


FIGURE 8 – CAPACITANCE VERSUS DRAIN-SOURCE VOLTAGE

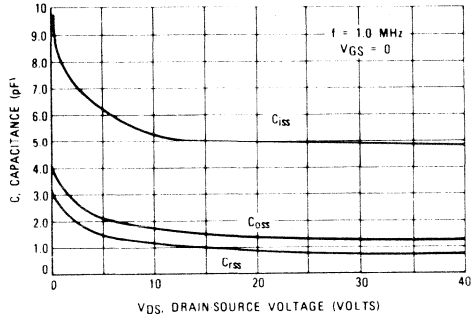


FIGURE 9 – NOISE FIGURE VERSUS FREQUENCY

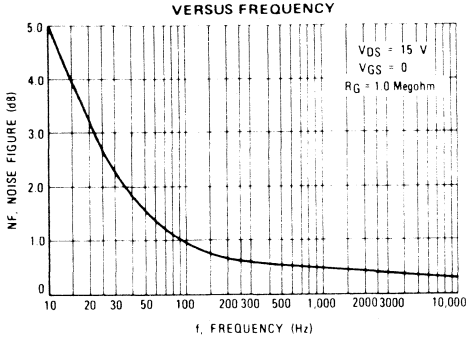


FIGURE 10 – NOISE FIGURE VERSUS SOURCE RESISTANCE

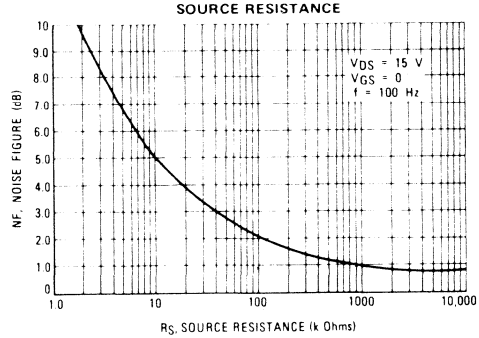
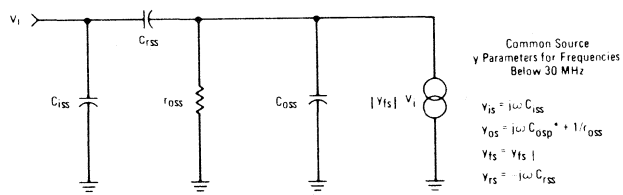


FIGURE 11 – EQUIVALENT LOW FREQUENCY CIRCUIT



*C_{osp} is C_{oss} in parallel with Series Combination of C_{iss} and C_{rss}

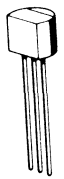
NOTE:

1. Graphical data is presented for dc conditions. Tabular data is given for pulsed conditions (Pulse Width = 630 ms, Duty Cycle = 10%)

5

2N5484 thru 2N5486

N-channel depletion mode (Type A) junction field-effect transistors designed for VHF/UHF amplifier applications.



CASE 29
(TO-92)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Gate Voltage	V_{DG}	25	Vdc
Reverse Gate-Source Voltage	$V_{GS(r)}$	25	Vdc
Drain Current	I_D	30	mAdc
Forward Gate Current	$I_{G(f)}$	10	mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D (1)	310 2.82	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg} (1)	-65 to +150	°C

(1) Continuous package improvements have enhanced these guaranteed Maximum Ratings as follows. P_D = 1.0 W @ T_C = 25°C. Derate above 25°C – 8.0 mW/°C. T_J = -65 to +150°C. θ_{JC} = 125° C/W

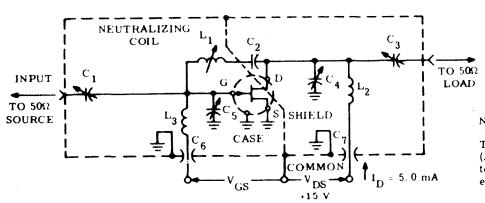
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage (I_G = -1.0 μAdc, V_{DS} = 0)		$V_{(BR)GSS}$	25	-	-	Vdc
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 10 nAdc)	2N5484 2N5485 2N5486	$V_{GS(off)}$	0.3 0.5 2.0	- - -	3.0 4.0 6.0	Vdc
Gate Reverse Current (V_{GS} = -20 Vdc, V_{DS} = 0)		I_{GSS}	-	-	1.0	nAdc
(V_{GS} = -20 Vdc, V_{DS} = 0, T_A = 100°C)			-	-	0.2	μAdc
ON CHARACTERISTICS						
Zero-Gate Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0)	2N5484 2N5485 2N5486	I_{DSS}	1.0 4.0 8.0	- - -	5.0 10 20	mAdc

ELECTRICAL CHARACTERISTICS (continued)

Characteristic		Symbol	Min	Typ	Max	Unit
SMALL-SIGNAL CHARACTERISTICS						
Forward Transadmittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5484	Y_{fs}	3000	-	6000	μmhos
	2N5485		3500	-	7000	
	2N5486		4000	-	8000	
Forward Transconductance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)	2N5484	$Re(y_{fs})$	2500	-	-	μmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 400 MHz)	2N5485		3000	-	-	
	2N5486		3500	-	-	
Output Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5484	Y_{os}	-	-	50	μmhos
	2N5485		-	-	60	
	2N5486		-	-	75	
Output Conductance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)	2N5484	$Re(y_{os})$	-	-	75	μmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 400 MHz)	2N5485, 2N5486		-	-	100	
Input Conductance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)	2N5484	$Re(y_{is})$	-	-	100	μmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 400 MHz)	2N5485, 2N5486		-	-	1000	
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	-	-	5.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	-	-	1.0	pF
Output Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{oss}	-	-	2.0	pF
Common-Source Noise Figure		NF				dB
(V_{DS} = 15 Vdc, V_{GS} = 0, R_G = 1.0 Megohm, f = 1.0 kHz)	All Types		-	-	2.5	
(V_{DS} = 15 Vdc, I_D = 1.0 mAdc, R_G = 1.0 k ohm, f = 100 MHz)	2N5484		-	-	3.0	
(V_{DS} = 15 Vdc, I_D = 1.0 mAdc, R_G = 1.0 k ohm, f = 200 MHz)	2N5484		-	4.0	-	
(V_{DS} = 15 Vdc, I_D = 4.0 mAdc, R_G = 1.0 k ohm, f = 100 MHz)	2N5485, 2N5486		-	-	2.0	
(V_{DS} = 15 Vdc, I_D = 4.0 mAdc, R_G = 1.0 k ohm, f = 400 MHz)	2N5485, 2N5486		-	-	4.0	
Insertion Power Gain		G_{ps}				dB
(V_{DS} = 15 Vdc, I_D = 1.0 mAdc, f = 100 MHz)	2N5484		16	-	25	
(V_{DS} = 15 Vdc, I_D = 1.0 mAdc, f = 200 MHz)	2N5484		-	14	-	
(V_{DS} = 15 Vdc, I_D = 4.0 mAdc, f = 100 MHz)	2N5485, 2N5486		18	-	30	
(V_{DS} = 15 Vdc, I_D = 4.0 mAdc, f = 400 MHz)	2N5485, 2N5486		10	-	20	

FIGURE 1 – 100 MHz AND 400 MHz NEUTRALIZED AMPLIFIER



ADJUST V_{GS} FOR
I_D = 5.0 mA
V_{GS} < 0 VOLTS

NOTE:

The noise source is a hot-cold body (AIL type 70 or equivalent) with a test receiver (AIL type 136 or equivalent).

Reference Designation	VALUE 100 MHz	VALUE 400 MHz
C_1	1-12 pF	0.8-8.0 pF
C_2	1000 pF	27 pF
C_3	1-12 pF	0.8-8.0 pF
C_4	1-12 pF	0.8-8.0 pF
C_5	1-12 pF	0.8-8.0 pF
C_6	0.0015 μF	0.001 μF
C_7	0.0015 μF	0.001 μF
L_1	3.0 μH*	0.2 μH**
L_2	0.25 μH*	0.03 μH**
L_3	0.14 μH*	0.022 μH**

* L_1 17 turns (approximately - depending upon circuit layout), AWG #28 enameled copper wire, close wound on 9/32" ceramic coil form. Tuning provided by a powdered iron slug.

L_2 4 1/2 turns, AWG #18 enameled copper wire, 5/16" long, 3/8" I. D. (AIR CORE).

L_3 3 1/2 turns, AWG #18 enameled copper wire, 1/4" long, 3/8" I. D. (AIR CORE).

** L_1 6 turns (approximately - depending upon circuit layout), AWG #24 enameled copper wire, close wound on 7/32" ceramic coil form. Tuning provided by an aluminum slug.

L_2 1 turn, AWG #16 enameled copper wire, 3/8" I. D. (AIR CORE).

L_3 1 2 turn, AWG #16 enameled copper wire, 1/4" I. D. (AIR CORE).

5

2N5638
2N5639 • 2N5640

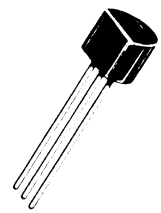
N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS

. . . depletion mode (Type A) Junction Field-Effect Transistors designed for chopper and high-speed switching applications.

- Low Drain-Source "ON" Resistance
  $r_{ds(on)}$ = 30 Ohms (2N5638)
  60 Ohms (2N5639)
  100 Ohms (2N5640)
- Low Reverse Transfer Capacitance
  C_{rss} = 4.0 pF (Max) @ f = 1.0 MHz
- Fast Switching Characteristics –
  t_r = 5.0 ns (Max) (2N5638)

N-CHANNEL
JUNCTION
FIELD-EFFECT
TRANSISTORS

TYPE A

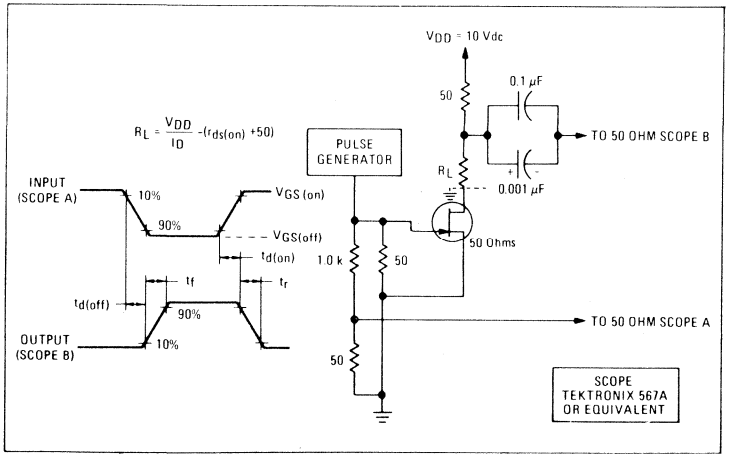


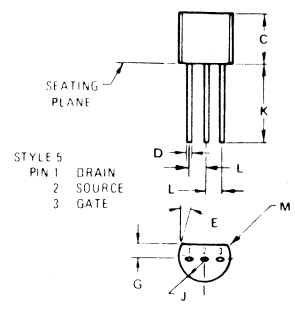
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	30	Vdc
*Drain-Gate Voltage	V_{DG}	30	Vdc
*Reverse Gate-Source Voltage	V_{GSR}	30	Vdc
*Forward Gate Current	I_{GF}	10	mAdc
*Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	310 2.82	mW mW/°C
*Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature Range	T_J	-65 to +135	°C

*Indicates JEDEC Registered Data.

FIGURE 1 – SWITCHING TIMES TEST CIRCUIT





DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
C	0.175	0.185	4.450	4.700
D	0.016	0.019	0.407	0.482
E	5° NOM		5° NOM	
G	0.045	0.055	1.150	1.390
J	0.085	0.095	2.160	2.420
K	0.500		12.700	
L	0.050 TP		1.270 TP	
M	0.003	0.013	0.076	0.330

CASE 29(5)
TO-92

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

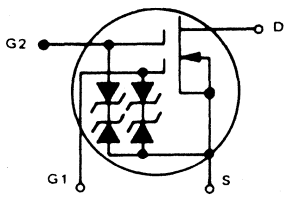
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Gate-Source Breakdown Voltage (I_G = 10 μAdc, V_{DS} = 0)		$V_{(BR)GSS}$	30	–	Vdc
Gate Reverse Current		I_{GSS}			
(V_{GS} = -15 Vdc, V_{DS} = 0)			–	1.0	nAdc
(V_{GS} = -15 Vdc, V_{DS} = 0, T_A = 100°C)			–	1.0	μAdc
Drain Cutoff Current		$I_{D(off)}$			
(V_{DS} = 15 Vdc, V_{GS} = -12 Vdc)	2N5638		–	1.0	μAdc
(V_{DS} = 15 Vdc, V_{GS} = -8.0 Vdc)	2N5639		–	1.0	
(V_{DS} = 15 Vdc, V_{GS} = -6.0 Vdc)	2N5640		–	1.0	
(V_{DS} = 15 Vdc, V_{GS} = -12 Vdc, T_A = 100°C)	2N5638		–	1.0	μAdc
(V_{DS} = 15 Vdc, V_{GS} = -8.0 Vdc, T_A = 100°C)	2N5639		–	1.0	
(V_{DS} = 15 Vdc, V_{GS} = -6.0 Vdc, T_A = 100°C)	2N5640		–	1.0	
ON CHARACTERISTICS					
Zero-Gate Voltage Drain Current (Note 1)		I_{DSS}			mAdc
(V_{DS} = 20 Vdc, V_{GS} = 0)	2N5638		50	–	
	2N5639		25	–	
	2N5640		5.0	–	
Drain-Source "ON" Voltage		$V_{DS(on)}$			Vdc
(I_D = 12 mAdc, V_{GS} = 0)	2N5638		–	0.5	
(I_D = 6.0 mAdc, V_{GS} = 0)	2N5639		–	0.5	
(I_D = 3.0 mAdc, V_{GS} = 0)	2N5640		–	0.5	
Static Drain-Source "ON" Resistance		$r_{DS(on)}$			Ohms
(I_D = 1.0 mAdc, V_{GS} = 0)	2N5638		–	30	
	2N5639		–	60	
	2N5640		–	100	
SMALL-SIGNAL CHARACTERISTICS					
Static Drain-Source "ON" Resistance		$r_{ds(on)}$			Ohms
(V_{GS} = 0, I_D = 0, f = 1.0 kHz)	2N5638		–	30	
	2N5639		–	60	
	2N5640		–	100	
Input Capacitance (V_{DS} = 0, V_{GS} = -12 Vdc, f = 1.0 MHz)		C_{iss}	–	10	pF
Reverse Transfer Capacitance (V_{DS} = 0, V_{GS} = -12 Vdc, f = 1.0 MHz)		C_{rss}	–	4.0	pF
SWITCHING CHARACTERISTICS (Figure 1)					
Turn-On Delay Time	V_{DD} = 10 Vdc, $V_{GS(on)}$ = 0, $V_{GS(off)}$ = -10 Vdc, R_G = 50 ohms	$I_{D(on)}$ = 12 mAdc 2N5638	$t_{d(on)}$	–	4.0	ns
		6.0 mAdc 2N5639		–	6.0	
		3.0 mAdc 2N5640		–	8.0	
Rise Time		$I_{D(on)}$ = 12 mAdc 2N5638	t_r	–	5.0	ns
		6.0 mAdc 2N5639		–	8.0	
		3.0 mAdc 2N5640		–	10	
Turn-Off Delay Time		$I_{D(on)}$ = 12 mAdc 2N5638	$t_{d(off)}$	–	5.0	ns
		6.0 mAdc 2N5639		–	10	
		3.0 mAdc 2N5640		–	15	
Fall Time		$I_{D(on)}$ = 12 mAdc 2N5638	t_f	–	10	ns
		6.0 mAdc 2N5639		–	20	
		3.0 mAdc 2N5640		–	30	

*Indicates JEDEC Registered Data.

Note 1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 3.0%.

5

3N201
3N202 • 3N203

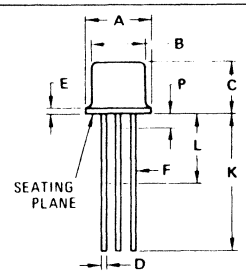


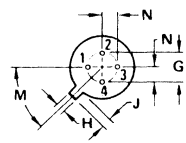
N-CHANNEL
DUAL GATE
MOS FIELD-EFFECT
TRANSISTORS

N-CHANNEL DUAL-GATE SILICON-NITRIDE PASSIVATED MOS FIELD-EFFECT TRANSISTORS

. . . depletion mode dual gate transistors designed for VHF amplifier and mixer applications.

- 3N201 – VHF Amplifier
  3N202 – VHF Mixer
  3N203 – IF Amplifier
- Low Reverse Transfer Capacitance –
  C_{rss} = 0.03 pF (Max)
- High Forward Transfer Admittance –
  $|y_{fs}|$ = 8.0 - 20 mmhos – 3N201, 3N202
  = 7.0 - 15 mmhos – 3N203
- Diode Protected Gates





STYLE 9
PIN 1. DRAIN
2 GATE 2
3 GATE 1
4 SOURCE, SUBSTRATE AND CASE

***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Drain – Source Voltage	V_{DS}	25	Vdc
Drain–Gate Voltage	V_{DG1} V_{DG2}	30 30	Vdc Vdc
Gate Current	I_{G1} I_{G2}	±10 ±10	mAdc mAdc
Drain Current – Continuous	I_D	50	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	360 2.4	mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.2 8.0	Watt mW/°C
Storage Channel Temperature Range	T_{stg}	-65 to +200	°C
Junction Temperature Range	T_J	-65 to +175	°C
Lead Temperature, 1/16" From Seated Surface for 10 Seconds	T_L	300	°C

*Indicates JEDEC Registered Data.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03
TO-72

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (I_D = 10 μAdc, V_S = 0, V_{G1S} = V_{G2S} = -5.0 Vdc)	$V_{(BR)DSX}$	25	–	–	Vdc
Gate 1 – Source Breakdown Voltage (1) (I_{G1} = ±10 mAdc, V_{G2S} = V_{DS} = 0)	$V_{(BR)G1SO}$	±6.0	–	±30	Vdc
Gate 2 – Source Breakdown Voltage (1) (I_{G2} = ± 10 mAdc, V_{G1S} = V_{DS} = 0)	$V_{(BR)G2SO}$	±6.0	–	±30	Vdc
Gate 1 to Source Cutoff Voltage (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 20 μAdc)	$V_{G1S(off)}$	-0.5	-1.5	-5.0	Vdc
Gate 2 to Source Cutoff Voltage (V_{DS} = 15 Vdc, V_{G1S} = 0, I_D = 20 μAdc)	$V_{G2S(off)}$	-0.2	-1.4	-5.0	Vdc
Gate 1 Leakage Current	I_{G1SS}				
(V_{G1S} = ±5.0 Vdc, V_{G2S} = V_{DS} = 0)		–	±.040	±10	nAdc
(V_{G1S} = -5.0 Vdc, V_{G2S} = V_{DS} = 0, T_A = 150°C)		–	–	-10	μAdc
Gate 2 Leakage Current	I_{G2SS}				
(V_{G2S} = ±5.0 Vdc, V_{G1S} = V_{DS} = 0)		–	±.050	±10	nAdc
(V_{G2S} = -5.0 Vdc, V_{G1S} = V_{DS} = 0, T_A = 150°C)		–	–	-10	μAdc
ON CHARACTERISTICS					
Zero-Gate Voltage Drain Current (2)	I_{DSS}				mAdc
(V_{DS} = 15 Vdc, V_{G1S} = 0, V_{G2S} = 4.0 Vdc) 3N201,3N202		6.0	13	30	
3N203		3.0	11	15	
SMALL-SIGNAL CHARACTERISTICS					
Forward Transfer Admittance (3)	$\|Y_{fs}\|$				mmhos
(V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, V_{G1S} = 0, f = 1.0 kHz)					
3N201,3N202		8.0	12.8	20	
3N203		7.0	12.5	15	
Input Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = I_{DSS}, f = 1.0 MHz)	C_{iss}	–	4.3	–	pF
Output Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = I_{DSS}, f = 1.0 MHz)	C_{oss}	–	1.7	–	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 10 mAdc, f = 1.0 MHz)	C_{rss}	0.005	0.014	0.03	pF
FUNCTIONAL CHARACTERISTICS					
Noise Figure	NF				
(V_{DD} = 18 Vdc, V_{GG} = 7.0 Vdc, f = 200 MHz) (Figure 1) 3N201		–	1.8	4.5	dB
(V_{DD} = 18 Vdc, V_{GG} = 6.0 Vdc, f = 45 MHz) (Figure 3) 3N203		–	5.3	6.0	
Common Source Power Gain	G_{ps}				
(V_{DD} = 18 Vdc, V_{GG} = 7.0 Vdc, f = 200 MHz) (Figure 1) 3N201		15	20	25	dB
(V_{DD} = 18 Vdc, V_{GG} = 6.0 Vdc, f = 45 MHz) (Figure 3) 3N203		20	25	30	
(V_{DD} = 18 Vdc, f_{LO} = 245 MHz, f_{RF} = 200 MHz) (Figure 2) 3N202	G_c(5)	15	19	25	
Bandwidth	BW				
(V_{DD} = 18 Vdc, V_{GG} = 7.0 Vdc, f = 200 MHz) (Figure 1) 3N201		5.0	–	9.0	MHz
(V_{DD} = 18 Vdc, f_{LO} = 245 MHz, f_{RF} = 200 MHz) (Figure 2) 3N202		4.5	–	7.5	
(V_{DD} = 18 Vdc, V_{GG} = 6.0 Vdc, f = 45 MHz) (Figure 3) 3N203		3.0	–	6.0	
Gain Control Gate-Supply Voltage (4)	$V_{GG(GC)}$				
(V_{DD} = 18 Vdc, $-G_{ps}$ = -30 dB, f = 200 MHz) (Figure 1) 3N201		0	-1.0	-3.0	Vdc
(V_{DD} = 18 Vdc, $-G_{ps}$ = -30 dB, f = 45 MHz) (Figure 3) 3N203		0	-0.6	-3.0	

* Indicates JEDEC Registered Data.

(1) All gate breakdown voltages are measured while the device is conducting rated gate current. This ensures that the gate-voltage limiting network is functioning properly.

(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

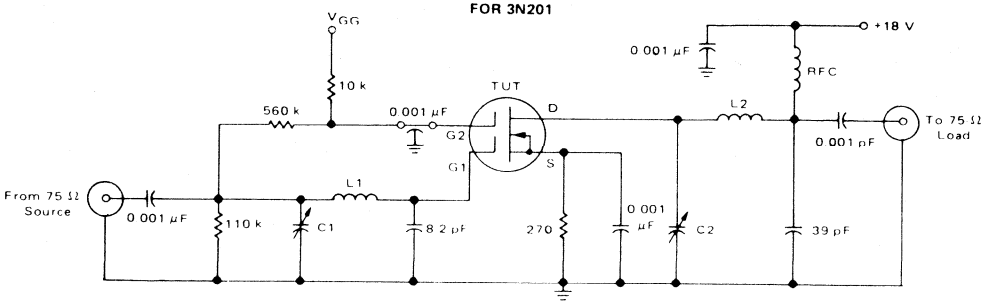
(3) This parameter must be measured with bias voltages applied for less than 5 seconds to avoid overheating.

(4) G_{ps} is defined as the change in G_{ps} from the value at V_{GG} = 7.0 volts (3N201) and V_{GG} = 6.0 volts (3N203).

(5) Power Gain Conversion

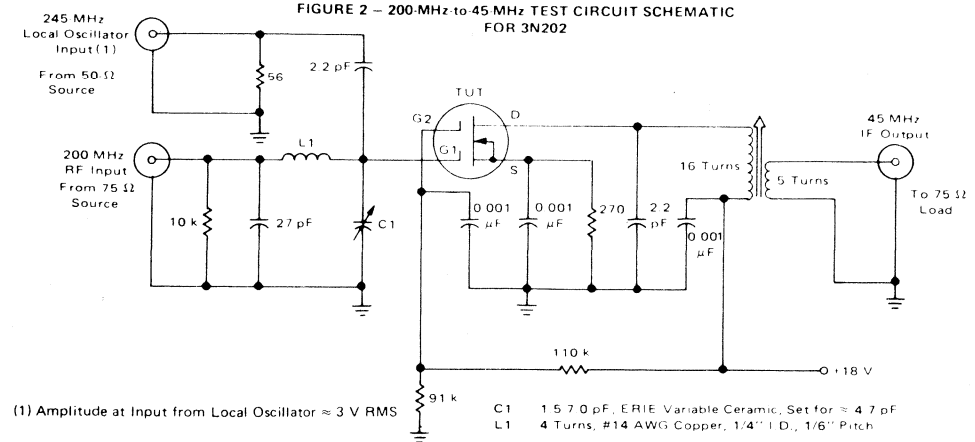
5

FIGURE 1 – 200-MHz TEST CIRCUIT SCHEMATIC FOR 3N201



C1 4.0-30 pF, ERIE Variable Ceramic, Set for ≈ 22 pF
C2 4.0-30 pF, ERIE Variable Ceramic, Set for ≈ 10 pF
L1 4 Turns, #14 AWG Copper, 1/4" I.D., 1/6" Pitch
L2 3 Turns, #14 AWG Copper, 1/4" I.D., 1/8" Pitch
RFC DELEVAN No. 153-12, 1.0 µH

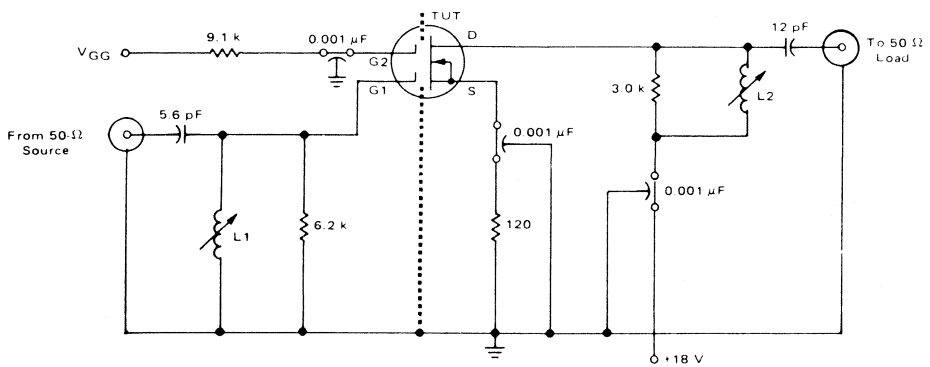
FIGURE 2 – 200-MHz-to-45-MHz TEST CIRCUIT SCHEMATIC FOR 3N202



(1) Amplitude at Input from Local Oscillator ≈ 3 V RMS

C1 1.5-7.0 pF, ERIE Variable Ceramic, Set for ≈ 4.7 pF
L1 4 Turns, #14 AWG Copper, 1/4" I.D., 1/6" Pitch

FIGURE 3 – 45-MHz TEST CIRCUIT SCHEMATIC 3N203



L1 14 Turns, #30 AWG Copper, Close-Wound 7/32" OD form with ARNOLD ENGINEERING "J" Tuning Core
L2 10 Turns, #30 AWG Copper, Close-Wound 7/32" OD form with ARNOLD ENGINEERING "J" Tuning Core

TYPICAL CHARACTERISTICS

FIGURE 4 – DRAIN CURRENT versus DRAIN to SOURCE VOLTAGE

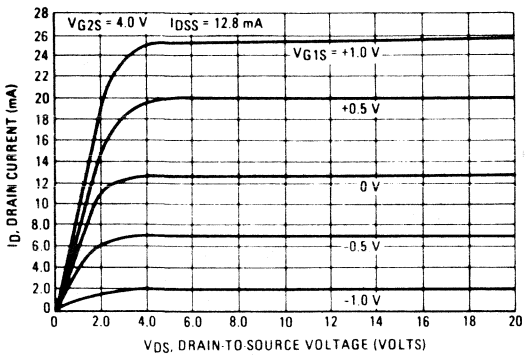


FIGURE 5 – DRAIN CURRENT versus GATE-ONE to SOURCE VOLTAGE

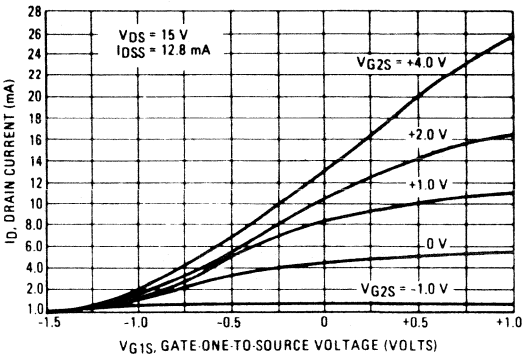


FIGURE 6 – SMALL-SIGNAL COMMON-SOURCE GATE-ONE FORWARD TRANSFER ADMITTANCE versus DRAIN CURRENT

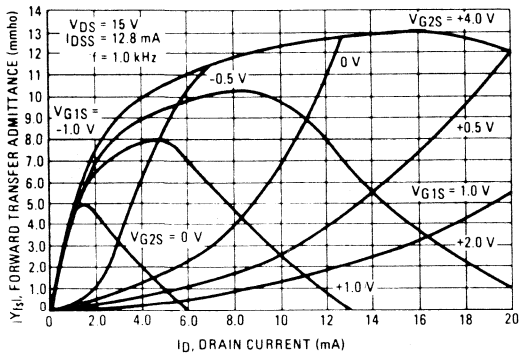


FIGURE 7 – SMALL-SIGNAL COMMON-SOURCE GATE-ONE FORWARD TRANSFER ADMITTANCE versus GATE-ONE to SOURCE VOLTAGE

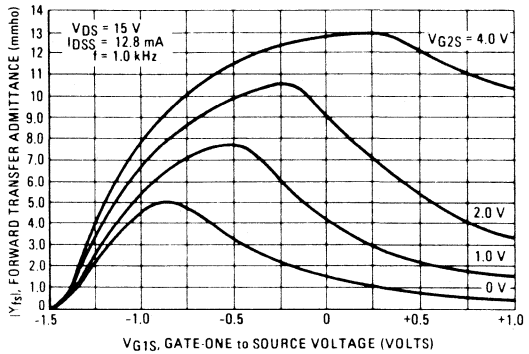


FIGURE 8 – SMALL-SIGNAL COMMON-SOURCE GATE-ONE FORWARD TRANSFER ADMITTANCE versus GATE-TWO to SOURCE VOLTAGE

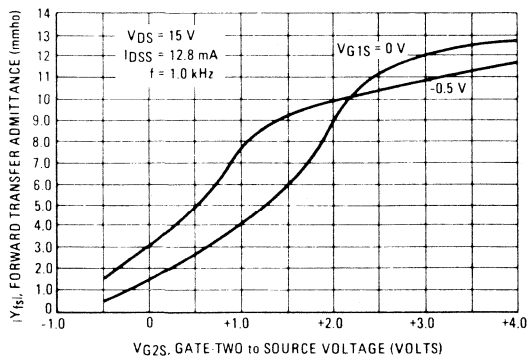
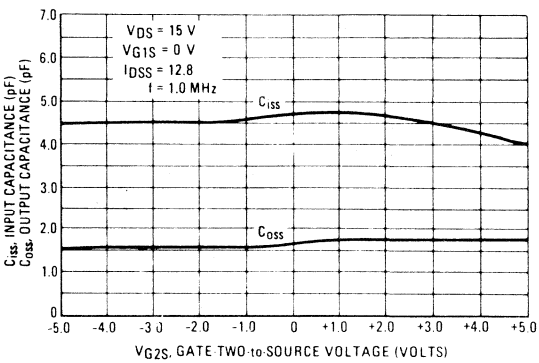


FIGURE 9 – SMALL-SIGNAL COMMON-SOURCE GATE-ONE INPUT AND OUTPUT CAPACITANCE versus GATE-TWO-to-SOURCE VOLTAGE



5

TYPICAL CHARACTERISTICS

FIGURE 10 – COMMON-SOURCE POWER GAIN AND SPOT NOISE FIGURE versus DRAIN CURRENT

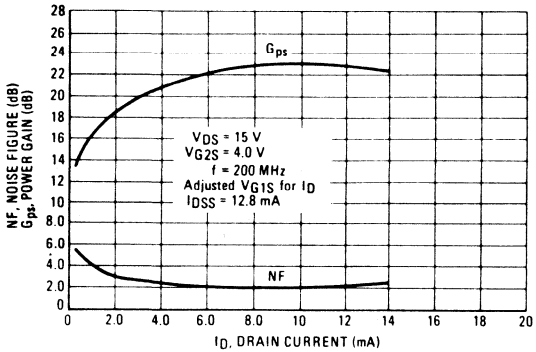


FIGURE 11 – COMMON-SOURCE POWER GAIN AND SPOT NOISE FIGURE versus GAIN CONTROL GATE-SUPPLY VOLTAGE – 3N201

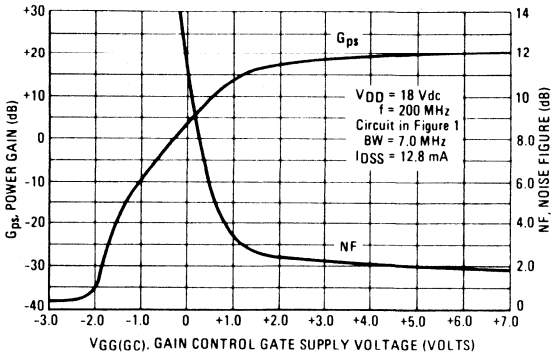


FIGURE 12 – COMMON-SOURCE POWER GAIN versus DRAIN SUPPLY CURRENT – 3N201

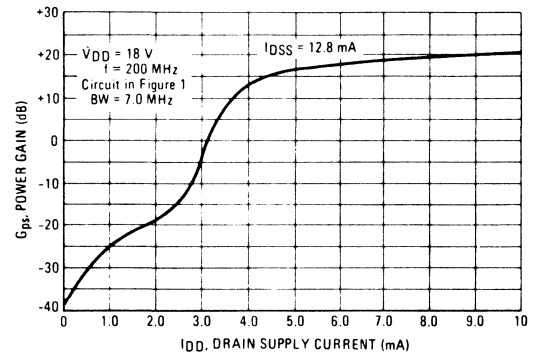


FIGURE 13 – SMALL-SIGNAL COMMON-SOURCE CONVERSION POWER GAIN versus LOCAL OSCILLATOR INPUT VOLTAGE – 3N202

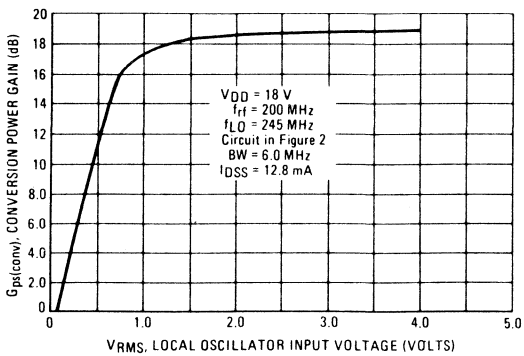
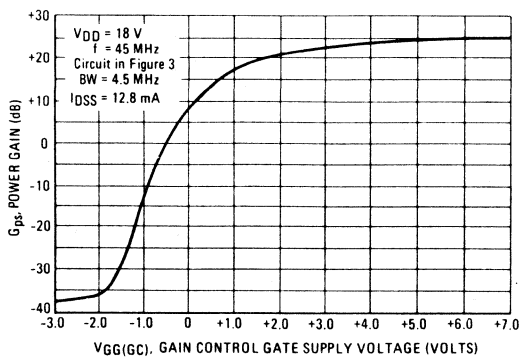


FIGURE 14 – SMALL-SIGNAL COMMON SOURCE INSERTION POWER GAIN versus GAIN CONTROL GATE-SUPPLY VOLTAGE – 3N203



TYPICAL CHARACTERISTICS

FIGURE 15 – SMALL-SIGNAL GATE ONE FORWARD TRANSFER ADMITTANCE versus FREQUENCY

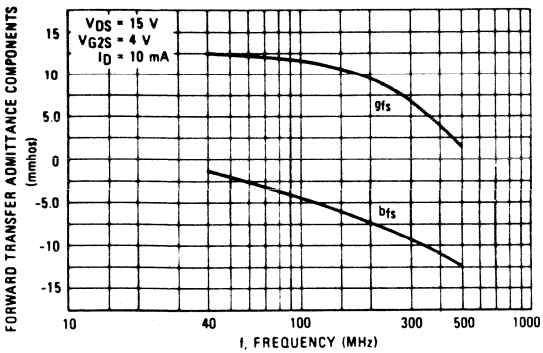


FIGURE 16 – SMALL-SIGNAL GATE ONE INPUT ADMITTANCE versus FREQUENCY

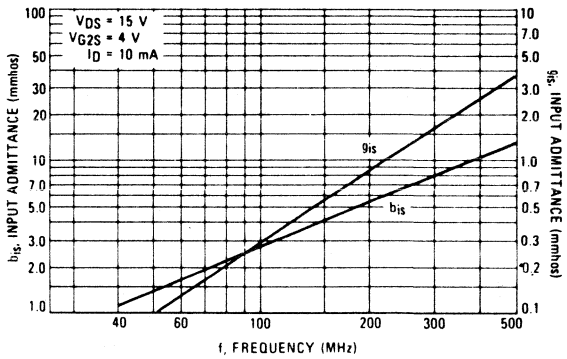
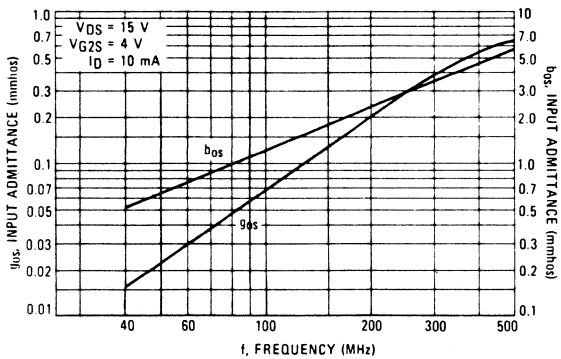


FIGURE 17 – SMALL-SIGNAL GATE ONE OUTPUT ADMITTANCE versus FREQUENCY



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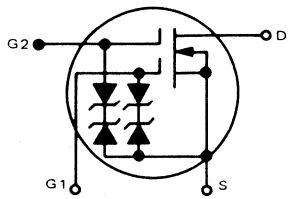
3N211
3N212 • 3N213



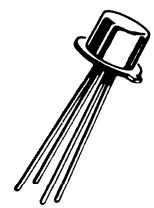
N-CHANNEL

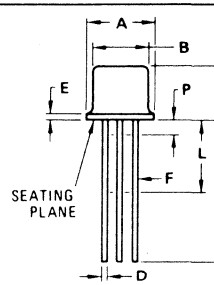
DUAL GATE
MOS FIELD-EFFECT
TRANSISTORS

N-CHANNEL DUAL GATE
SILICON-NITRIDE PASSIVATED
MOS FIELD-EFFECT TRANSISTORS

. . . high Y_{fs} depletion mode dual gate transistors designed for VHF amplifier and mixer applications.

- 3N211 – VHF Amplifier/IF Amplifier
  3N212 – VHF Mixer
  3N213 – IF Amplifier
- High Forward Transfer Admittance –
  $|Y_{fs}|$ = 17-40 mmhos – 3N211, 3N212
  = 15-35 mmhos – 3N213
- Low Reverse Transfer Capacitance –
  C_{rss} = 0.03 pF (Max)
- Diode Protected Gates





STYLE 9
PIN 1. DRAIN
2. GATE 2
3. GATE 1
4. SOURCE
SUBSTRATE
AND CASE

***MAXIMUM RATINGS**

Rating	Symbol	3N211 3N212	3N213	Unit
Drain – Source Voltage	V_{DS}	27	35	Vdc
Drain – Gate Voltage	V_{DG1}	35	40	Vdc
	V_{DG2}	35	40	Vdc
Gate Current	I_{G1}	±10		mAdc
	I_{G2}	±10		mAdc
Drain Current – Continuous	I_D	50		mAdc
Total Power Dissipation @ T_A = 25°C	P_D	360		mW
Derate above 25°C		2.4		mW/°C
Total Power Dissipation @ T_C = 25°C	P_D	1.2		Watt
Derate above 25°C		8.0		mW/°C
Storage Channel Temperature Range	T_{stg}	-65 to +200		°C
Junction Temperature Range	T_J	-65 to +175		°C
Lead Temperature, 1/16" From Seated Surface for 10 Seconds	T_L	300		°C

*Indicates JEDEC Registered Data.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03
TO 72

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Instantaneous Drain-Source Breakdown Voltage(1) (I_D = 10 μAdc, V_{G1S} = V_{G2S} = -4.0 Vdc)	3N211, 212 3N213	$V_{(BR)DSX}$	27 35	–	Vdc
Drain-Source Breakdown Voltage (I_D = 10 μAdc, V_{G1S} = V_{G2S} = -4.0 Vdc)	3N211, 212 3N213	$V_{(BR)DSX}$	25 30	–	Vdc
Gate 1 – Source Breakdown Voltage (2) (I_{G1} = ±10 mAdc, V_{G2S} = V_{DS} = 0)		$V_{(BR)G1SO}$	±6.0	–	Vdc
Gate 2 – Source Breakdown Voltage(2) (I_{G2} = ±10 mAdc, V_{G1S} = V_{DS} = 0)		$V_{(BR)G2SO}$	±6.0	–	Vdc
Gate 1 to Source Cutoff Voltage (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 20 μAdc)	3N211, 213 3N212	$V_{G1S(off)}$	-0.5 -0.5	-5.5 -4.0	Vdc
Gate 2 to Source Cutoff Voltage (V_{DS} = 15 Vdc, V_{G1S} = 0, I_D = 20 μAdc)	3N211 3N212, 213	$V_{G2S(off)}$	-0.2 -0.2	-2.5 -4.0	Vdc
Gate 1 Leakage Current (V_{G1S} = ±5.0 Vdc, V_{G2S} = V_{DS} = 0) (V_{G1S} = -5.0 Vdc, V_{G2S} = V_{DS} = 0, T_A = 150°C)		I_{G1SS}	– –	±10 -10	mAdc μAdc
Gate 2 Leakage Current (V_{G2S} = ±5.0 Vdc, V_{G1S} = V_{DS} = 0) (V_{G2S} = -5.0 Vdc, V_{G1S} = V_{DS} = 0, T_A = 150°C)		I_{G2SS}	– –	±10 -10	nAdc μAdc
ON CHARACTERISTICS					
Zero-Gate Voltage Drain Current(3) (V_{DS} = 15 Vdc, V_{G1S} = 0, V_{G2S} = 4.0 Vdc)		I_{DSS}	6.0	40	mAdc
SMALL-SIGNAL CHARACTERISTICS					
Forward Transfer Admittance(4) (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, V_{G1S} = 0, f = 1.0 kHz)	3N211, 212 3N213	$\|Y_{fs}\|$	17 15	40 35	mmhos
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 10 mAdc, f = 1.0 MHz)		C_{rss}	0.005	0.05	pF
FUNCTIONAL CHARACTERISTICS					
Noise Figure (V_{DD} = 18 Vdc, V_{GG} = 7.0 Vdc, f = 200 MHz) (Figure 1) 3N211 (V_{DD} = 24 Vdc, V_{GG} = 6.0 Vdc, f = 45 MHz) (Figure 2) 3N211, 13		NF	– –	3.5 4.0	dB
Common Source Power Gain (V_{DD} = 18 Vdc, V_{GG} = 7.0 Vdc, f = 200 MHz) (Figure 1) 3N211 (V_{DD} = 24 Vdc, V_{GG} = 6.0 Vdc, f = 45 MHz) (Figure 2) 3N211 (V_{DD} = 24 Vdc, V_{GG} = 6.0 Vdc, f = 45 MHz) (Figure 2) 3N213 (V_{DD} = 18 Vdc, f_{LO} = 245 MHz, f_{RF} = 200 MHz) (Figure 3) 3N212		G_{ps} G_c (6)	24 29 27 21	35 37 35 28	dB
Bandwidth (V_{DD} = 18 Vdc, V_{GG} = 7.0 Vdc, f = 200 MHz) (Figure 1) 3N211 (V_{DD} = 18 Vdc, f_{LO} = 245 MHz, f_{RF} = 200 MHz) (Figure 3) 3N212 (V_{DD} = 24 Vdc, V_{GG} = 6.0 Vdc, f = 45 MHz) (Figure 2) 3N211, 213		BW	5.0 4.0 3.5	12 7.0 6.0	MHz
Gain Control Gate-Supply Voltage(5) (V_{DD} = 18 Vdc, ΔG_{ps} = -30 dB, f = 200 MHz) (Figure 1) 3N211 (V_{DD} = 24 Vdc, ΔG_{ps} = -30 dB, f = 45 MHz) (Figure 2) 2N211, 213		$V_{GG(GC)}$	– –	-2.0 ±1.0	Vdc

* Indicates JEDEC Registered Data.

(1) Measured after five seconds of applied voltage

(2) All gate breakdown voltages are measured while the device is conducting rated gate current. This ensures that the gate-voltage limiting network is functioning properly.

(3) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

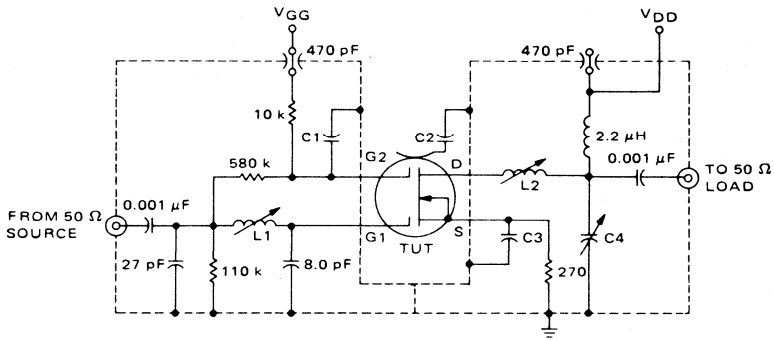
(4) This parameter must be measured with bias voltages applied for less than 5 seconds to avoid overheating. The signal is applied to gate 1 with gate 2 at ac ground.

(5) ΔG_{ps} is defined as the change in G_{ps} from the value at V_{GG} = 7.0 Volts (3N211) and V_{GG} = 6.0 Volts (3N213).

(6) Power Gain Conversion. Amplitude at input from local oscillator is adjusted for maximum G_c.

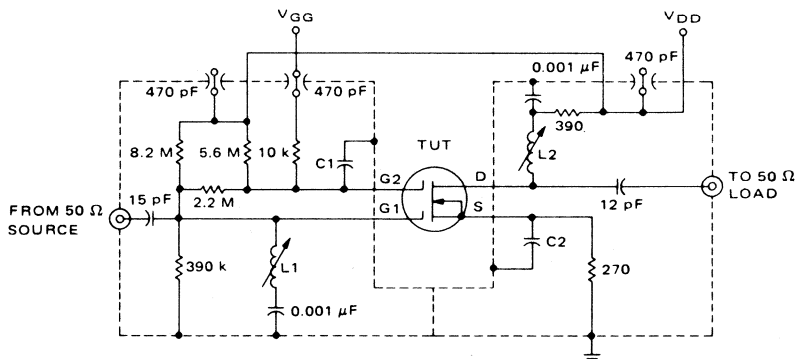
5

FIGURE 1 – 200 MHz POWER GAIN, GAIN CONTROL VOLTAGE, AND NOISE FIGURE TEST CIRCUIT FOR 3N211*



C1, C2 & C3: Leadless disc ceramic, 0.001 μF
C4: ARCO 462, 5-80 pF, or equivalent
L1: 3 Turns #18, 3/16" diameter aluminum slug
L2: 8 Turns #20, 3/16" diameter aluminum slug

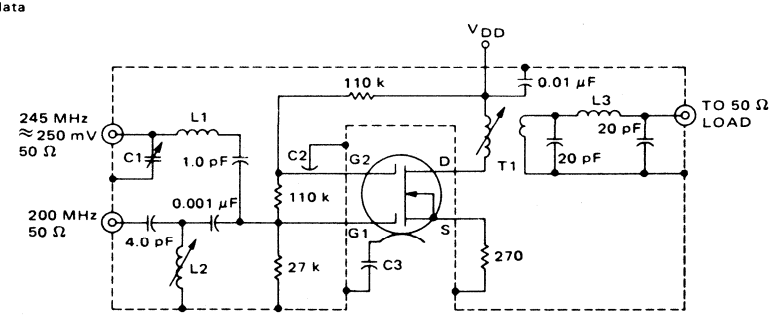
FIGURE 2 – 45-MHz POWER GAIN AND NOISE FIGURE TEST CIRCUIT FOR 3N211 AND 3N213*



C1: Leadless disc ceramic, 0.001 μF
C2: Leadless disc ceramic, 0.01 μF
L1: 8 Turns #28, 5/32" diameter form, type "J" slug
L2: 9 Turns #28, 5/32" diameter form, type "J" slug

FIGURE 3 – 200-MHz-to-45-MHz CIRCUIT FOR CONVERSION POWER GAIN FOR 3N212*

*JEDEC registered data



L1: 7 Turns #34, 1/4" diameter aluminum slug
L2: 5-1/2 Turns #20, 1/4" diameter aluminum slug
L3: 7 Turns #24, 1/4" diameter air core
C1: Arco type 462, 5-80 pF
C2: 0.001 μF leadless disc
C3: 0.01 μF leadless disc
T1: Pri: 25 Turns #30, close wound on 1/4" diameter form, type "J" slug
Sec: 4 Turns #30, centered over primary

TYPICAL CHARACTERISTICS

FIGURE 4 – DRAIN CURRENT versus DRAIN TO SOURCE VOLTAGE

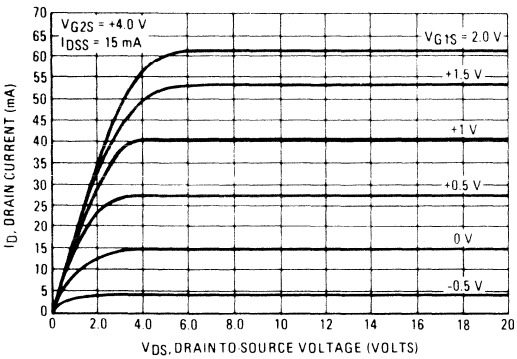
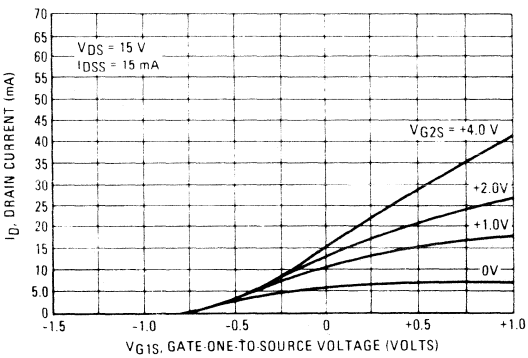


FIGURE 5 – DRAIN CURRENT versus GATE ONE TO SOURCE VOLTAGE



SMALL-SIGNAL COMMON-SOURCE PARAMETER

FIGURE 6 – FORWARD TRANSFER ADMITTANCE versus GATE-TWO TO SOURCE VOLTAGE

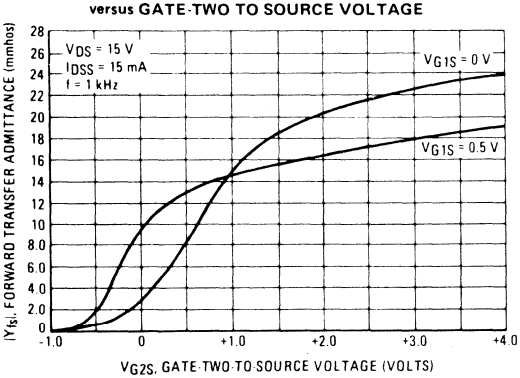


FIGURE 7 – FORWARD TRANSFER ADMITTANCE versus GATE-ONE TO SOURCE VOLTAGE

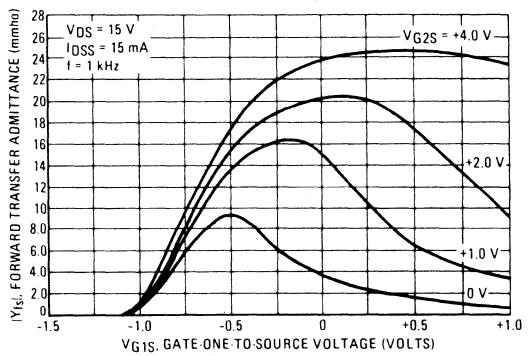


FIGURE 8 – FORWARD TRANSFER ADMITTANCE versus DRAIN CURRENT

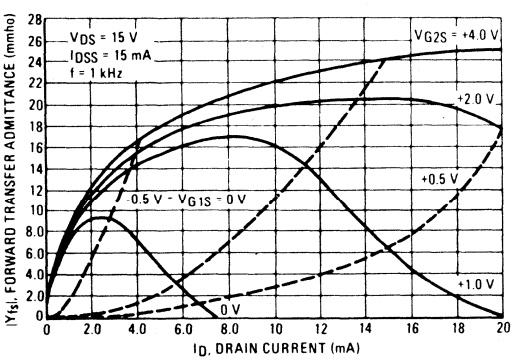
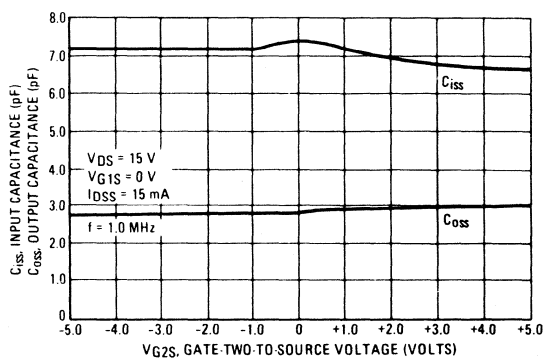


FIGURE 9 – INPUT AND OUTPUT CAPACITANCE versus GATE-TWO TO SOURCE VOLTAGE



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TYPICAL CHARACTERISTICS (continued)

FIGURE 10 – SMALL-SIGNAL GATE-ONE INPUT ADMITTANCE versus FREQUENCY

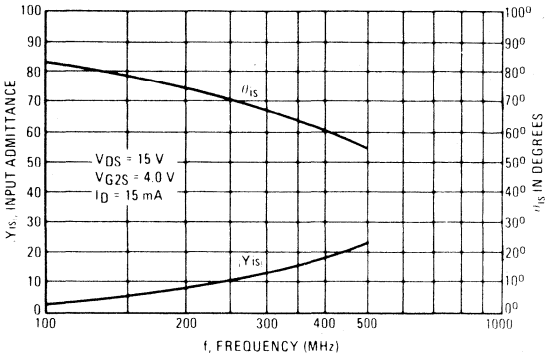


FIGURE 11 – SMALL-SIGNAL FORWARD TRANSFER ADMITTANCE versus FREQUENCY

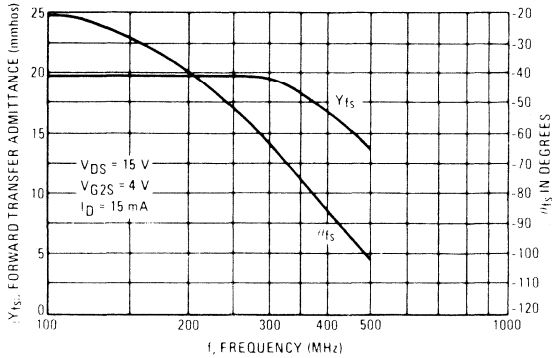


FIGURE 12 – SMALL-SIGNAL GATE-ONE REVERSE TRANSFER ADMITTANCE versus FREQUENCY

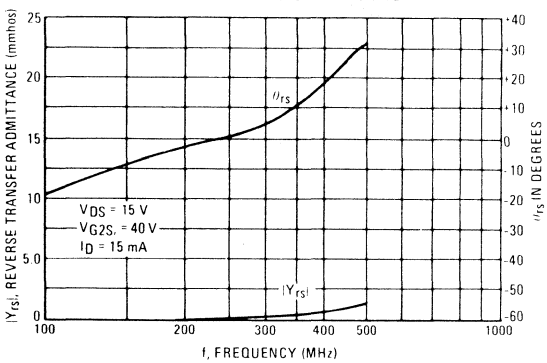


FIGURE 13 – SMALL-SIGNAL GATE-ONE OUTPUT ADMITTANCE versus FREQUENCY

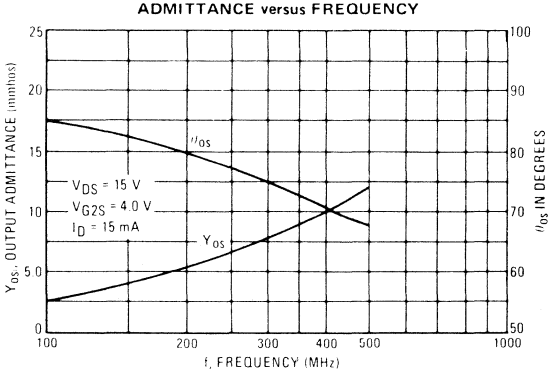


FIGURE 14 – RELATIVE SMALL-SIGNAL POWER GAIN versus GAIN CONTROL GATE SUPPLY VOLTAGE 3N211

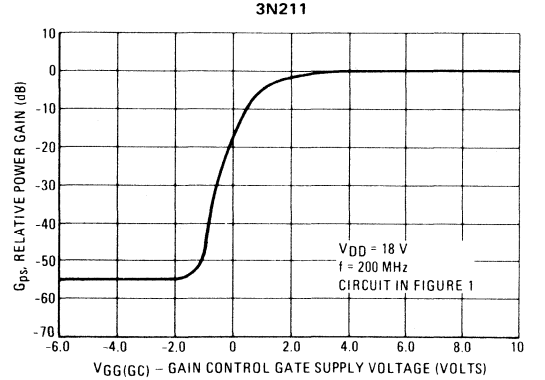
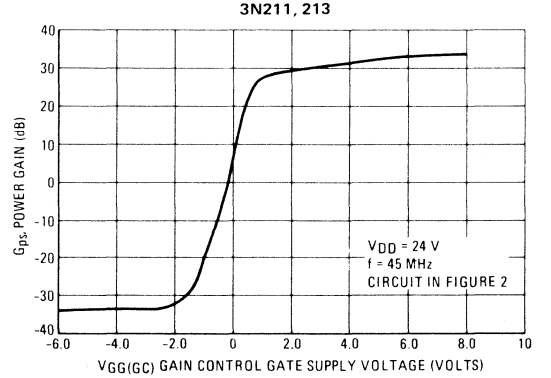


FIGURE 15 – SMALL-SIGNAL COMMON-SOURCE INSERTION POWER GAIN versus GAIN CONTROL GATE SUPPLY VOLTAGE 3N211, 213



TYPICAL CHARACTERISTICS (continued)

FIGURE 16 – COMMON SOURCE SPOT NOISE FIGURE versus GAIN CONTROL GATE SUPPLY VOLTAGE 3N211

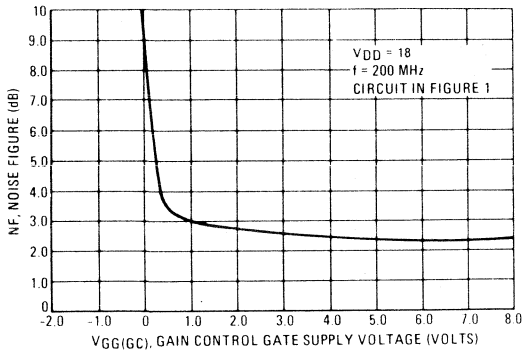
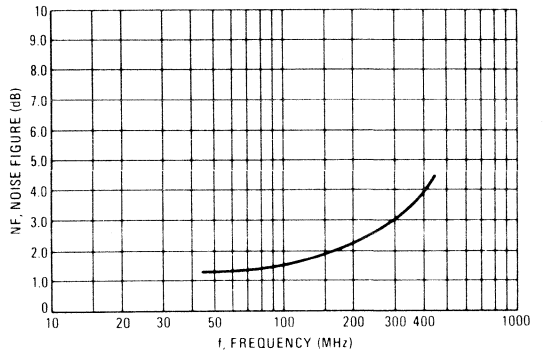


FIGURE 17 – OPTIMUM SPOT NOISE FIGURE versus FREQUENCY



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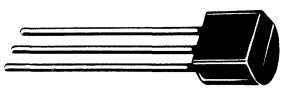
SECTION 6
THYRISTORS AND TRIGGER DEVICES

- SCR's and Triacs
- Unijunction and Programmable Unijunction transistors

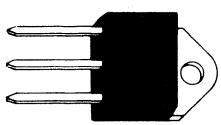
Section 6—Packages



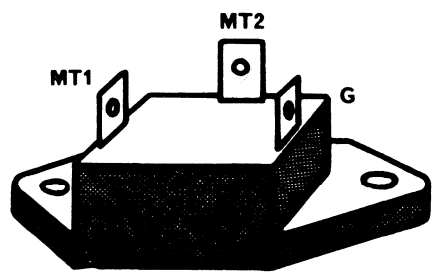
TO 92

Case 77.02

Case 22A



TO 220



*T03 base (MAC 525, A)

6

6 THYRISTORS AND TRIGGER DEVICES

Silicon Controlled Rectifiers

Device		V_{DRM} Max. A	$I_{T\ (RMS)}$ Max. A	I_{TSM} Max. A	I_{GT} Max. mA	V_{GT} Max. V	I_H Max. mA	Package	Page
MCR100 Series (3-8)	General Line Powered Applications	100-600	0,8	6	0.2	0.8	5	TO-92	6-21
MCR106 (1-4, 6, 8)	General Temp. Light, Speed control	30-600	4	25	0.2	1	5	77.02	6-23
2N5060-5064	General Relay, Lamp. Motor Applications	30-200	0.8	6	0.2	0.8	5	TO-92	6-39
2N6236-6241	General Temp. Light, Speed control	30-600	4	25	0.2	1	5	77.02	6-51
2N6394-6399 (MCR220)	General Half Wave Control	50-800	12	100	30	1-5	40	TO-220	6-25
2N6400-6405 (MCR221)	General Half Wave Control	50-800	16	160	30	1.5	40	TO-220	6-29
2N 6504-6509	General Half Wave Control	50-800	25	350	40	1.5	40	TO-220	6-61

Triacs

Device		V_{DRM} Max. V	$I_{T(RMS)}$ Max. A	I_{GT} (Max.) mA MT2− G−	MT2+ G−	MT2− G+	MT2+ G+	V_{GT} (Max.) V MT2− G−	MT2+ G−	MT2− G+	MT2+ G+	I_H Max. mA	Package	Page
BT 162	For ZVS Applications	400-600	12	40	40	-	-	1.5	1.5	-	-	30	TO-220	6-3
MAC 15,A	General Full Wave Control	200-800	15	50	75	75	50	2	2.5	2.5	2	40	TO-220	6-7
MAC 92	Low Power Full Wave Control	30-600	0.6	5	5	-	5	2.5	2.5	-	2.5	10	T092	6-11
MAC 223	General Full Wave Control	100-800	25	50	50	-	50	2.0	2.0	-	2.0	50	TO-220	6-15
MAC 228	General Full Wave Control	50-800	8	5	5	-	5	2.2	2.2	-	2.2	15	TO-220	6-18
MAC 525,A	Fast connect Power Module	100-800	25	50	75	50	50	-	-	-	-	-	*	6-20
2N6068,A,B-6075,A,B	Sensitive Gate Triggering	25-600	4	3	3	5	3	2.5	2.5	2.5	2.5	15	77.02	6-47
2N6342-49	General Full Wave Control	200-800	8	50	75	75	50	2	2.5	2.5	2	40	TO-220	6-59
2N6342A-49A	General Full Wave Control	200-800	12	50	75	75	50	2	2.5	2.5	2	40	TO-220	6-57

* = Case number not yet allocated. TO3 base

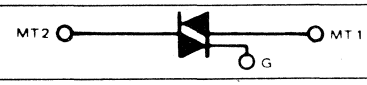
Unijunction Transistors (UJT)

Device		$V_{B_2B_1}$ Max. V	η ($V_{B_2B_1}$ = 10 V) Min.	Max.	I_P ($V_{B_2B_1}$ = 25 V) Max. μA	I_{EB_2O} (V_{B_2E} = 30 V) Max. μA	I_V ($V_{B_2B_1}$ = 20 V, R_{B_2} = 100 Ω) Min. mA	Package	Page
2N2646	Timing and Thyristor Trigger	35	0.56	0.75	5	12	4	22A	6-33
2N2647		35	0.68	0.82	2	0.2	8	22A	6-33
2N4870	Timing and Thyristor Trigger	35	0.56	0.75	5	1	2	TO-92	6-35
2N4871		35	0.7	0.85	5	1	4	TO-92	6-35

Programmable Unijunction Transistors (PUT)

Device		V_{AK} Max. V	I_T Max. mA	I_P V_S = 10 V R_G = 10K μA Max.	I_V V_S = 10 V R_G = 10K Ω μA Max.	Package	Page
2N6027	Oscillator, Timing and Thyristor Trigger	±40	200	5	70	TO-92	6-43
2N6028		±40	200	1	25	TO-92	6-43

BT162-400
BT162-600



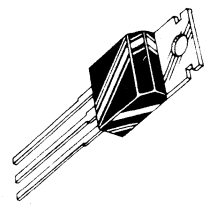
SILICON BIDIRECTIONAL THYRISTORS

. . . designed primarily for consumer and industrial applications of power control using the zero voltage switching technique, such as heater controls, hot plate controls and static switches. These devices are characterized in the second and third quadrants (negative pulse triggering) and permit the design of most circuits entirely from the information presented.

- Low gate trigger current
- Low latching current
- All diffused and glass passivated junctions for greater parameter uniformity and stability
- Small, rugged, Thermowatt▲ construction for low thermal resistance, high heat dissipation and durability
- 8 Amp. devices available as BT158-400, BT158-600.

TRIACS
(THYRISTORS)
12 AMPERES RMS

400-600 VOLTS

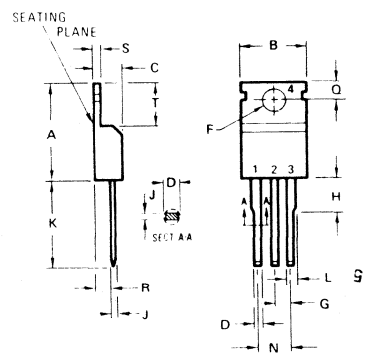


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage (T_J = −40 to +110 °C) Half Sine Wave 50 to 60 Hz, Gate Open BT162-400 BT162-600	V_{DRM}	400 600	Volts
Non Repetitive Peak Off-State Voltage[1] (T_J = −40 to +110 °C) t ≤ 10 ms, Gate Open BT162-400 BT162-600	V_{DSM}	500 700	Volts
On-State Current RMS (T_C = +80 °C) Full Cycle Sine Wave 50 to 60 Hz (T_C = +95 °C)	$I_{T(RMS)}$	12.0 6.0	Amp
Peak Surge Current (One Full Cycle, T_C = 80 °C) 60 Hz 50 Hz preceded and followed by rated current	I_{TSM}	120 110	Amp
Rate of Rise of ON-State Current (Non Repetitive), Gate Open	$\frac{dI_T}{dt}$	10	Amp/μs
Circuit Fusing Considerations (T_J = −40 to +110 °C, t = 1.0 to 10 ms)	I^2t	40	A^2s
Peak Gate Voltage	V_{GM}	10	Volts
Peak Gate Current	I_{GM}	2.0	Amp
Peak Gate Power (T_C = +80 °C, Pulse Width = 2,0 μs)	P_{GM}	20	Watts
Average Gate Power (T_C = +80 °C, t = 10 ms)	$P_{G(AV)}$	0.5	Watt
Operating Junction Temperature Range	T_J	−40 to +110	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	°C/W



STYLE 2:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H		6.35		0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

CASE 221-02
TO-220 AB

▲Trademark of Motorola Inc.

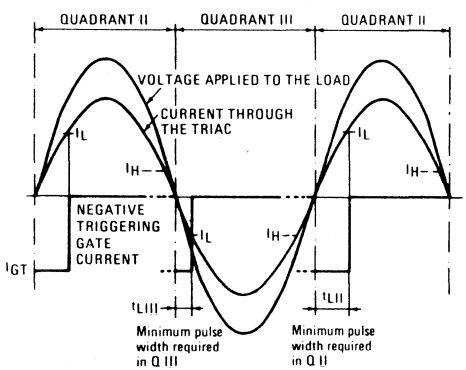
6

ELECTRICAL CHARACTERISTICS (T_C = 25 ° unless otherwise noted)

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Peak Blocking Current (Either Direction) Rated V_{DRM} @ T_J = 110°C; Gate Open	I_{DRM}			2.0	mA
Peak On-State Voltage (Either Direction) I_{TM} = 17 A Peak; Pulse Width = 1 to 2 ms, Duty Cycle ≤ 2.0 %	V_{TM}		1.3	1.75	Volts
Gate Trigger Current, Continuous dc Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 µs MT2 (+), G (−) MT2 (−), G (−) MT2 (+), G (−); MT2 (−), G (−), T_C = −40 °C	I_{GT}		 25 20	 40 40 75	mA
Gate Trigger Voltage, Continuous dc Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 µs MT2 (+), G (−) MT2 (−), G (−) MT2 (+), G (−); MT2 (−), G (−), T_C = −40 °C Main Terminal Voltage = Rated V_{DRM}, R_L = 10 K, T_J = 110 °C MT2 (+), G (−); MT2 (−), G (−)	V_{GT}	 0.2	 0.9 1.1	 1.5 1.5 2.0	Volts
Holding Current (Either Direction) Main Terminal Voltage = 12 Vdc, Gate Open } T_C = 25 °C Initiating Current = 200 mA } T_C = −40 °C	I_H		6.0	30 50	mA
Latching Current Main Terminal Voltage = 12 Vdc; R_L = variable Gate Pulse Width = 20 µs, Duty Cycle ≤ 2 % MT2 (+), G (−) } @ I_{GT} = 40 mA MT2 (−), G (−) } MT2 (+), G (−) } @ I_{GT} = 75 mA; T_C = −40 °C MT2 (−), G (−) }	I_L		 30 6.0	 60 40 100 60	mA
Critical Rate of Rise of Off-State Voltage Rated V_{DRM}, Exponential Voltage Rise, Gate Open T_C = 110 °C	dV/dt		100		V/µs

[1] Off-State Voltage up to 800 V may be applied, but triac may switch into the On-State. In that case, the Rate of Rise of On-State current should not exceed its specified maximum rating.

ZERO VOLTAGE SWITCHING MAIN CHARACTERISTICS



RECOMMENDED ZERO VOLTAGE SWITCH INTEGRATED CIRCUITS

Part Nr.	Usage	Package
UAA1004	On-Off Applications, high volume	DIL 8 pin
UAA1006	Proportional Applications; variable duty cycle modulator	DIL 16 pin

See separate Data Sheets for complete information.

FIGURE 1 – RMS CURRENT DERATING

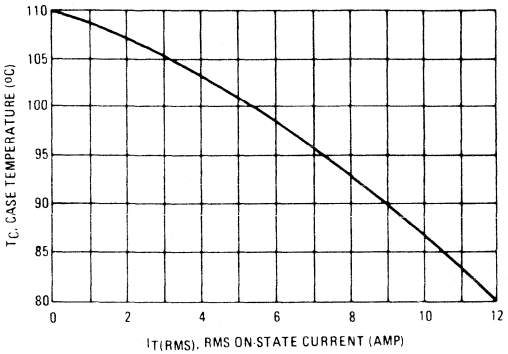


FIGURE 2 – ON-STATE POWER DISSIPATION

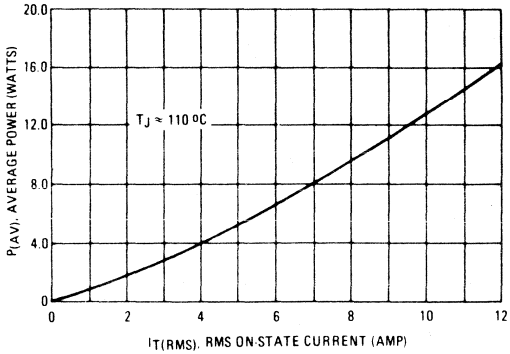


FIGURE 3 – TYPICAL GATE TRIGGER VOLTAGE

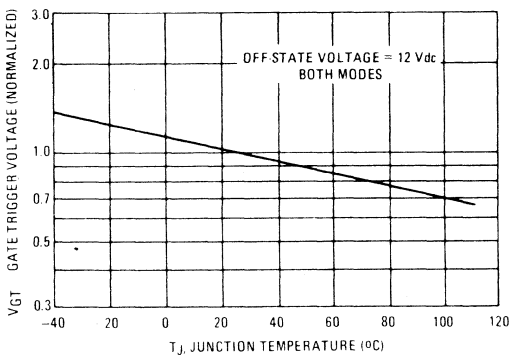


FIGURE 4 – TYPICAL GATE TRIGGER CURRENT

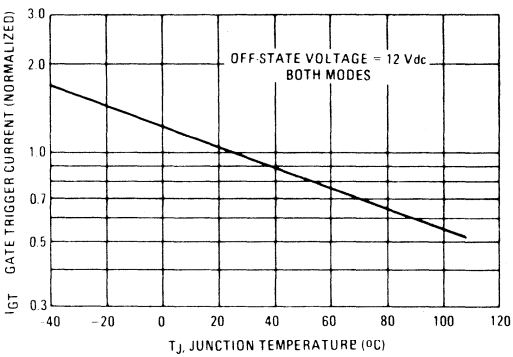


FIGURE 5 – TYPICAL HOLDING CURRENT

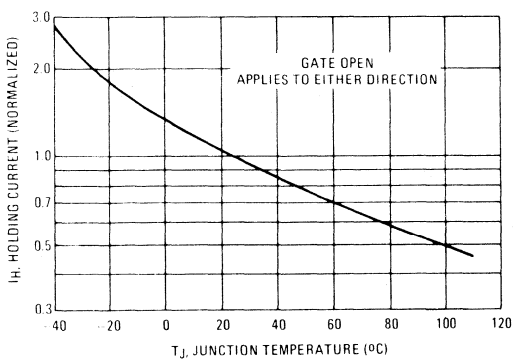


FIGURE 6 – TYPICAL LATCHING CURRENT

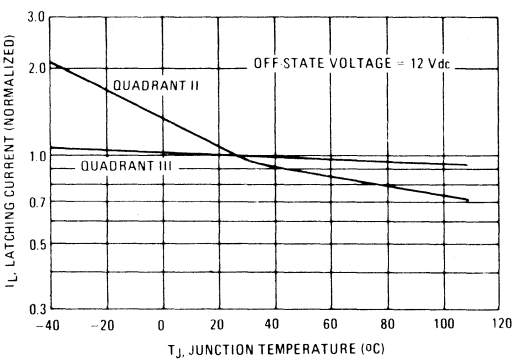


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FIGURE 7 – MAXIMUM ON-STATE CHARACTERISTICS

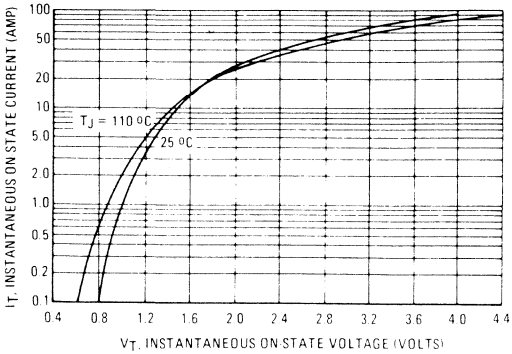


FIGURE 8 – MAXIMUM NON-REPETITIVE SURGE CURRENT

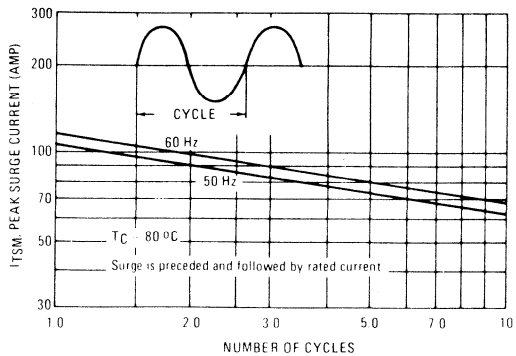
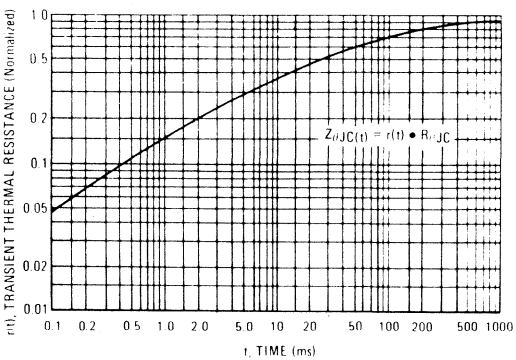


FIGURE 9 – TYPICAL THERMAL RESISTANCE FROM MOUNTING BASE TO HEATSINK

Metal to Metal:	Dry	0,9 °C/W
Metal to Metal:	Lubed	0,3 °C/W
With Insulator:	Dry	Not recommended
With Insulator:	Lubed	1,3 °C/W

These values are available when using the rectangular washer and mica insulator furnished with the kit MK221-2. The recommended mounting torque is 8 Kg. cm.

FIGURE 10 – THERMAL RESPONSE



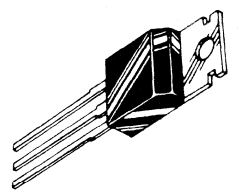
MAC15
MAC15A

SILICON BIDIRECTIONAL THYRISTORS

. . . designed primarily for full-wave ac control applications, such as solid-state relays, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt▲ Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Two Modes (MAC15)
  Four Modes (MAC15A)

TRIACS
(THYRISTORS)
15 AMPERES RMS
200 – 800 VOLTS



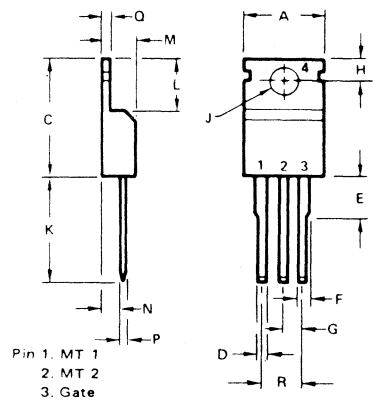
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage, Note 1 (T_J = -40 to +125°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open	V_{DRM}		Volts
MAC15-4, MAC15A-4		200	
MAC15-6, MAC15A-6		400	
MAC15-8, MAC15A-8		600	
MAC15-10, MAC15A-10		800	
Peak Gate Voltage	V_{GM}	10	Volts
On-State Current RMS (T_C = +80°C) Full Cycle Sine Wave 50 to 60 Hz (T_C = +95°C)	$I_{T(RMS)}$	15 12	Amp
Peak Surge Current (One Full Cycle, 60 Hz, T_C = +80°C) preceded and followed by rated current	I_{TSM}	150	Amp
Peak Gate Power (T_C = +80°C, Pulse Width = 2 μs	P_{GM}	20	Watts
Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
Peak Gate Current	I_{GM}	2	Amp
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTIC

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	°C/W

▲Trademark of Motorola Inc.



All JEDEC dimensions and notes apply

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.380	0.420	9.660	10.66
C	0.560	0.625	14.23	15.87
D	0.020	0.045	0.510	1.140
E		0.250		6.350
F	0.045	0.070	1.140	1.770
G	0.090	0.110	2.290	2.790
H	0.100	0.120	2.540	3.040
J	0.139	0.147	3.531	3.733
K	0.500	0.562	12.70	14.27
L	0.230	0.270	5.850	6.820
M	0.140	0.190	3.560	4.820
N	0.080	0.115	2.040	2.920
P	0.012	0.045	0.310	1.140
Q	0.020	0.055	0.510	1.390
R	0.190	0.210	4.830	5.330

CASE 221-02
TO-220 AB

6

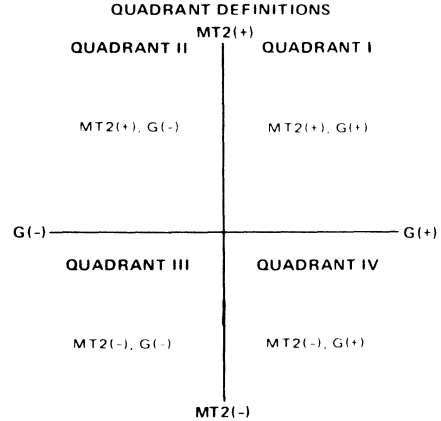
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current (Either Direction) Rated V_{DRM} @ T_J = 125°C, Gate Open	I_{DRM}	–	–	2	mA
Peak On-State Voltage (Either Direction) I_{TM} = 21 A Peak; Pulse Width = 1 to 2 ms, Duty Cycle ≤ 2%	V_{TM}	–	1.3	1.6	Volts
Peak Gate Trigger Current Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2 μs	I_{GTM}				mA
MT2 (+), G(+) – MAC15, MAC15A		–	–	50	
MT2 (+), G(–) – MAC15A		–	–	75	
MT2 (–), G(–) – MAC15, MAC15A		–	–	50	
MT2 (–), G(+) – MAC15A		–	–	75	
Peak Gate Trigger Voltage Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2 μs	V_{GTM}				Volts
MT2 (+), G(+) – MAC15, MAC15A		–	0.9	2	
MT2 (+), G(–) – MAC15A		–	0.9	2.5	
MT2 (–), G(–) – MAC15, MAC15A		–	1.1	2	
MT2 (–), G(+) – MAC15A		–	1.4	2.5	
Main Terminal Voltage = Rated V_{DRM}, R_L = 10 k ohms, T_J = 110°C					
MT2 (+), G(+); MT2 (–), G(–) – MAC15, MAC15A		0.2	–	–	
MT2 (+), G(–); MT2 (–), G(+) – MAC15A		0.2	–	–	
Holding Current (Either Direction) Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current = 200 mA	I_H	–	6	40	mA
Turn-On Time Rated V_{DRM}, I_{TM} = 17 A I_{GT} = 120 mA, Rise Time = 0.1 μs, Pulse Width = 2 μs	tgt	–	1.5	2	μs
Critical Rate of Rise of Commutation Voltage Rated V_{DRM}, I_{TM} = 21 A, Commutating di/dt = 8 A/ms, Gate Unenergized, T_C = 80°C	dv/dt(C)	–	5	–	V/μs

NOTES:

1 Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

QUADRANT DEFINITIONS



Trigger devices are recommended for gating on Triacs. They provide:

1. Consistent predictable turn-on points.
2. Simplified circuitry.
3. Fast turn-on time for cooler, more efficient and reliable operation.

ELECTRICAL CHARACTERISTICS of RECOMMENDED BIDIRECTIONAL SWITCHES

USAGE	General	
PART NUMBER	MBS4991	MBS4992
V_S	6–10 V	7.5–9 V
I_S	350 μA Max	120 μA Max
$V_{S1} - V_{S2}$	0.5 V Max	0.2 V Max
Temperature Coefficient	0.02%/°C Typ	

See AN-526 for Theory and Characteristics of Silicon Bidirectional Switches.

FIGURE 1 – RMS CURRENT DERATING

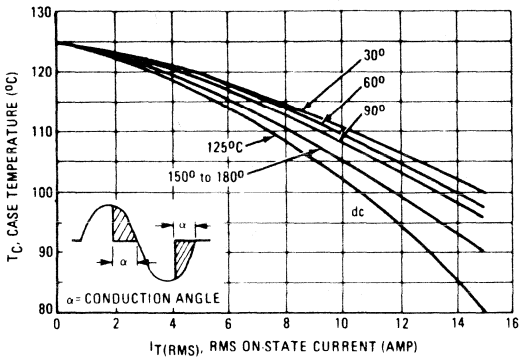


FIGURE 2 – ON-STATE POWER DISSIPATION

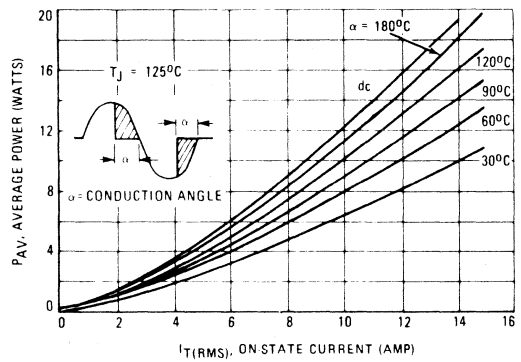


FIGURE 3 – TYPICAL GATE TRIGGER VOLTAGE

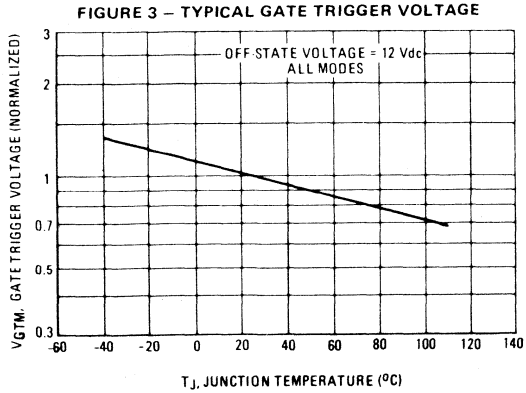


FIGURE 4 – TYPICAL GATE TRIGGER CURRENT

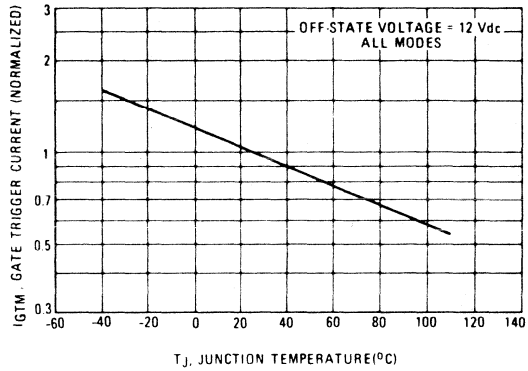


FIGURE 5 – MAXIMUM ON-STATE CHARACTERISTICS

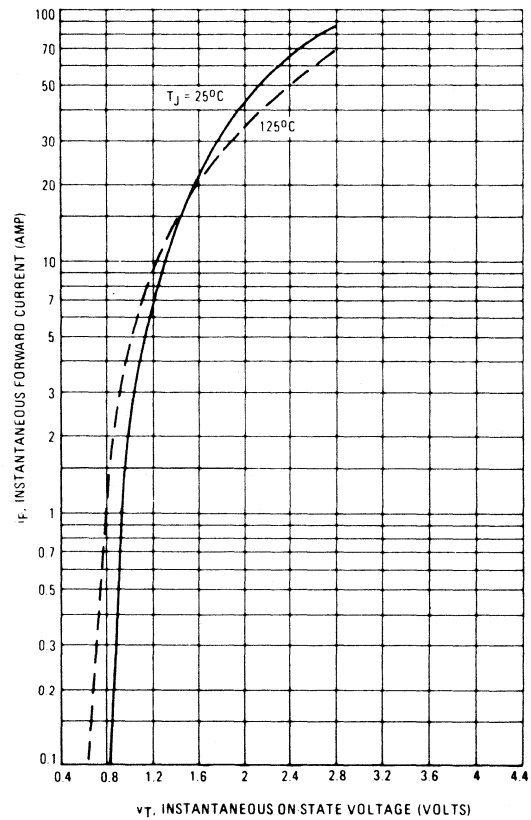


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FIGURE 6 – TYPICAL HOLDING CURRENT

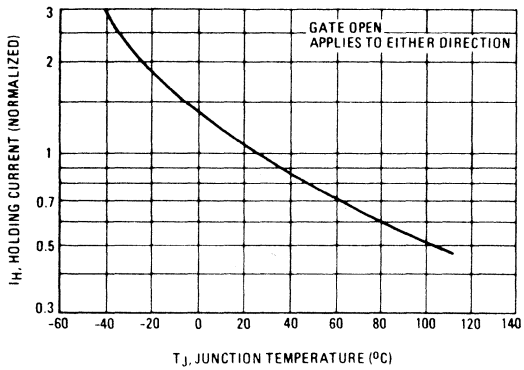


FIGURE 7 – MAXIMUM NON-REPETITIVE SURGE CURRENT

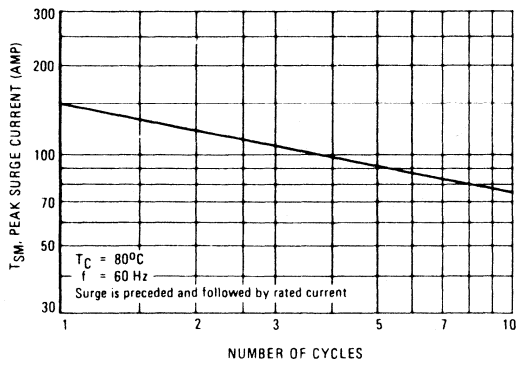
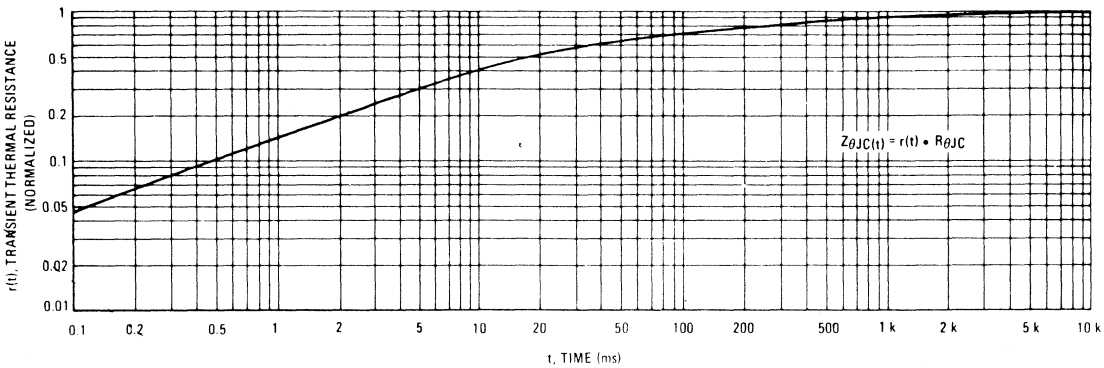
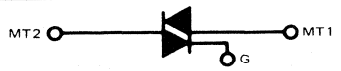


FIGURE 8 – THERMAL RESPONSE



MAC92-1 thru MAC92-8



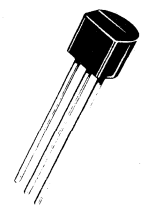
SILICON BIDIRECTIONAL TRIODE THYRISTORS

. . . designed for use in solid state relays, TTL logic and light industrial applications. Supplied in an inexpensive plastic TO-92 package which is readily adaptable for use in automatic insertion equipment.

- Sensitive Gate Triggering Guaranteed in Three Modes
- One-Piece, Injection-Molded Unibloc ▲ Package

TRIACS

0.6 AMPERE RMS
30–600 VOLTS



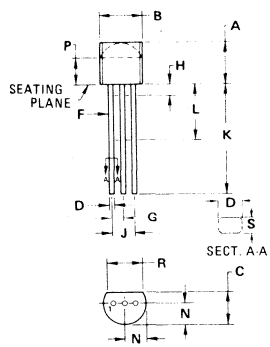
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage (T_J = -40 to +110°C) ½ Sine Wave 50 to 60 Hz, Gate Open MAC92 – 1 – 2 – 3 – 4 – 5 – 6 – 7 – 8	V_{DRM}	 30 60 100 200 300 400 500 600	Volts
On-State RMS Current Full Cycle Sine Wave 50 to 60 Hz, (T_C = +50°C)	$I_{T(RMS)}$	0.8	Amp
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T_C = +50°C) preceded and followed by rated current	I_{TSM}	8.0	Amp
Circuit Fusing Considerations (T_J = -40 to +110°C, t = 1.0 to 8.3 ms)	I^2t	0.26	A^2s
Average Gate Power	$P_{G(AV)}$	0.01	Watt
Peak Gate Current	I_{GM}	1.0	Amp
Operating Junction Temperature Range	T_J	-40 to +110	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	75	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W

▲Trademark of Motorola Inc.



STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.
CASE 29-02
TO-92

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DS 6543 R2

6

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and Either Polarity of MT2 to MT1 Voltage unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Peak Blocking Current V_D = Rated V_{DRM} @ T_J = 110°C, Gate Open	I_{DRM}	–	100	μA
Peak On-State Voltage I_{TM} = 1.0 A Peak; Pulse Width = 1.0 to 2.0 ms, Duty Cycle ≤ 2.0%	V_{TM}	–	1.9	Volts
Gate Trigger Current, Continuous dc V_D = 7.0 Vdc, R_L = 100 Ohms MT2(+), G(+); MT2(–), G(–), MT2(+), G(–)	I_{GT}	–	5.0	mA
Gate Trigger Voltage, Continuous dc V_D = 7.0 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 μs MT2(+), G(+); MT2(–), G(–), MT2(+), G(–) MT2(+), G(+); MT2(–), G(–), MT2(+), G(–); T_C = –40°C V_D = Rated V_{DRM}, R_L = 10 k ohms, T_J = 110°C MT2(+), G(+); MT2(–), G(–)	V_{GT}	– – 0.1	2.5 3.5 –	Volts
Holding Current V_D = 7.0 Vdc, Gate Open; T_C = 25°C Initiating Current = 20 mA T_C = –40°C	I_H	– –	10 20	mA

FIGURE 1 – TYPICAL GATE TRIGGER VOLTAGE

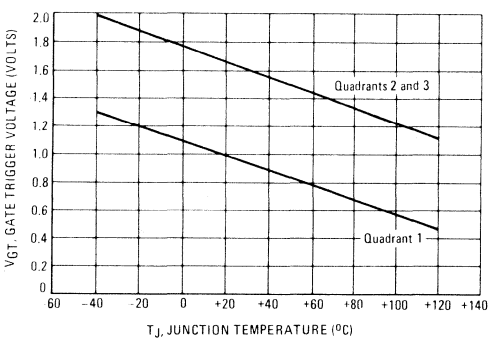

FIGURE 2 – TYPICAL GATE TRIGGER CURRENT

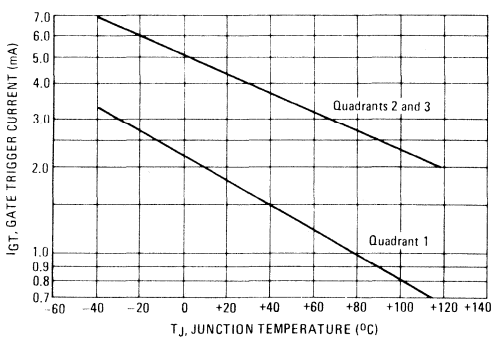

FIGURE 3 – AVERAGE CURRENT DERATING
(REFERENCE: CASE TEMPERATURE)

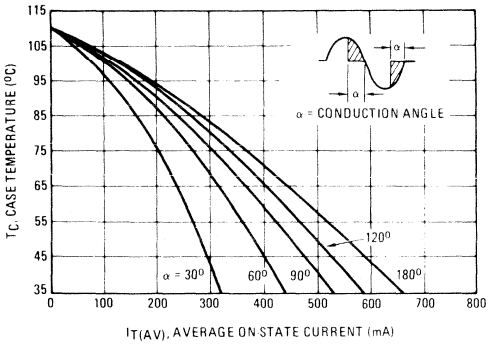

FIGURE 4 – RMS CURRENT DERATING
(REFERENCE: CASE TEMPERATURE)

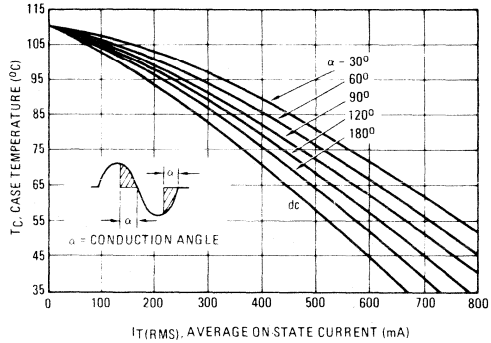

FIGURE 5 – AVERAGE CURRENT DERATING
(REFERENCE: AMBIENT TEMPERATURE)

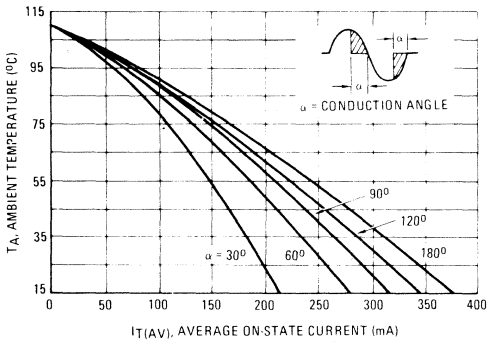

FIGURE 6 – RMS CURRENT DERATING
(REFERENCE: AMBIENT TEMPERATURE)

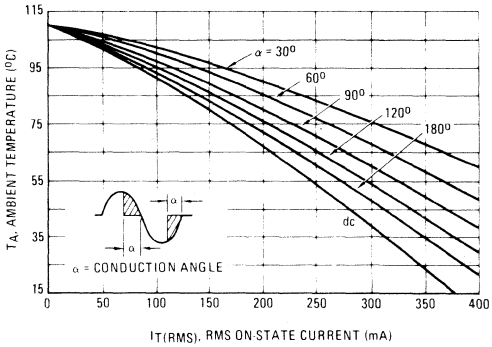

FIGURE 7 – ON-STATE POWER DISSIPATION

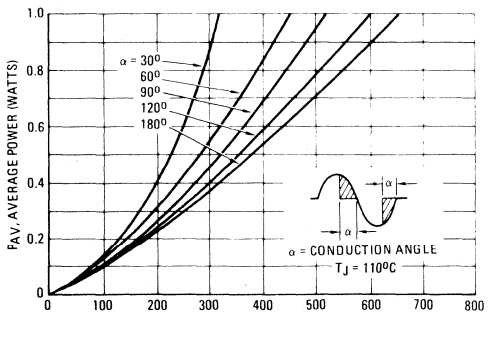

FIGURE 8 – ON-STATE POWER DISSIPATION

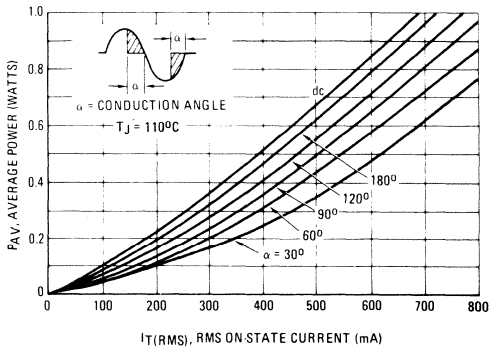

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FIGURE 9 – ON-STATE CHARACTERISTICS

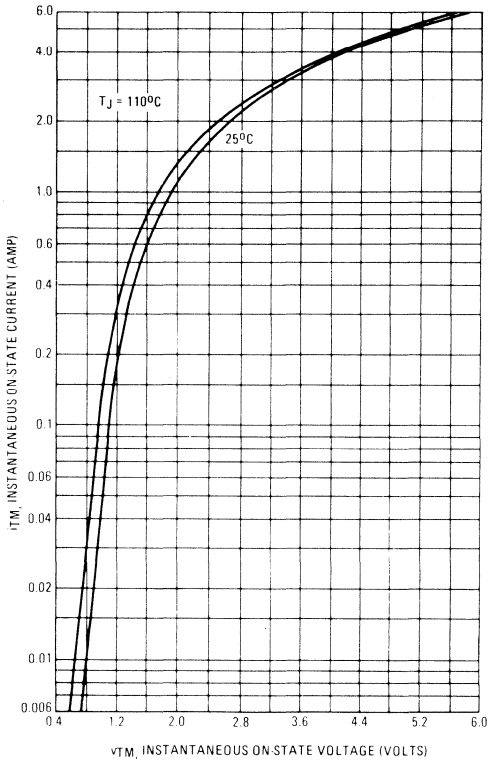


FIGURE 10 – TYPICAL HOLDING CURRENT

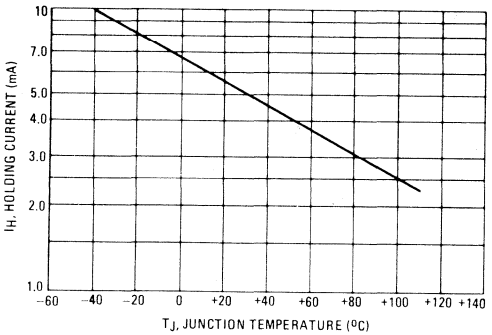


FIGURE 11 – MAXIMUM ALLOWABLE SURGE CURRENT

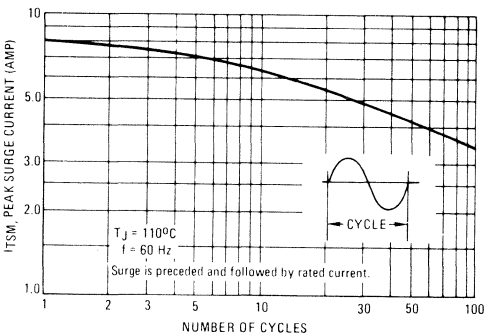
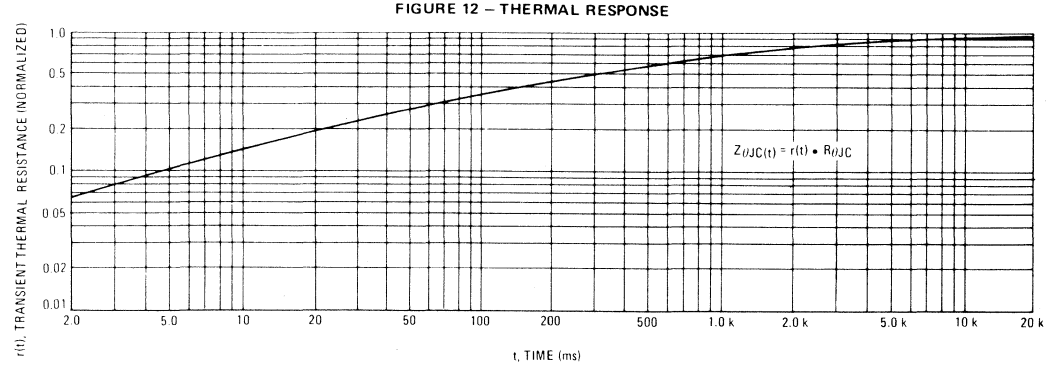
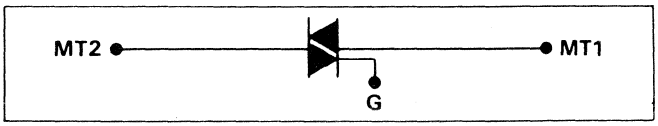


FIGURE 12 – THERMAL RESPONSE

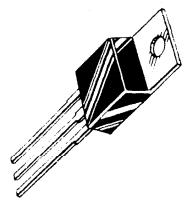


MAC223 series
MAC223A series



TRIACS
(THYRISTORS)

25 AMPERES RMS
100-800 VOLTS



SILICON BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for full-wave ac control applications such as lighting systems, heater controls, motor controls and power supplies; or wherever full-wave silicon-gate-controlled devices are needed.

- Off-State Voltages to 800 Volts
- All Diffused and Glass-Passivated Junctions for Parameter Uniformity and Stability
- Small, Rugged Thermowatt Construction for Thermal Resistance and High Heat Dissipation
- Gate Triggering Guaranteed in Three modes (MAC223 series) or Four Modes (MAC223A) series

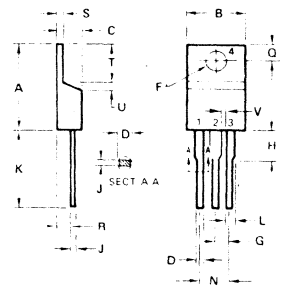
MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Peak Repetitive Off-State Voltage (T_J = -40 to 125°C) Note 1 (1/2 Sine Wave 50 to 60 Hz, Gate Open)		V_{DRM}		Volts
MAC223 / MAC223A	3		100	
	4		200	
	5		300	
	6		400	
	7		500	
	8		600	
	9		700	
	10		800	
On-State RMS Current (T_C = 80°C) (Full Cycle Sine Wave 50 to 60 Hz)		$I_{T(RMS)}$	25	Amp
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T_J = 125°C)		I_{TSM}	250	Amp
Circuit Fusing (T_J = -40 to 125°C; t = 8.3 ms)		I^2t	260	A^2s
Peak Gate Current (t ≤ 2.0 μs)		I_{GM}	2.0	Amp
Peak Gate Voltage (t ≤ 2.0 μs)		V_{GM}	±10	Volts
Peak Gate Power (t ≤ 2.0 μs)		P_{GM}	20	Watts
Average Gate Power (T_C = 80°C, t ≤ 8.3 ms)		$P_{G(AV)}$	0.5	Watts
Operating Junction Temperature Range		T_J	-40 to 125	°C
Storage Temperature Range		T_{stg}	-40 to 150	°C
Mounting Torque		—	8.0	in/lb

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.2	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W

NOTE 1: Ratings apply for open gate conditions. Devices shall not be tested with a constant current source for blocking voltage such that the voltage applied exceeds the rated blocking voltage.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	—	0.045	—

NOTE
1. DIM. L & H APPLIES TO ALL LEADS.

STYLE 4:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

CASE 221-A-02
TO-220AB

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DS6613

6

ELECTRICAL CHARACTERISTICS (T_C = 25°C and either polarity of MT2 to MT1 voltage unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current (Note 1) (V_D = Rated V_{DRM}, T_J = 125°C)	I_{DRM}	—	—	2.0	mA
Peak On-State Voltage (I_{TM} = 35 A Peak, Pulse Width ≤ 2 ms, Duty Cyle ≤ 2%)	V_{TM}	—	1.4	1.85	Volts
Gate Trigger Current, Continuous dc (V_D = 12 V, R_L = 100 Ω) MT2(+), G(+); MT2(-), G(-), MT2(+), G(-) All Types MT2(-), G(+) A Suffix Only	I_{GT}	 — —	 20 30	 50 75	mA
Gate Trigger Voltage, Continuous dc (V_D = 12 V, R_L = 100 Ω) MT2(+), G(+); MT2(-), G(-), MT2(+), G(-) All Types MT2(-), G(+) A Suffix Only (V_D = Rated V_{DRM}, T_J = 125°C, R_L = 10 k) All Types, All Trigger Modes	V_{GT}	 — — 0.2	 1.1 1.3 0.4	 2.0 2.5 —	Volts
Holding Current (V_D = 12 V, I_{TM} = 200 mA, Gate Open)	I_H	—	10	50	mA
Gate Controlled Turn-On Time (V_D = Rated V_{DRM}, I_{TM} = 35 A Peak, I_G = 200 mA)	t_{gt}	—	1.5	—	μs
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, T_C = 125°C)	dv/dt	—	40	—	V/μs
Critical Rate of Rise of Commutation Voltage (V_D = Rated V_{DRM}, I_{TM} = 35 A Peak, Commutating di/dt = 13.4 A/ms, Gate Unenergized, T_C = 80°C)	dv/dt(c)	—	5.0	—	V/μs

NOTE 1 Ratings apply for open gate conditions. Devices shall not be tested with a constant current source for blocking voltage such that the voltage applied exceeds the rated blocking voltage.

FIGURE 1 — RMS CURRENT DERATING

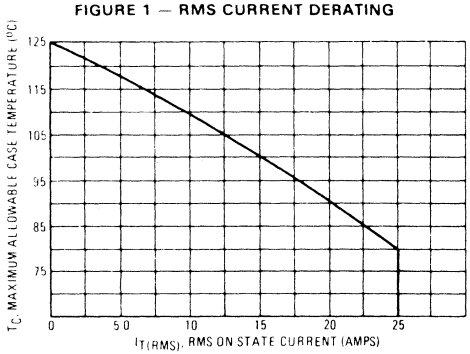


FIGURE 2 — ON-STATE POWER DISSIPATION

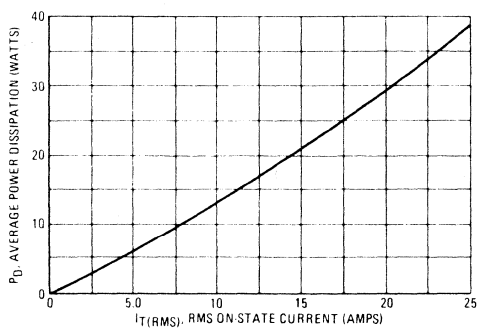


FIGURE 3 — GATE TRIGGER CURRENT

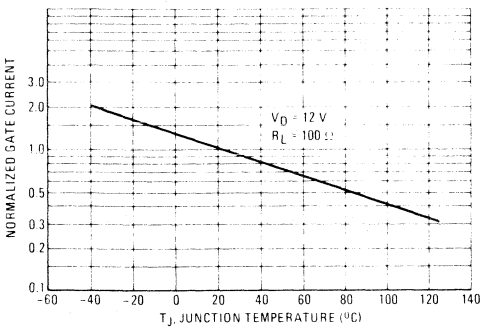


FIGURE 4 — GATE TRIGGER VOLTAGE

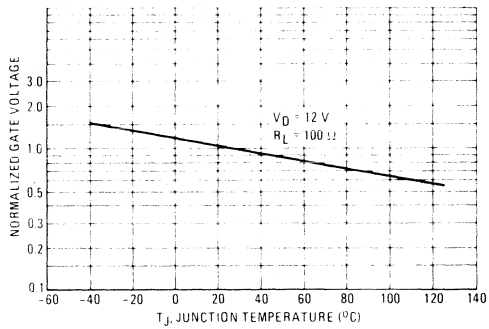


FIGURE 5 — HOLD CURRENT

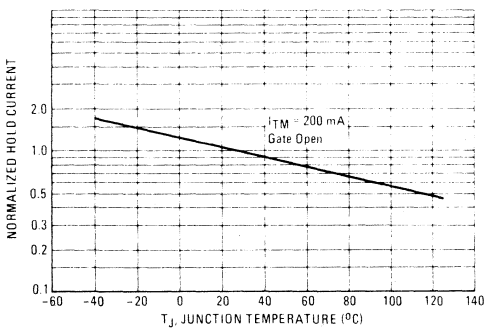
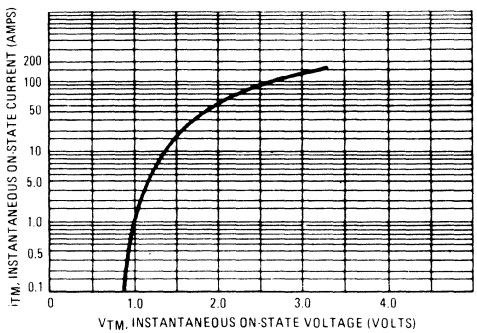


FIGURE 6 — ON-STATE CHARACTERISTICS



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MAC228-2 thru -10
MAC228A2 thru A10

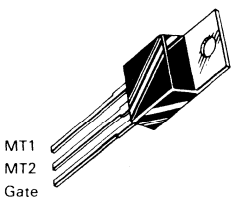
TRIACS
(THYRISTORS)

8 AMPERES RMS
25-800 VOLTS

SILICON BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for industrial and consumer applications for full wave control of ac loads such as appliance controls, heater controls, motor controls, and other power switching applications.

- Sensitive Gate Triggering in Three Trigger Modes for AC Triggering or Sinking Current Sources (MAC228 series)
- Four Mode Triggering (10 mA) for Drive Circuits that Source Current (MAC228A series)
- All Diffused and Glass-Passivated Junctions for Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance and High Heat Dissipation
- Center Gate Geometry for Uniform Current Spreading

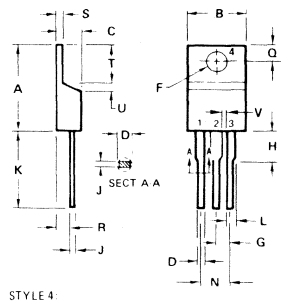


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (T_J = -40 to 110°C) Note 1. 1. 2 Sine Wave 50 to 60 Hz, Gate Open	V_{DRM}		Volts
MAC228 -2, A2		50	
MAC228 -3, A3		100	
MAC228 -4, A4		200	
MAC228 -5, A5		300	
MAC228 -6, A6		400	
MAC228 -7, A7		500	
MAC228 -8, A8		600	
MAC228 -9, A9		700	
MAC228 -10, A10		800	
On-State RMS Current (T_C = 80°C) Full Cycle Sine Wave 50 to 60 Hz	$I_{T(RMS)}$	8.0	Amps
Peak Non-Repetitive Surge Current (One Full Cycle 60 Hz, T_J = 110°C)	I_{TSM}	80	Amps
Circuit Fusing (T_J = -40 to 110°C, t = 8.3 ms)	I^2t	40	A^2s
Peak Gate Current (t ≤ 2 μs)	I_{GM}	±2.0	Amps
Peak Gate Voltage (t ≤ 2 μs)	V_{GM}	±10	Volts
Peak Gate Power (t ≤ 2 μs)	P_{GM}	20	Watts
Average Gate Power (T_C = 80°C, t ≤ 8.3 ms)	$P_{G(AV)}$	0.5	Watts
Operating Junction Temperature Range	T_J	-40 to 110	°C
Storage Temperature Range	T_{stg}	-40 to 150	°C
Mounting Torque		8.0	in-lb

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W



STYLE 4:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

NOTE:
1. DIM. L & H APPLIES TO ALL LEADS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

CASE 221A-02
TO-220 AB

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DS6618

ELECTRICAL CHARACTERISTICS (T_C = 25°C and either polarity of MT2 to MT1 voltage unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Blocking Current (Note 1) (V_D = Rated V_{DRM}, T_J = 110°C)		I_{DRM}	—	—	2.0	mA
Peak On-State Voltage (I_{TM} = 11 A Peak, Pulse Width ≤ 2 ms, Duty Cycle ≤ 2%)		V_{TM}	—	—	1.5	Volts
Gate Trigger Current, Continuous dc (V_D = 12 V, R_L = 100 Ω)		I_{GT}				mA
MT2(+), G(+); MT2(+), G(−); MT2(−), G(−)	MAC228 series		—	—	5.0	
MT2(+), G(+); MT2(+), G(−); MT2(−), G(−); MT2(−), G(+)	MAC228A series		—	—	10	
Gate Trigger Voltage, Continuous dc (V_D = 12 V, R_L = 100 Ω)		V_{GT}				Volts
MT2(+), G(+); MT2(+), G(−); MT2(−), G(−)	MAC228 series		—	—	2.2	
MT2(+), G(+); MT2(+), G(−); MT2(−), G(−); MT2(−), G(+)	MAC228A series		—	—	2.5	
(V_D = Rated V_{DRM}, T_C = 110°C, R_L = 10 k)						
MT2(+), G(+); MT2(+), G(−); MT2(−), G(−)	All Types		0.2	—	—	
MT2(−), G(+)	MAC228A series		0.2	—	—	
Holding Current (V_D = 12 Vdc, I_{TM} = 200 mA, Gate Open)		I_H	—	—	15	mA
Gate-Controlled Turn-On Time (V_D = Rated V_{DRM}, I_{TM} = 16 A Peak, I_G = 30 mA)		t_{gt}	—	1.5	—	μs
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, T_C = 110°C)		dv/dt	—	25	—	V/μs
Critical Rate of Rise of Commutation Voltage (V_D = Rated V_{DRM}, I_{TM} = 11 A Peak, Commutating di/dt = 5.8 A/ms, Gate Unenergized, T_C = 80°C)		dv/dt (c)	—	5.0	—	V/μs

Note 1. Ratings apply for open gate conditions. Devices shall not be tested with a constant current source for blocking voltage such that the voltage applied exceeds the rated blocking voltage.

FIGURE 1 — RMS CURRENT DERATING

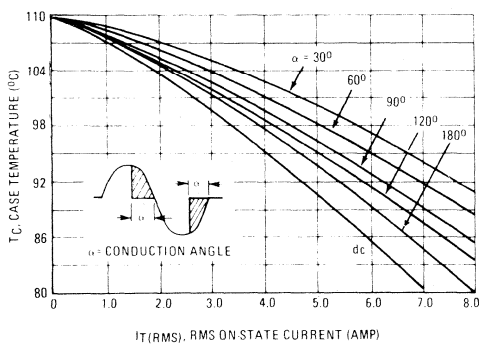
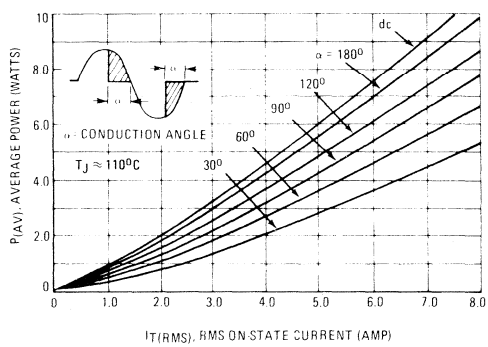


FIGURE 2 — ON-STATE POWER DISSIPATION



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MAC 525
MAC 525 A

Product Preview

SILICON BIDIRECTIONAL TRIODE THYRISTORS

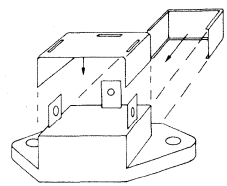
The MAC525,A is designed primarily for industrial and consumer applications, for full-wave control of ac load such as appliance control, power supplies, solid state relays, heating control, motor control, welding equipment and power switching systems.

- Quick connect/disconnect terminal.
- Glass passivated and center gate geometry.
- Meet UL flammability and lead spacing requirement.
- Low cost solution.
- TO-3 base.

TRIAC

100 – 800V

25 Amp RMS



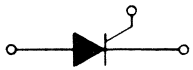
(Case number not yet allocated. TO3 base.)

MAXIMUM RATINGS

Rating			Symbol	Value	Unit
Peak Repetitive Off-Stage Voltage			V_{DRM}		Volts
		– 3		100	
		– 4		200	
		– 5		300	
	MAC525	– 6		400	
	MAC525A	– 7		500	
		– 8		600	
		– 9		700	
		– 10		800	
On State RMS Current ($T_C = 80\,^{\circ}C$)			I_T(RMS)	25	Amp
Peak Non-Repetitive Surge Current			I_{TSM}	250	Amp
Circuit Fusing			I^2t	260	A^2s
Operating Junction Temperature Range			T_J	−40 to +125	°C
Mounting Torque			–	6	in/lb

ELECTRICAL CHARACTERISTICS ($T_C = 25\,^{\circ}C$ unless otherwise noted)

Peak Blocking Current ($T_C = 125\,^{\circ}C$)		I_{DRM}	2.0	mA
Peak On-Stage Voltage (I_{TM} = 35A Peak)		V_{TM}	1.6	mA
Peak Gate Current	MAC525	I_{GT123}	50	mA
(V_D = 12Vdc, R_L = 50Ohms)	MAC525A	I_{GT4}	75	mA
Holding Current (V_D = 12Vdc, Gate Open)		I_H	50	mA



PLASTIC SILICON CONTROLLED RECTIFIERS

PNPN devices designed for high volume, line-powered consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive plastic TO-92 package which is readily adaptable for use in automatic insertion equipment.

- Sensitive Gate Trigger Current – 200 μA Maximum
- Low Reverse and Forward Blocking Current – 100 μA Maximum, T_C = 125°C
- Low Holding Current – 5.0 mA Maximum
- Glass-Passivated Surface for Reliability and Uniformity

MAXIMUM RATINGS

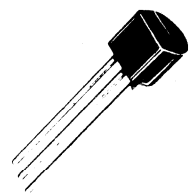
Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage	V_{RRM}		Volts
MCR100-3		100	
MCR100-4		200	
MCR100-5		300	
MCR100-6		400	
MCR100-7		500	
MCR100-8		600	
Forward Current RMS (See Figures 1 & 2) (All Conduction Angles)	$I_{T(RMS)}$	0.8	Amp
Peak Forward Surge Current, T_A = 25°C (1/2 cycle, Sine Wave, 60 Hz)	I_{TSM}	6.0	Amp
Circuit Fusing Considerations, T_A = 25°C (t = 1.0 to 8.3 ms)	I^2t	0.15	A^2s
Peak Gate Power — Forward, T_A = 25°C	P_{GM}	0.1	Watt
Average Gate Power — Forward, T_A = 25°C	$P_{GF(AV)}$	0.01	Watt
Peak Gate Current — Forward, T_A = 25°C (300 μs, 120 PPS)	I_{GFM}	1.0	Amp
Peak Gate Voltage — Reverse	V_{GRM}	5.0	Volts
Operating Junction Temperature Range @ Rated V_{RRM} and V_{DRM}	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Lead Solder Temperature (<1/16" from case, 10 s max)		230	°C

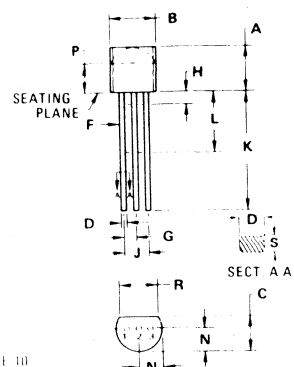
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R θJC	75	°C/W
Thermal Resistance, Junction to Ambient	R θJA	200	°C/W

PLASTIC SILICON CONTROLLED RECTIFIERS

0.8 AMPERE RMS
100 to 600 VOLTS





STYLE 10
PIN 1 CATHODE
2 GATE
3 ANODE

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	—	2.54	—	0.100
J	2.41	2.67	0.095	0.105
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.03	2.92	0.080	0.115
P	2.92	—	0.115	—
R	3.43	—	0.135	—
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply
CASE 29-02
TO-92

6

ELECTRICAL CHARACTERISTICS (R_{GK} = 1000 Ohms)

Characteristic		Symbol	Min	Max	Unit
Peak Forward Blocking Voltage (T_C = 125°C)	MCR100-3	V_{DRM}	100		Volts
	MCR100-4		200		
	MCR100-5		300		
	MCR100-6		400		
	MCR100-7		500		
	MCR100-8		600		
Peak Forward Blocking Current (Rated V_{DRM} @ T_C = 125°C)		I_{DRM}	--	100	μA
Peak Reverse Blocking Current (Rated V_{RRM} @ T_C = 125°C)		I_{RRM}	--	100	μA
Forward "On" Voltage (Note 1) (I_{TM} = 1.0 A peak @ T_A = 25°C)		V_{TM}	-	1.7	Volts
Gate Trigger Current (Continuous dc) (Note 2) (Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = 25°C	I_{GT}		200	μA
Gate Trigger Voltage (Continuous dc)	T_C = 25°C	V_{GT}		0.8	Volts
(Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = -65°C		-	1.2	
(Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms)	T_C = 125°C		0.1		
Holding Current	T_C = 25°C	I_H		5.0	mA
(Anode Voltage = 7.0 Vdc, initiating current = 20 mA)	T_C = -65°C		-	10	

NOTE

1. Forward current applied for 1.0 ms maximum duration, duty cycle = 1.0%.
2. R_{GK} current is not included in measurement.

FIGURE 1 – CURRENT DERATING
(REFERENCE: CASE TEMPERATURE)

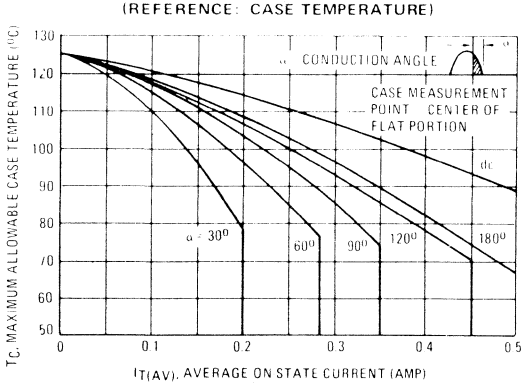
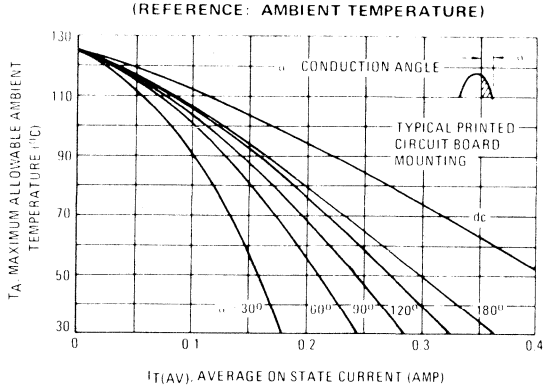


FIGURE 2 – CURRENT DERATING
(REFERENCE: AMBIENT TEMPERATURE)



MCR106-1 thru MCR106-4
MCR106-6 • MCR106-8

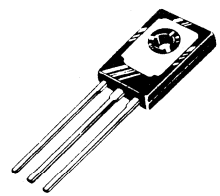
SILICON
CONTROLLED RECTIFIERS

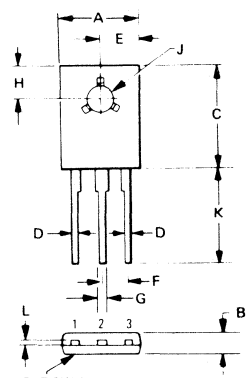
. . . Annular◆ PNPN devices designed for high volume consumer applications such as temperature, light, and speed control; process and remote control, and warning systems where reliability of operation is important.

- Annular◆ Passivated Surface for Reliability and Uniformity
- Power Rated at Economical Prices
- Practical Level Triggering and Holding Characteristics
- Flat, Rugged, Thermopad▲ Construction for Low Thermal Resistance, High Heat Dissipation and Durability

THYRISTORS

4.0 AMPERES RMS
30 thru 600 VOLTS





Pin 1. Cathode
2. Anode
3. Gate

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	6.860	8.380	0.270	0.330
B	1.770	3.300	0.070	0.130
C	9.910	11.430	0.390	0.450
D	0.508	0.660	0.020	0.026
E	3.810 NOM		0.150 NOM	
F	2.290 TP		0.090 TP	
G	0.635	0.889	0.025	0.035
H	3.300	4.450	0.130	0.175
J	2.910	3.000	0.115	0.118
K	15.110	16.650	0.595	0.655
L	0.381	0.635	0.015	0.025

CASE 77-02

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage (Note 1) MCR106-1	V_{RRM}	30	Volts
-2		60	
-3		100	
-4		200	
-6		400	
-8		600	
RMS Forward Current (All Conduction Angles)	$I_{T(RMS)}$	4.0	Amp
Average Forward Current $T_C = 93^oC$ $T_A = 30^oC$	$I_{T(AV)}$	2.55 0.68	Amp
Peak Non-Repetitive Surge Current (1/2 cycle, 60 Hz, $T_J = -40$ to $+110^oC$)	I_{TSM}	25	Amp
Circuit Fusing Considerations ($T_J = -40$ to $+110^oC$, t = 1.0 to 8.3 ms)	I^2t	2.6	A^2s
Peak Gate Power	P_{GM}	0.5	Watt
Average Gate Power	$P_{G(AV)}$	0.1	Watt
Peak Forward Gate Current	I_{GM}	0.2	Amp
Peak Reverse Gate Voltage	V_{RGM}	6.0	Volts
Operating Junction Temperature Range	T_J	-40 to +110	^oC
Storage Temperature Range	T_{stg}	-40 to +150	^oC
Mounting Torque (Note 2)	—	6.0	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.0	$^oC/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	$^oC/W$

◆Annual Semiconductors Patented by Motorola Inc.

▲Trademark of Motorola Inc.

6

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted, R_{GK} = 1000 ohms.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Voltage (T_J = 110°C, Note 1)	V_{DRM}				Volts
MCR106-1		30	–	–	
-2		60	–	–	
-3		100	–	–	
-4		200	–	–	
-6		400	–	–	
-8		600	–	–	
Peak Forward Blocking Current (Rated V_{DRM}, T_J = 110°C)	I_{DRM}	–	–	200	μA
Peak Reverse Blocking Current (Rated V_{RRM}, T_J = 110°C)	I_{RRM}	–	–	200	μA
Forward "On" Voltage (I_{TM} = 4.0 A Peak)	V_{TM}	–	–	2.0	Volts
Gate Trigger Current (Continuous dc)	I_{GT}				μA
(V_{AK} = 7.0 Vdc, R_L = 100 ohms)		–	–	200	
(V_{AK} = 7.0 Vdc, R_L = 100 ohms, T_C = -40°C)		–	–	500	
Gate Trigger Voltage (Continuous dc) (V_{AK} = 7.0 Vdc, R_L = 100 ohms, T_C = 25°C)	V_{GT}	–	–	1.0	Volts
Gate Non-Trigger Voltage (V_{AK} = Rated V_{DRM}, R_L = 100 ohms, T_J = 110°C)	V_{GD}	0.2	–	–	Volts
Holding Current (V_{AK} = 7.0 Vdc, T_C = 25°C)	I_H	–	–	5.0	mA
Forward Voltage Application Rate (T_J = 110°C)	dv/dt	–	10	–	V/μs

NOTES

1. Ratings apply for zero or negative gate voltage but positive gate voltage shall not be applied concurrently with a negative potential on the anode. When checking forward or reverse blocking capability, thyristor devices should not be tested with a constant current source in a manner that the voltage applied exceeds the rated blocking voltage.
2. Torque rating applies with use of torque washer (Shakeproof WD19523 or equivalent). Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Anode lead and heatsink contact pad are common. (See AN-290 B)

   For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +225°C. For optimum results, an activated flux (oxide removing) is recommended.

CURRENT DERATING

FIGURE 1 – MAXIMUM CASE TEMPERATURE

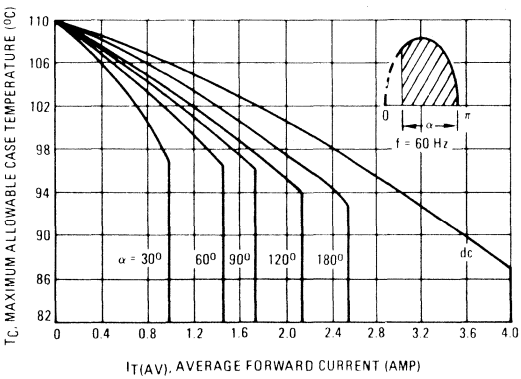
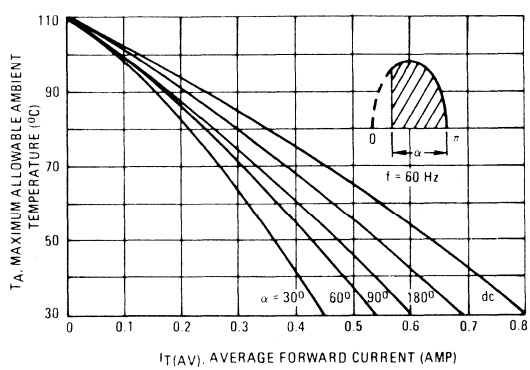
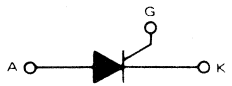


FIGURE 2 – MAXIMUM AMBIENT TEMPERATURE



2N6394 thru 2N6399
MCR220-5 • MCR220-7 • MCR220-9



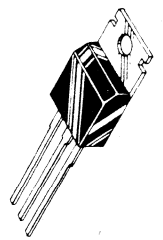
THYRISTORS

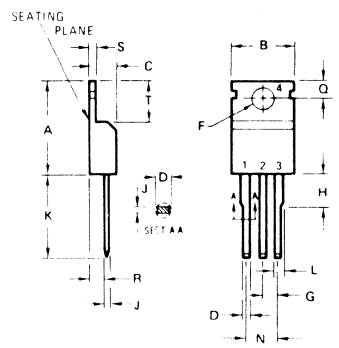
12 AMPERES RMS
50-800 VOLTS

SILICON CONTROLLED RECTIFIERS

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate controlled, solid-state devices are needed.

- Glass Passivated Junctions and Center Gate Fire for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt▲ Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 800 Volts





PIN 1 CATHODE
2 ANODE
3 GATE
4 ANODE

All JEDEC dimensions and notes apply

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H		6.35		0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

CASE 221-02
TO 220 AB

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Reverse Voltage (1)	V_{RRM}		Volts
2N6394		50	
2N6395		100	
2N6396		200	
MCR220-5		300	
2N6397		400	
MCR220-7		500	
2N6398		600	
MCR220-9		700	
2N6399		800	
Forward Current RMS T_J = 125°C (All Conduction Angles)	$I_{T(RMS)}$	12	Amps
Peak Forward Surge Current (1/2 cycle, Sine Wave, 60 Hz, T_J = 125°C)	I_{TSM}	100	Amps
Circuit Fusing Considerations (T_J = -40 to +125°C, t = 1.0 to 8.3 ms)	I^2t	40	A^2s
Forward Peak Gate Power	P_{GM}	20	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watt
Forward Peak Gate Current	I_{GM}	2.0	Amps
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	°C/W

(1) V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

*Indicates JEDEC Registered Data.

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6

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Voltage		V_{DRM}				Volts
(T_J = 125°C)	2N6394		50	–	–	
	2N6395		100	–	–	
	2N6396		200	–	–	
	MCR220-5		300	–	–	
	2N6397		400	–	–	
	MCR220-7		500	–	–	
	2N6398		600	–	–	
	MCR220-9		700	–	–	
	2N6399		800	–	–	
* Peak Forward Blocking Current (Rated V_{DRM} @ T_J = 125°C)		I_{DRM}	–	–	2.0	mA
* Peak Reverse Blocking Current (Rated V_{RRM} @ T_J = 125°C)		I_{RRM}	–	–	2.0	mA
* Forward "On" Voltage (I_{TM} = 24 A Peak)		V_{TM}	–	1.7	2.2	Volts
* Gate Trigger Current (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms)		I_{GT}	–	5.0	30	mA
* Gate Trigger Voltage (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms)		V_{GT}	–	0.7	1.5	Volts
* Gate Non-Trigger Voltage (Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms, T_J = 125°C)		V_{GD}	0.2	–	–	Volts
* Holding Current (Anode Voltage = 12 Vdc)		I_H	–	6.0	40	mA
Turn-On Time (I_{TM} = 12 A, I_{GT} = 40 mAdc)		t_{gt}	–	1.0	2.0	µs
Turn-Off Time (V_{DRM} = rated voltage)		tq				µs
(I_{TM} = 12 A, I_R = 12 A)			–	15	–	
(I_{TM} = 12 A, I_R = 12 A, T_J = 125°C)			–	35	–	
Forward Voltage Application Rate (T_J = 125°C)		dv/dt	–	50	–	V/µs

*Indicates JEDEC Registered Data.

FIGURE 1 – AVERAGE CURRENT DERATING

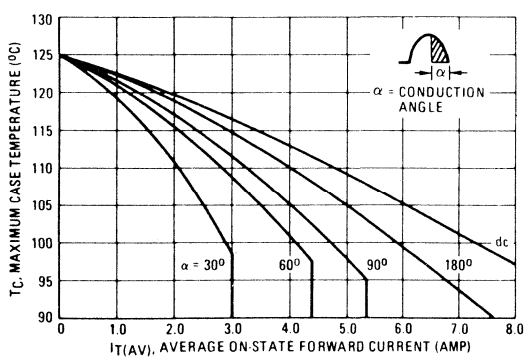


FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION

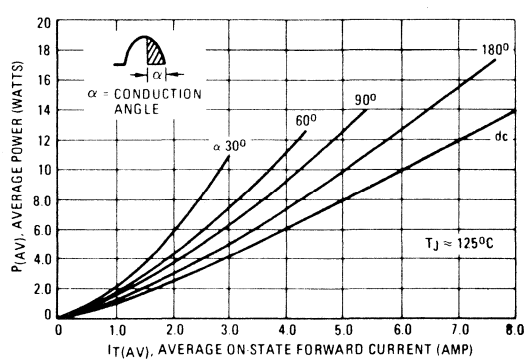


FIGURE 3 – ON-STATE CHARACTERISTICS

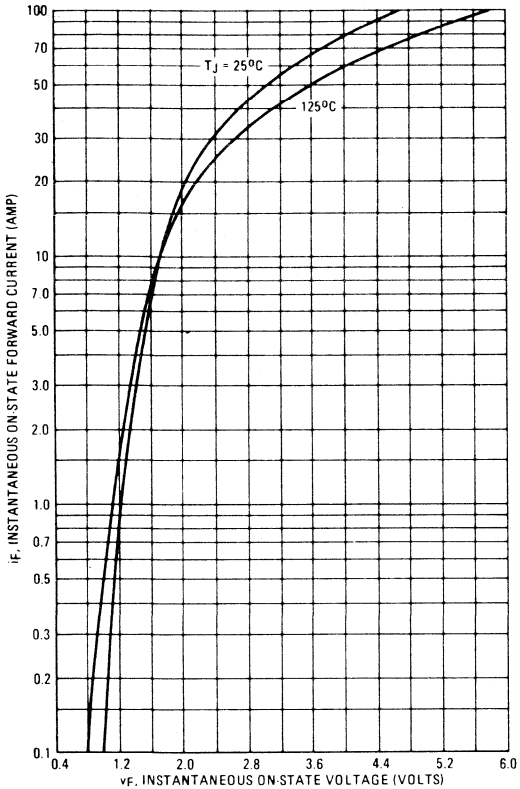


FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE CURRENT

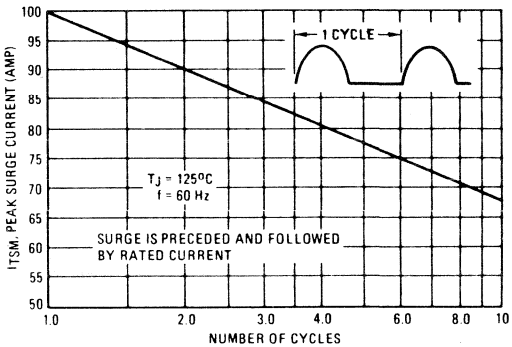


FIGURE 5 – CHARACTERISTICS AND SYMBOLS

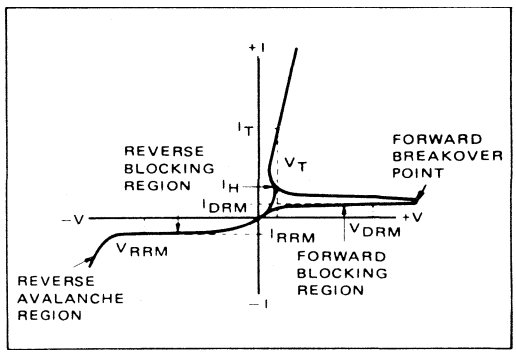
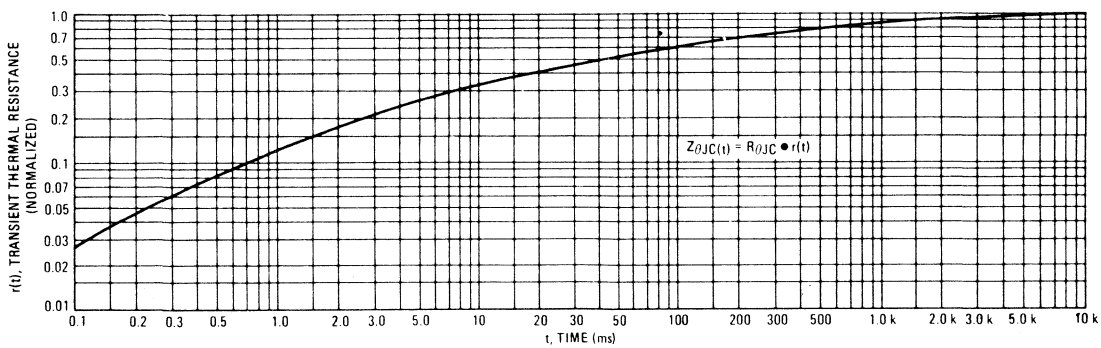


FIGURE 6 – THERMAL RESPONSE



6

TYPICAL CHARACTERISTICS

FIGURE 7 – PULSE TRIGGER CURRENT

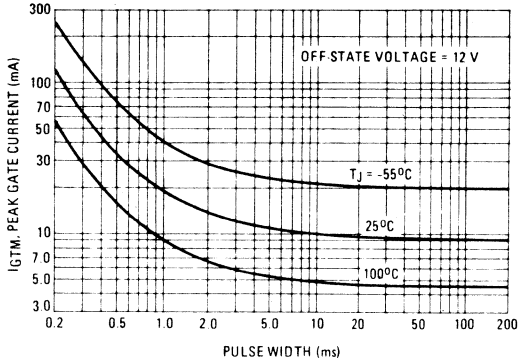


FIGURE 8 – GATE TRIGGER CURRENT

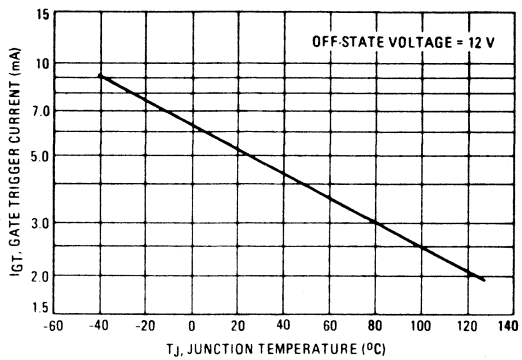


FIGURE 9 – GATE TRIGGER VOLTAGE

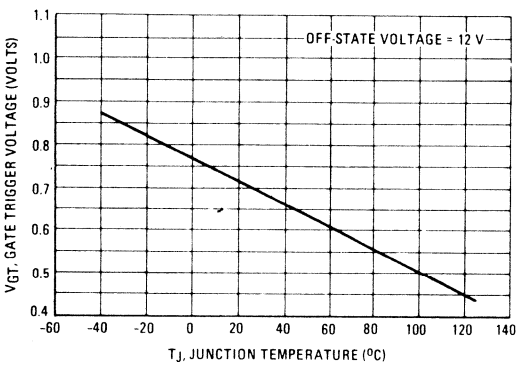
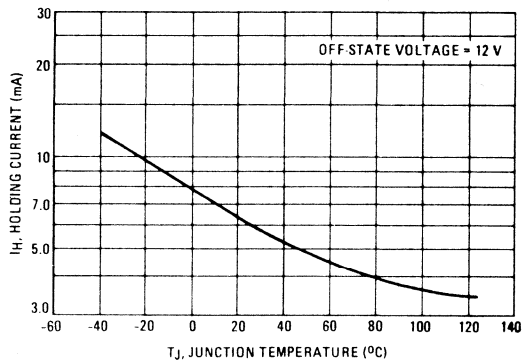


FIGURE 10 – HOLDING CURRENT



THYRISTOR APPLICATION NOTES

AN-189 Solid-State Pulse Width Modulation DC Motor Control

AN-240 SCR Power Control Fundamentals

AN-295 Suppressing RFI in Thyristor Circuits

AN-413 Unijunction Trigger Circuits for Gated Thyristors

AN-443 Directional and Speed Control for Series, Universal and Shunt Motors

AN-453 Zero Point Switching Techniques

AN-482 Electronic Speed Control of Appliance Motors

AN-526 Theory, Characteristics and Applications of Silicon Unilateral and Bilateral Switches

AN-527 Theory, Characteristics and Applications of the Programmable Unijunction Transistor

AN-568 A Fuse-Thyristor Coordinator Primer

AN-725 A Low-Cost 80-V-1.5 A Color TV Power Supply

AN-734 SCR Controller for a Series Field dc Motor

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Motorola Semiconductor Products, Inc.
P.O Box 20924
Phoenix, Arizona 85036

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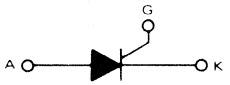


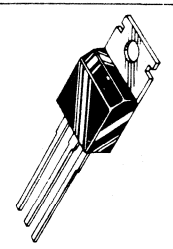
SILICON CONTROLLED RECTIFIERS

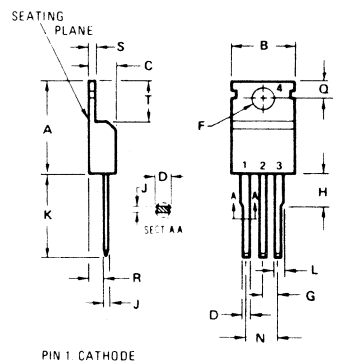
. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass Passivated Junctions with Center Gate Fire for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt▲ Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 800 Volts

THYRISTORS

16 AMPERES RMS
50-800 VOLTS





PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

All JEDEC dimensions and notes apply

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	–	6.35	–	0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

CASE 221-02
TO 220 AB

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage (1)	V_{RRM}		Volts
2N6400		50	
2N6401		100	
2N6402		200	
MCR221-5		300	
2N6403		400	
MCR221-7		500	
2N6404		600	
MCR221-9		700	
2N6405		800	
Forward Current RMS (T_C = 90°C) (All Conduction Angles)	$I_{T(RMS)}$	16	Amps
Peak Forward Surge Current (1/2 cycle, Sine Wave, 60 Hz, T_J = 125°C)	I_{TSM}	160	Amps
Circuit Fusing Considerations (T_J = -40 to +125°C, t = 1.0 to 8.3 ms)	I^2t	100	A^2s
Forward Peak Gate Power	P_{GM}	20	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watt
Forward Peak Gate Current	I_{GM}	2.0	Amps
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W

(1) V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

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*Indicates JEDEC Registered Data.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Voltage (T_J = 125°C)	2N6400	V_{DRM}	50	–	–	Volts
	2N6401		100	–	–	
	2N6402		200	–	–	
	MCR221-5		300	–	–	
	2N6403		400	–	–	
	MCR221-7		500	–	–	
	2N6404		600	–	–	
	MCR221-9		700	–	–	
	2N6405		800	–	–	
*Peak Forward Blocking Current (Rated V_{DRM} @ T_J = 125°C)		I_{DRM}	–	–	2.0	mA
*Peak Reverse Blocking Current (Rated V_{RRM} @ T_J = 125°C)		I_{RRM}	–	–	2.0	mA
*Forward "On" Voltage (I_{TM} = 32 A peak)		V_{TM}	–	–	1.7	Volts
*Gate Trigger Current (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms)		I_{GT}	–	5.0	30	mA
*Gate Trigger Voltage (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms)		V_{GT}	–	0.7	1.5	Volts
*Gate Non-Trigger Voltage (Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms, T_J = 125°C)		V_{GD}	0.2	–	–	Volts
*Holding Current (Anode Voltage = 12 Vdc)		I_H	–	6.0	40	mA
Turn-On Time (I_{TM} = 16 A, I_{GT} = 40 mAdc)		t_{gt}	–	1.0	–	μs
Turn-Off Time (V_{DRM} = rated voltage)		t_q				μs
(I_{TM} = 16 A, I_R = 16 A)			–	15	–	
(I_{TM} = 16 A, I_R = 16 A, T_J = 125°C)			–	35	–	
Forward Voltage Application Rate (T_J = 125°C)		dv/dt	–	50	–	V/μs

*Indicates JEDEC Registered Data.

FIGURE 1 – AVERAGE CURRENT DERATING

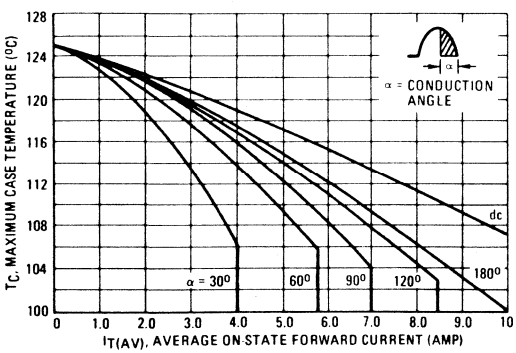


FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION

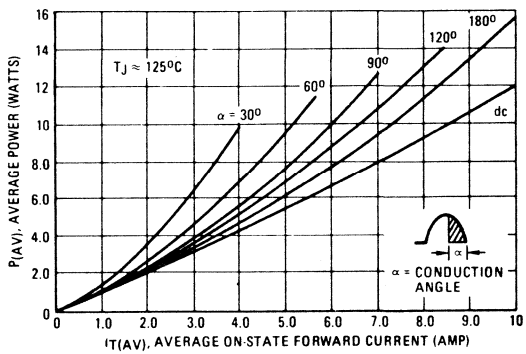


FIGURE 3 – ON-STATE CHARACTERISTICS

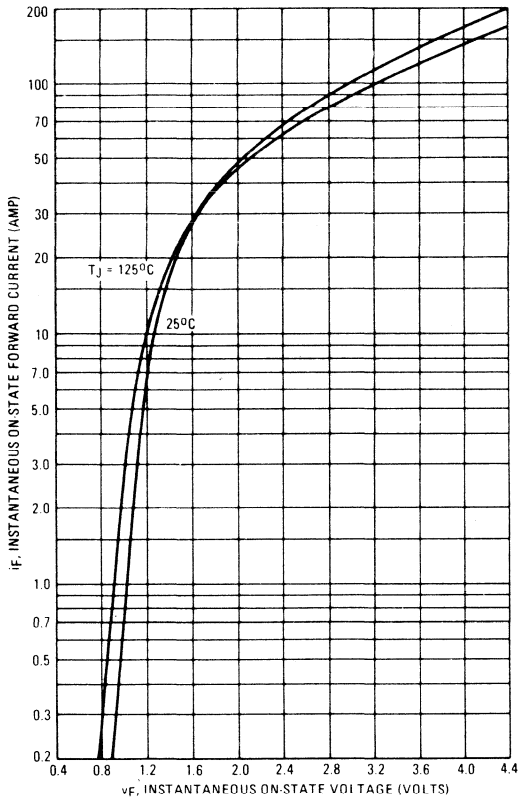


FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE CURRENT

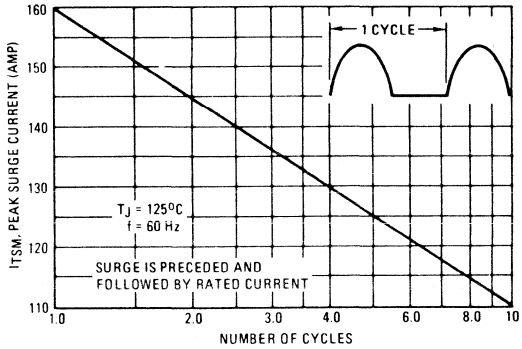


FIGURE 5 – CHARACTERISTICS AND SYMBOLS

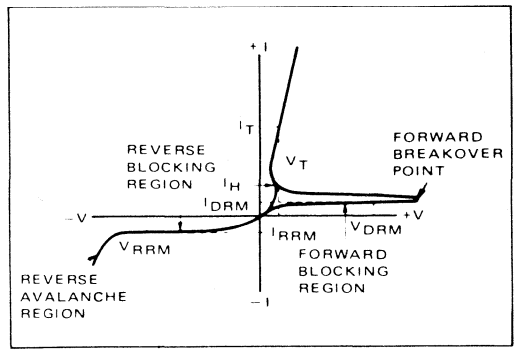
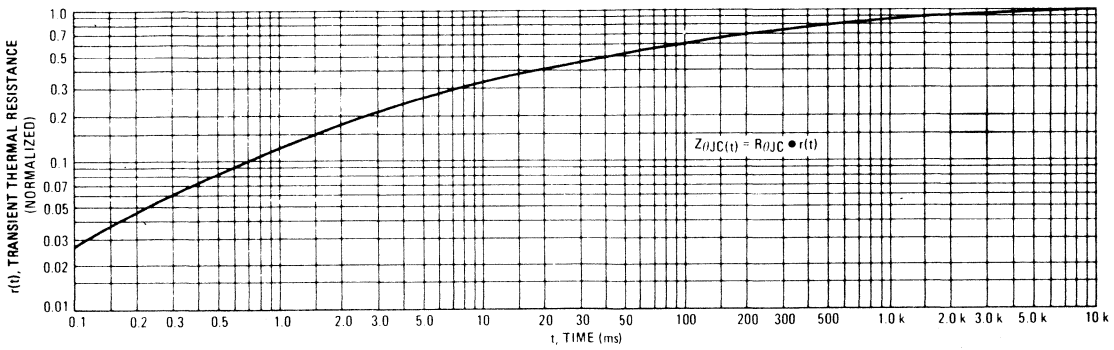


FIGURE 6 – THERMAL RESPONSE



6

TYPICAL TRIGGER CHARACTERISTICS

FIGURE 7 – GATE TRIGGER CURRENT

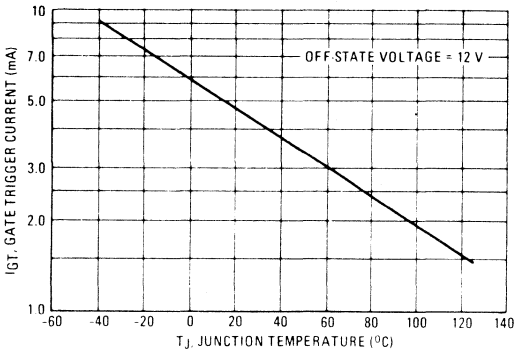


FIGURE 8 – GATE TRIGGER VOLTAGE

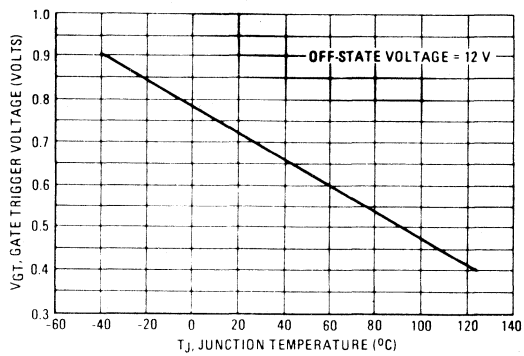
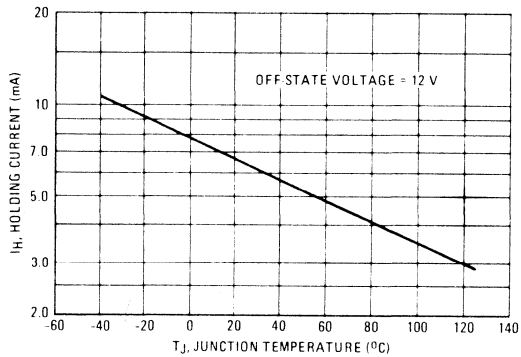


FIGURE 9 – HOLDING CURRENT



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2N2646
2N2647

SILICON ANNULAR♦ PN UNIJUNCTION TRANSISTORS

. . . designed for use in pulse and timing circuits, sensing circuits and thyristor trigger circuits. These devices feature:

- Low Peak Point Current – 2.0 μA (Max)
- Low Emitter Reverse Current – 200 nA (Max)
- Passivated Surface for Reliability and Uniformity

PN UNIJUNCTION TRANSISTORS

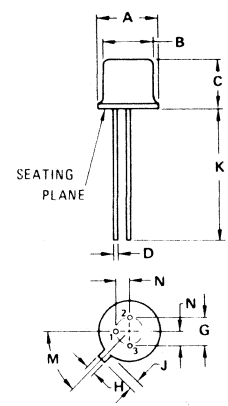
*MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Dissipation (1)	P_D	300	mW
RMS Emitter Current	$I_{E(RMS)}$	50	mA
Peak Pulse Emitter Current (2)	i_E	2.0	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Interbase Voltage	V_{B2B1}	35	Volts
Operating Junction Temperature Range	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

*Indicates JEDEC Registered Data.

(1) Derate 3.0 mW/°C increase in ambient temperature. The total power dissipation (available power to Emitter and Base-Two) must be limited by the external circuitry.

(2) Capacitor discharge – 10 μF or less, 30 volts or less.



STYLE 1:
PIN 1. EMITTER
2. BASE 1
3. BASE 2

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.48	0.016	0.019
G	2.54 TYP		0.100 TYP	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
M	45° TYP		45° TYP	
N	1.27 TYP		0.050 TYP	

CASE 22A

♦Annular Semiconductors Patented by Motorola Inc.

6

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio (V_{B2B1} = 10 V) (Note 1)	2N2646	η	0.56	–	0.75	–
	2N2647		0.68	–	0.82	
Interbase Resistance (V_{B2B1} = 3.0 V, I_E = 0)		r_{BB}	4.7	7.0	9.1	k ohms
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3.0 V, I_E = 0, T_A = -55°C to +125°C)		α_{rBB}	0.1	–	0.9	%/°C
Emitter Saturation Voltage (V_{B2B1} = 10 V, I_E = 50 mA) (Note 2)		$V_{EB1(sat)}$	–	3.5	–	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)		$I_{B2(mod)}$	–	15	–	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0)	2N2646	I_{EB2O}	–	0.005	12	μA
	2N2647		–	0.005	0.2	
Peak Point Emitter Current (V_{B2B1} = 25 V)	2N2646	I_P	–	1.0	5.0	μA
	2N2647		–	1.0	2.0	
Valley Point Current (V_{B2B1} = 20 V, R_{B2} = 100 ohms) (Note 2)	2N2646	I_V	4.0	6.0	–	mA
	2N2647		8.0	10	18	
Base-One Peak Pulse Voltage (Note 3, Figure 3)	2N2646	V_{OB1}	3.0	5.0	–	Volts
	2N2647		6.0	7.0	–	

*Indicates JEDEC Registered Data.

Notes:

(1) Intrinsic standoff ratio, η, is defined by equation:

$$\eta = \frac{V_P - V_F}{V_{B2B1}}$$

Where V_P = Peak Point Emitter Voltage
V_{B2B1} = Interbase Voltage
V_F = Emitter to Base-One Junction Diode Drop (≈0.5 V @ 10 μA)

(2) Use pulse techniques: PW ≈ 300 μs, duty cycle ≤ 2% to avoid internal heating due to interbase modulation which may result in erroneous readings.

(3) Base-One Peak Pulse Voltage is measured in circuit of Figure 3. This specification is used to ensure minimum pulse amplitude for applications in SCR firing circuits and other types of pulse circuits.

FIGURE 1
UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

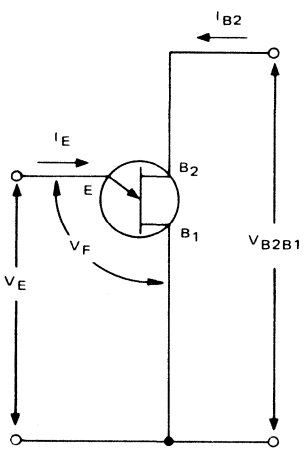


FIGURE 2
STATIC EMITTER CHARACTERISTIC CURVES
(Exaggerated to Show Details)

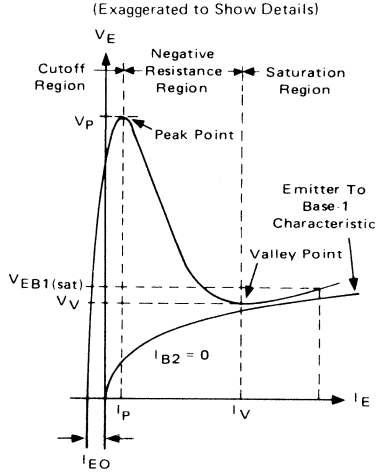
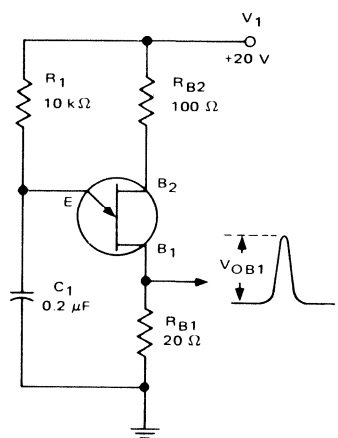
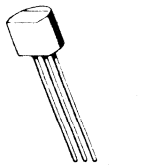


FIGURE 3 – V_{OB1} TEST CIRCUIT
(Typical Relaxation Oscillator)



2N4870
2N4871



CASE 29
(TO-92)

PN unijunction transistors designed for use in pulse and timing circuits, sensing circuits and thyristor trigger circuits.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
RMS Power Dissipation*	P_D*	300	mW
RMS Emitter Current	I_e	50	mA
Peak-Pulse Emitter Current**	i_e**	1.5	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Interbase Voltage†	V_{B2B1}†	35	Volts
Operating Junction Temperature Range	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

*Derate 3.0 mW/°C increase in ambient temperature.
**Duty cycle ≦ 1%, PRR = 10 PPS (see Figure 5).
†Based upon power dissipation at T_A = 25°C.

FIGURE 1 — UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

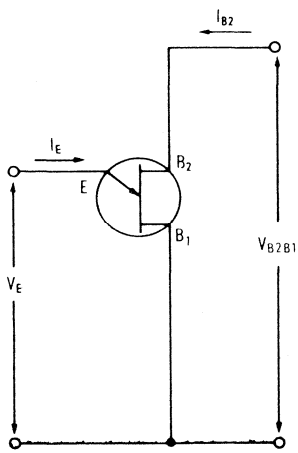
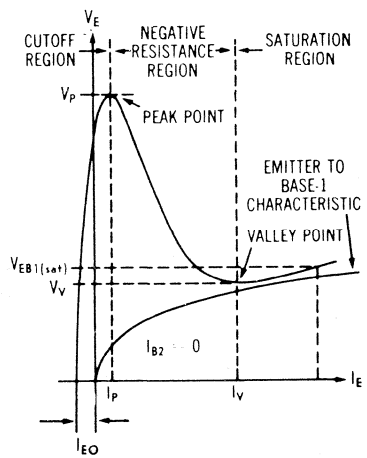


FIGURE 2 — STATIC EMITTER CHARACTERISTICS CURVES



6

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio* (V_{B2B1} = 10 V)	2N4870 2N4871	4, 7	η*	0.56 0.70	- -	0.75 0.85	-
Interbase Resistance (V_{B2B1} = 3.0 V, I_E = 0)		10, 11	R_{BB}	4.0	6.0	9.1	k ohms
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3.0 V, I_E = 0, T_A = -65 to +125°C)		11	αR_{BB}	0.10	-	0.90	%/°C
Emitter Saturation Voltage** (V_{B2B1} = 10 V, I_E = 50 mA)			$V_{EB1(sat)}$**	-	2.5	-	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)			$I_{B2(mod)}$	-	15	-	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0)		6	I_{EB2O}	-	0.005	1.0	μA
Peak-Point Emitter Current (V_{B2B1} = 25 V)		8, 9	I_P	-	1.0	5.0	μA
Valley-Point Current** (V_{B2B1} = 20 V, R_{B2} = 100 ohms)	2N4870 2N4871	12, 13	I_V**	2.0 4.0	5.0 7.0	- -	mA
Base-One Peak Pulse Voltage	2N4870 2N4871	3, 16	V_{OB1}	3.0 5.0	6.0 8.0	- -	Volts

* η Intrinsic standoff ratio, is defined in terms of peak-point voltage, V_P, by means of the equation: $V_P = \eta V_{B2B1} + V_F$, where V_F is approximately 0.49 volt at 25° C @ I_F = 10 μA and decreases with temperature at approximately 2.5 mV/°C. The test circuit is shown in Figure 4. Components R_1, C_1, and the UJT form a relaxation oscillator, the remaining circuitry serves as a peak-voltage detector. The forward drop of Diode D_1 compensates for V_F. To use, the "cal" button is pushed, and R_3 is adjusted to make the current meter, M_1, read full scale. When the "cal" button is released, the value of η is read directly from the meter, if full scale on the meter reads 1.0.

** Use pulse techniques: PW ≈ 300 μs, duty cycle ≤ 2.0% to avoid internal heating, which may result in erroneous readings.

FIGURE 3 — V_{OB1} TEST CIRCUIT

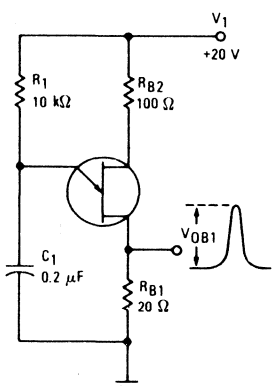


FIGURE 4 — η TEST CIRCUIT

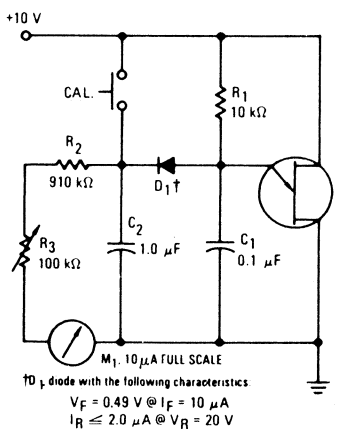
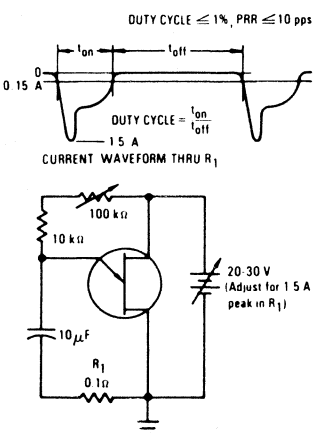


FIGURE 5 — PRR TEST CIRCUIT AND WAVEFORM



TYPICAL CHARACTERISTICS

FIGURE 6 — EMITTER REVERSE CURRENT

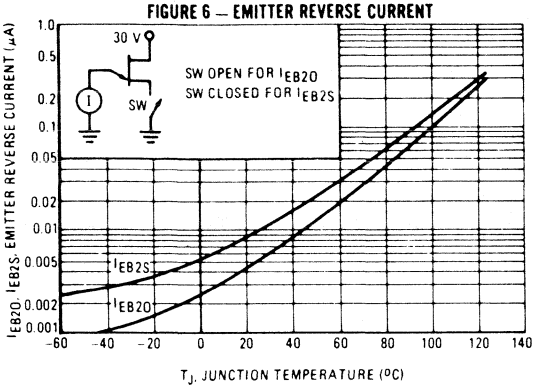
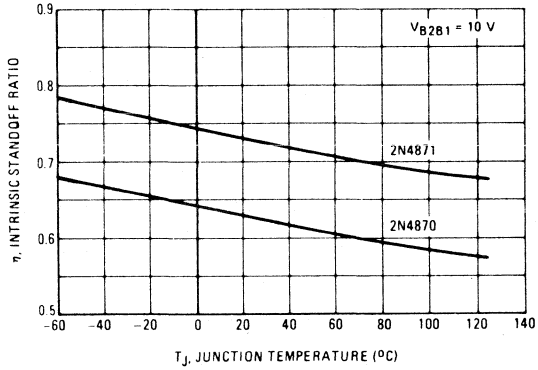


FIGURE 7 — INTRINSIC STANDOFF RATIO



PEAK POINT CURRENT

FIGURE 8 — EFFECT OF VOLTAGE

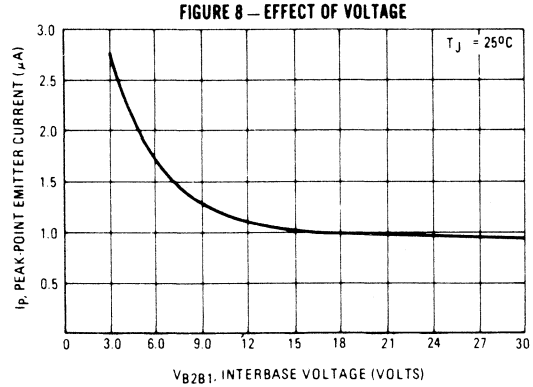
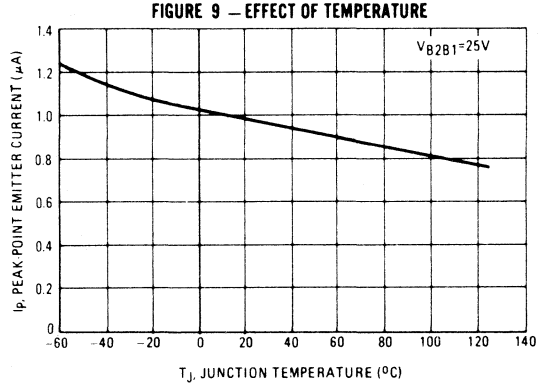


FIGURE 9 — EFFECT OF TEMPERATURE



INTERBASE RESISTANCE

FIGURE 10 — EFFECT OF VOLTAGE

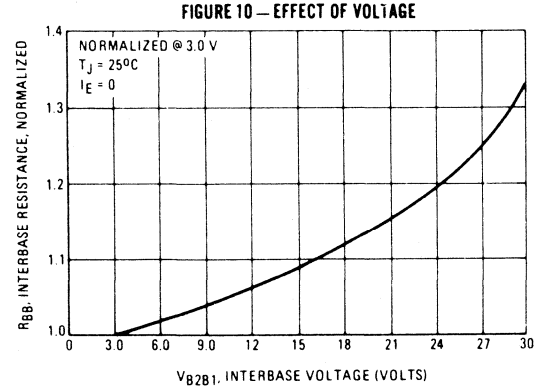
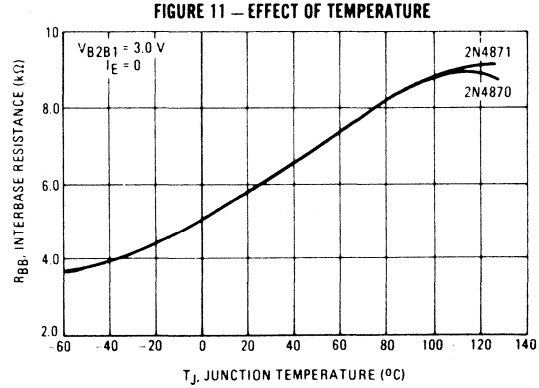


FIGURE 11 — EFFECT OF TEMPERATURE



6

TYPICAL CHARACTERISTICS

VALLEY CURRENT

FIGURE 12 — EFFECT OF VOLTAGE

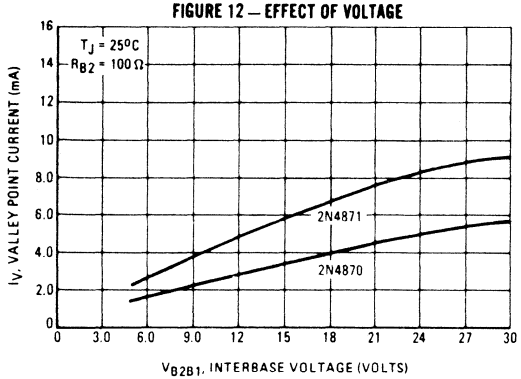
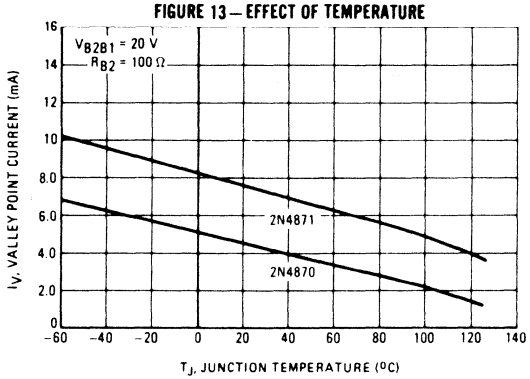


FIGURE 13 — EFFECT OF TEMPERATURE



VALLEY VOLTAGE

FIGURE 14 — EFFECT OF VOLTAGE

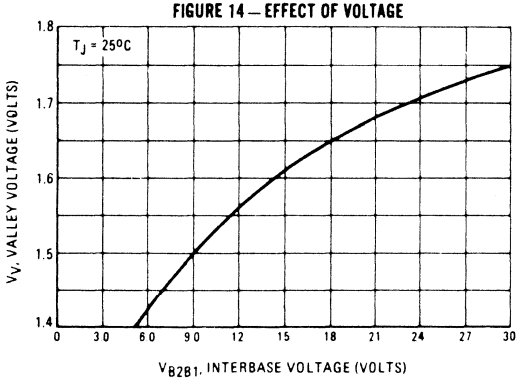


FIGURE 15 — EFFECT OF TEMPERATURE

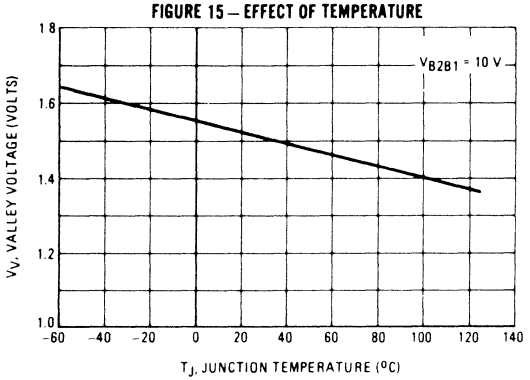
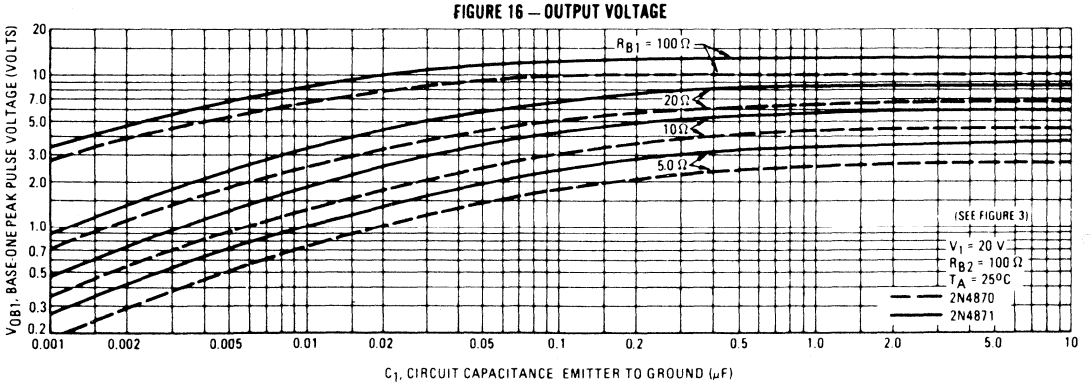
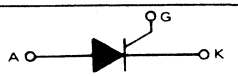


FIGURE 16 — OUTPUT VOLTAGE





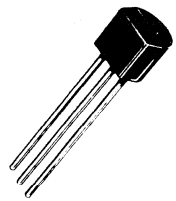
PLASTIC THYRISTORS

. . . Annular♦ PNPN devices designed for high volume consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive plastic TO-92 package which is readily adaptable for use in automatic insertion equipment.

- Sensitive Gate Trigger Current – 200 μA Maximum
- Low Reverse and Forward Blocking Current – 50 μA Maximum, T_C = 125°C
- Low Holding Current – 5.0 mA Maximum
- Passivated Surface for Reliability and Uniformity

PLASTIC SILICON CONTROLLED RECTIFIERS

0.8 AMPERE RMS
30 thru 200 VOLTS



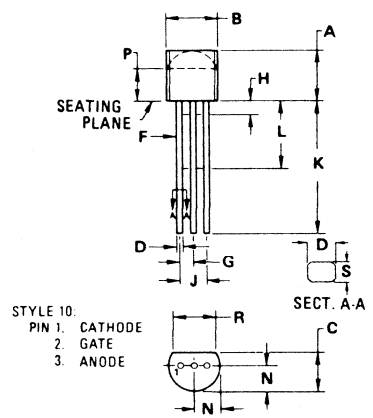
MAXIMUM RATINGS(1)

Rating	Symbol	Value	Unit
*Peak Repetitive Reverse Blocking Voltage (2) 2N5060 2N5061 2N5062 2N5063 2N5064	V_{RRM}	 30 60 100 150 200	Volts
On-State Current RMS (All Conduction Angles)	$I_{T(RMS)}$	0.8	Amp
*Average On-State Current (T_C = 67°C) (T_C = 102°C)	$I_{T(AV)}$	 0.51 0.255	Amp
*Peak Non-Repetitive Surge Current, T_A = 25°C (1/2 cycle, Sine Wave, 60 Hz)	I_{TSM}	6.0	Amp
Circuit Fusing Considerations, T_A = 25°C (t = 1.0 to 8.3 ms)	I^2t	0.15	A^2s
*Peak Gate Power, T_A = 25°C	P_{GM}	0.1	Watt
*Average Gate Power, T_A = 25°C	$P_{G(AV)}$	0.01	Watt
*Peak Forward Gate Current, T_A = 25°C (300 μs, 120 PPS)	I_{FGM}	1.0	Amp
*Peak Reverse Gate Voltage	V_{RGM}	5.0	Volts
*Operating Junction Temperature Range @ Rated V_{RRM} and V_{DRM}	T_J	-65 to +125	°C
*Storage Temperature Range	T_{stg}	-65 to +150	°C
*Lead Solder Temperature (Lead Length ≥ 1/16" from case, 10 s Max)	–	+230*	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	75	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W

(1) Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode. Devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.
(2) This measurement is made with the case mounted "flat side down" on a heat sink and held in position by means of a metal clamp over the curved surface.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

CASE 29-02
TO-92

♦Annular Semiconductor Patented by Motorola Inc.
*Indicates JEDEC Registered Data.

6

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Voltage (Note 1) (T_C = 125°C, R_{GK} = 1000 Ohms)	2N5060	V_{DRM}	30	–	–	Volts
	2N5061		60	–	–	
	2N5062		100	–	–	
	2N5063		150	–	–	
	2N5064		200	–	–	
*Peak Forward Blocking Current (Rated V_{DRM} @ T_C = 125°C, R_{GK} = 1000 Ohms)		I_{DRM}	–	–	50	μA
*Peak Reverse Blocking Current (Rated V_{RRM} @ T_C = 125°C, R_{GK} = 1000 Ohms)		I_{RRM}	–	–	50	μA
*Forward "On" Voltage (Note 2) (I_{TM} = 1.2 A peak @ T_A = 25°C)		V_{TM}	–	–	1.7	Volts
Gate Trigger Current (Continuous dc) (Note 3)	T_C = 25°C	I_{GT}	–	–	200	μA
*(Anode Voltage = 7.0 Vdc, R_L = 100 Ohms, R_{GK} = 1000 Ohms)	T_C = -65°C		–	–	350	
Gate Trigger Voltage (Continuous dc)	T_C = 25°C	V_{GT}	–		0.8	Volts
*(Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = -65°C		–		1.2	
(Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms)	T_C = 125°C	V_{GD}	0.1		–	
Holding Current	T_C = 25°C	I_H	–	–	5.0	mA
*(Anode Voltage = 7.0 Vdc, initiating current = 20 mA	T_C = -65°C		–	–	10	
Turn-On Time						μs
Delay Time		t_d	–	3.0	–	
Rise Time (I_{GT} = 1.0 mA, R_{GK} = 1.0 Ohm, V_{RRM} = 30 V, Forward Current = 1.0 A, di/dt = 6.0 A/μs)		t_r	–	0.2	–	
Turn-Off Time	2N5060,2N5061	tq	–	10	–	μs
(Forward Current = 1.0 A pulse, Pulse Width = 50 μs, 0.1% Duty Cycle, di/dt = 6.0 A/μs, dv/dt = 20 V/μs, I_{GT} = 1.0 mA, R_{GK} = 1.0 k Ohm)	2N5062,5063,5064		–	30	–	
Forward Voltage Application Rate (Rated V_{DRM}, R_{GK} = 1.0 k, Exponential)		dv/dt	–	300	–	V/μs

*Indicates JEDEC Registered Data.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage but positive gate voltage shall not be applied concurrently with a negative potential on the anode. When checking forward or reverse blocking capability, thyristor devices should not be tested with a constant current source in a manner that the voltage applied exceeds the rated blocking voltage.
2. Forward current applied for 1.0 ms maximum duration, duty cycle ≤ 1.0%.
3. R_{GK} current is not included in measurement.

CURRENT DERATING

FIGURE 1 – MAXIMUM CASE TEMPERATURE

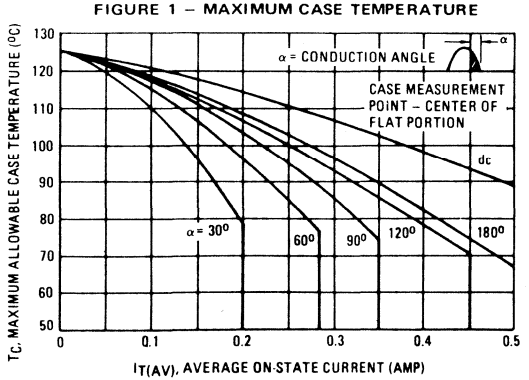


FIGURE 2 – MAXIMUM AMBIENT TEMPERATURE

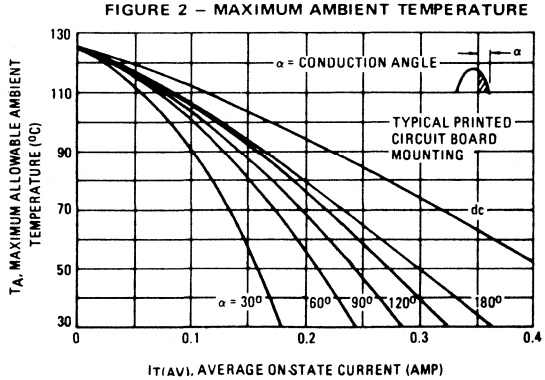


FIGURE 3 – TYPICAL FORWARD VOLTAGE

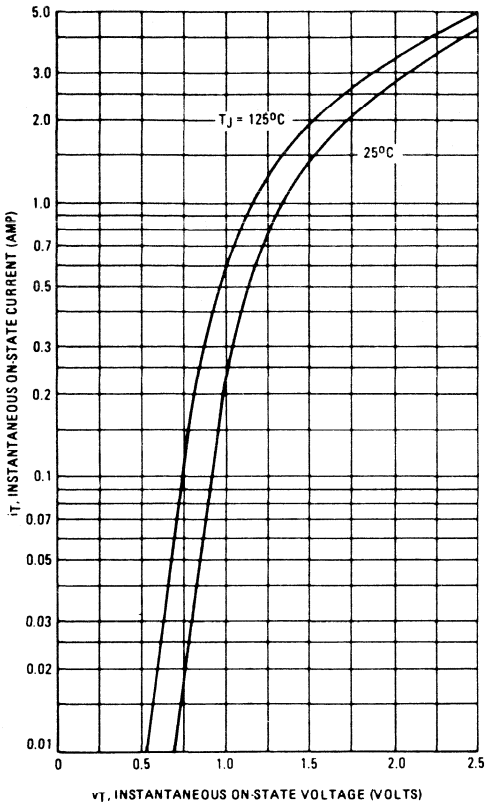


FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE CURRENT

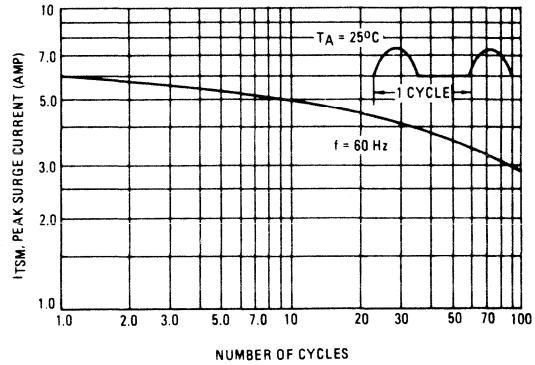


FIGURE 5 – POWER DISSIPATION

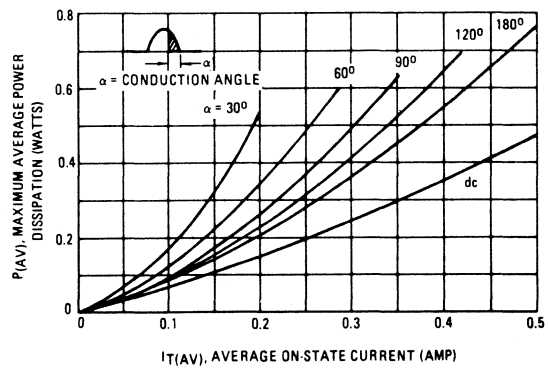
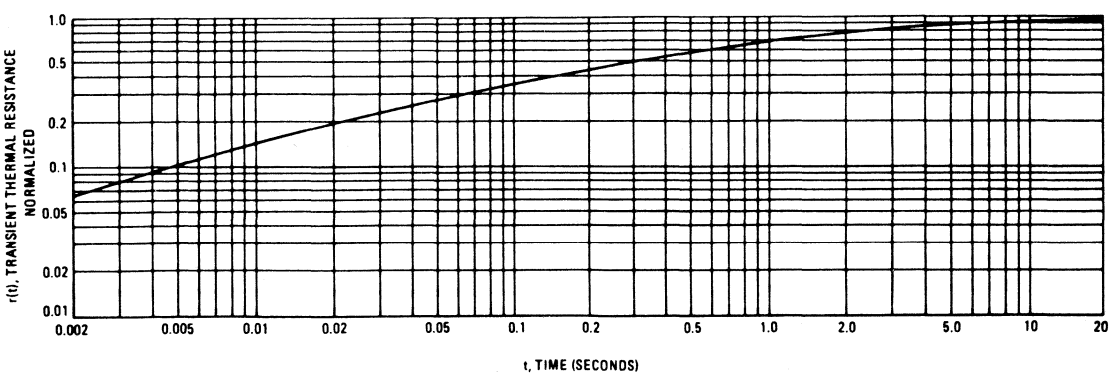


FIGURE 6 – THERMAL RESPONSE



6

TYPICAL CHARACTERISTICS

FIGURE 7 – GATE TRIGGER VOLTAGE

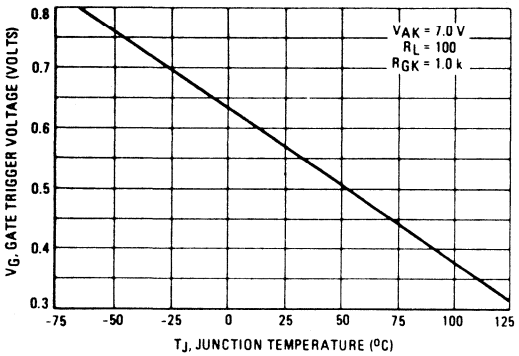


FIGURE 8 – GATE TRIGGER CURRENT

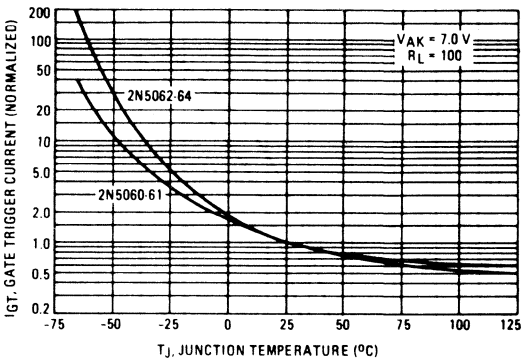


FIGURE 9 – HOLDING CURRENT

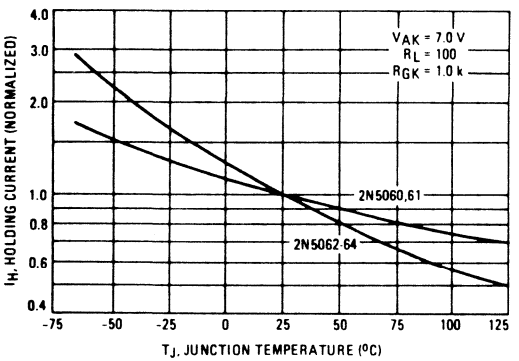
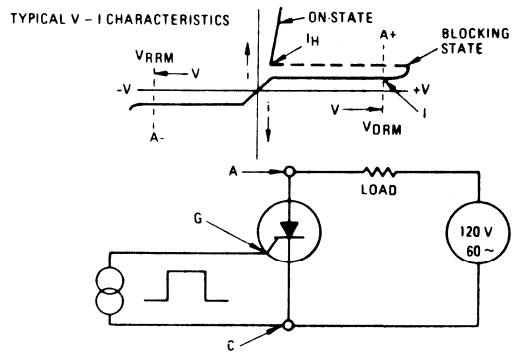


FIGURE 10 – CHARACTERISTICS AND SYMBOLS



THYRISTOR APPLICATION NOTES

AN-189 Solid-State Pulse Width Modulation DC Motor Control

AN-240 SCR Power Control Fundamentals

AN-295 Suppressing RFI in Thyristor Circuits

AN-413 Unijunction Trigger Circuits for Gated Thyristors

AN-441 SCR Slaving Circuits

AN-443 Directional and Speed Control for Series, Universal and Shunt Motors

AN-450 Induction Motor Speed Control

AN-453 Zero Point Switching Techniques

AN-482 Electronic Speed Control of Appliance Motors

AN-526 Theory, Characteristics and Applications of Silicon Unilateral and Bilateral Switches

AN-527 Theory, Characteristics and Applications of the Programmable Unijunction Transistor

AN-568 A Fuse-Thyristor Coordinator Primer

AN-580 Thermal Runaway in High Power Thyristors

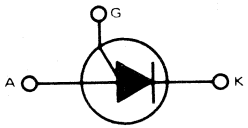
AN-597 Power Control Uisng the Zero Voltage Switch

AN-599 Mounting Techniques for Metal Packaged Power Semiconductors

To obtain copies of these notes list the AN number(s) on your company letterhead and send your request to:

Technical Information Center
Motorola Semiconductor Products, Inc.
P.O Box 20924
Phoenix, Arizona 85036

2N6027
2N6028



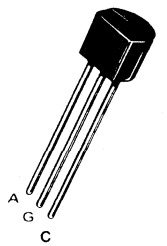
SILICON PROGRAMMABLE UNIJUNCTION TRANSISTORS

. . . designed to enable the engineer to "program" unijunction characteristics such as R_{BB}, η, I_V, and I_P by merely selecting two resistor values. Application includes thyristor-trigger, oscillator, pulse and timing circuits. These devices may also be used in special thyristor applications due to the availability of an anode gate. Supplied in an inexpensive TO-92 plastic package for high-volume requirements, this package is readily adaptable for use in automatic insertion equipment.

- Programmable – R_{BB}, η, I_V and I_P.
- Low On-State Voltage – 1.5 Volts Maximum @ I_F = 50 mA
- Low Gate to Anode Leakage Current – 10 nA Maximum
- High Peak Output Voltage – 11 Volts Typical
- Low Offset Voltage – 0.35 Volt Typical (R_G = 10 k ohms)

SILICON PROGRAMMABLE UNIJUNCTION TRANSISTORS

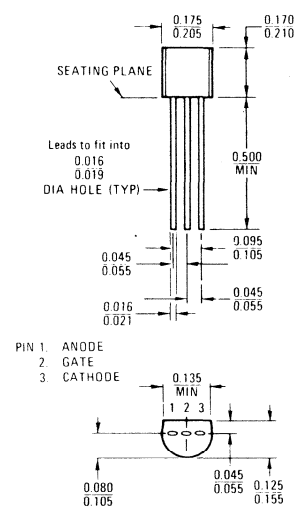
40 VOLTS
375 mW



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Dissipation(1) Derate Above 25°C	P_F $1/\theta_{JA}$	375 5.0	mW mW/°C
DC Forward Anode Current(2) Derate Above 25°C	I_T	200 2.67	mA mA/°C
*DC Gate Current	I_G	±50	mA
Repetitive Peak Forward Current 100 μs Pulse Width, 1.0% Duty Cycle *20 μs Pulse Width, 1.0% Duty Cycle	I_{TRM}	 1.0 2.0	 Amp Amp
Non-Repetitive Peak Forward Current 10 μs Pulse Width	I_{TSM}	5.0	Amp
*Gate to Cathode Forward Voltage	V_{GKF}	40	Volt
*Gate to Cathode Reverse Voltage	V_{GKR}	-5.0	Volt
*Gate to Anode Reverse Voltage	V_{GAR}	40	Volt
*Anode to Cathode Voltage	V_{AK}	±40	Volt
Operating Junction Temperature Range	T_J	-50 to +100	°C
*Storage Temperature Range	T_{stg}	-55 to +150	°C

*Indicates JEDEC Registered Data
(1) JEDEC Registered Data is 300 mW, derating at 4.0 mW/°C.
(2) JEDEC Registered Data is 150 mA.



All JEDEC dimensions and notes apply

CASE 29-03
TO-92
PLASTIC

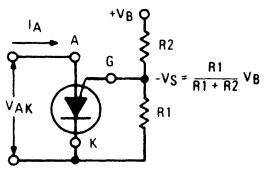
6

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

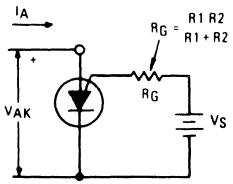
Characteristic		Figure	Symbol	Min	Typ	Max	Unit
•Peak Current		2,9,11	I_P				μA
(V_S = 10 Vdc, R_G = 1.0 MΩ)	2N6027			–	1.25	2.0	
	2N6028			–	0.08	0.15	
(V_S = 10 Vdc, R_G = 10 k ohms)	2N6027			–	4.0	5.0	
	2N6028			–	0.70	1.0	
•Offset Voltage		1	V_T				Volts
(V_S = 10 Vdc, R_G = 1.0 MΩ)	2N6027			0.2	0.70	1.6	
	2N6028			0.2	0.50	0.6	
(V_S = 10 Vdc, R_G = 10 k ohms)	(Both Types)			0.2	0.35	0.6	
*Valley Current		1,4,5,	I_V				μA
(V_S = 10 Vdc, R_G = 1.0 MΩ)	2N6027			–	18	50	
	2N6028			–	18	25	
(V_S = 10 Vdc, R_G = 10 k ohms)	2N6027			70	270	–	
	2N6028			25	270	–	
(V_S = 10 Vdc, R_G = 200 Ohms)	2N6027			1.5	–	–	mA
	2N6028			1.0	–	–	
* Gate to Anode Leakage Current		–	I_{GAO}				nAdc
(V_S = 40 Vdc, T_A = 25°C, Cathode Open)				–	1.0	10	
(V_S = 40 Vdc, T_A = 75°C, Cathode Open)				–	3.0	–	
Gate to Cathode Leakage Current (V_S = 40 Vdc, Anode to Cathode Shorted)		–	I_{GKS}	–	5.0	50	nAdc
*Forward Voltage (I_F = 50 mA Peak)		1,6	V_F	–	0.8	1.5	Volts
* Peak Output Voltage (V_B = 20 Vdc, C_C = 0.2 μF)		3,7	V_o	6.0	11	–	Volts
Pulse Voltage Rise Time (V_B = 20 Vdc, C_C = 0.2 μF)		3	t_r	–	40	80	ns

*Indicates JEDEC Registered Data

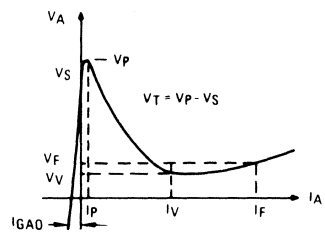
FIGURE 1 – ELECTRICAL CHARACTERIZATION



1A – PROGRAMMABLE UNIJUNCTION WITH "PROGRAM" RESISTORS R1 and R2



1B – EQUIVALENT TEST CIRCUIT FOR FIGURE 1A USED FOR ELECTRICAL CHARACTERISTICS TESTING (ALSO SEE FIGURE 2)



1C – ELECTRICAL CHARACTERISTICS

FIGURE 2 – PEAK CURRENT (I_P) TEST CIRCUIT

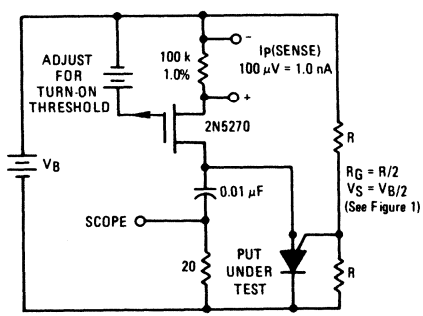
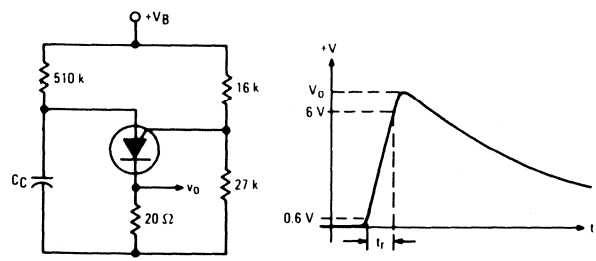


FIGURE 3 – V_o AND t_r TEST CIRCUIT



TYPICAL VALLEY CURRENT BEHAVIOR

FIGURE 4 – EFFECT OF SUPPLY VOLTAGE

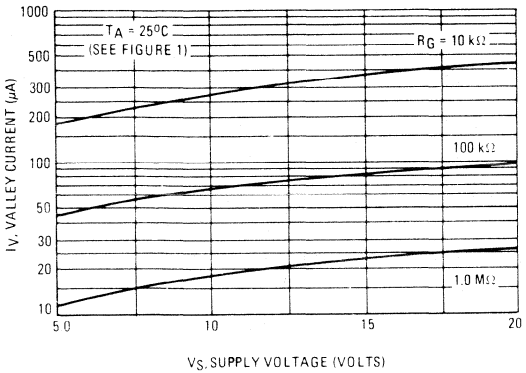


FIGURE 5 – EFFECT OF TEMPERATURE

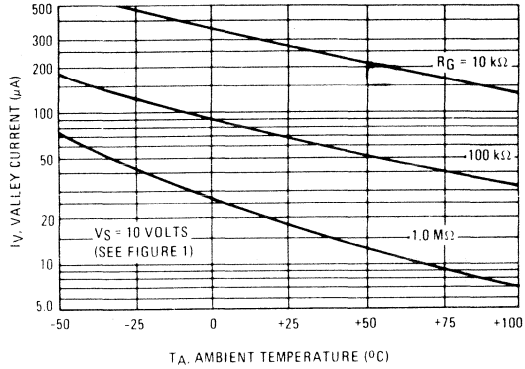


FIGURE 6 – FORWARD VOLTAGE

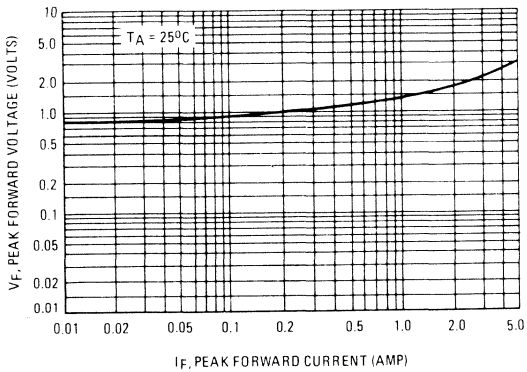


FIGURE 7 – PEAK OUTPUT VOLTAGE

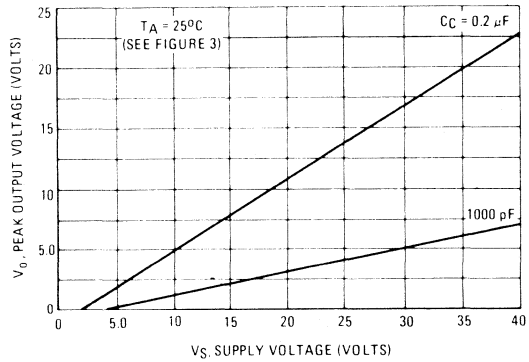
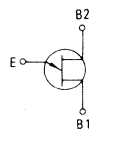
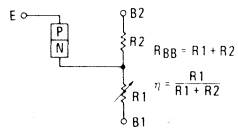


FIGURE 8 – STANDARD UNIJUNCTION COMPARED TO PROGRAMMABLE UNIJUNCTION

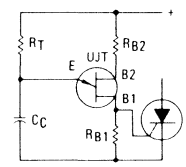
STANDARD UNIJUNCTION



CIRCUIT SYMBOL

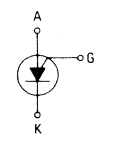


EQUIVALENT CIRCUIT

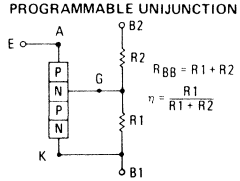


TYPICAL APPLICATION

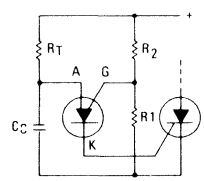
PROGRAMMABLE UNIJUNCTION



CIRCUIT SYMBOL



EQUIVALENT CIRCUIT
WITH EXTERNAL "PROGRAM"
RESISTORS R1 and R2



TYPICAL APPLICATION

6

TYPICAL PEAK CURRENT BEHAVIOR

2N6027

FIGURE 9 – EFFECT OF SUPPLY VOLTAGE AND R_G

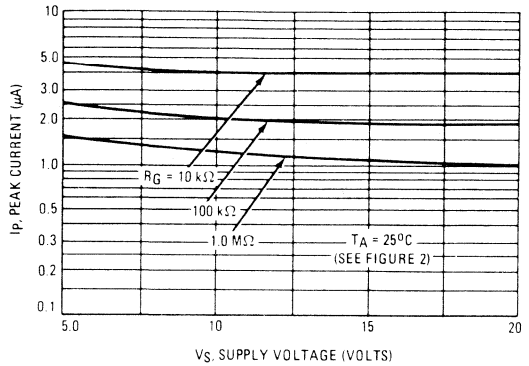
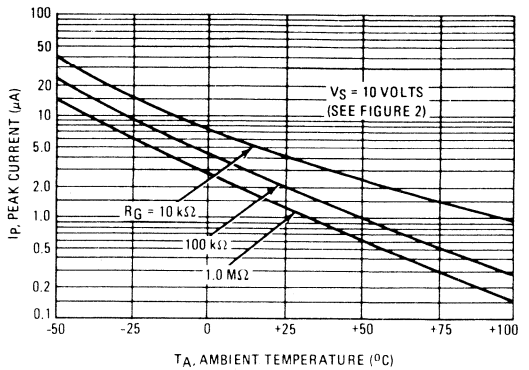


FIGURE 10 – EFFECT OF TEMPERATURE AND R_G



2N6028

FIGURE 11 – EFFECT OF SUPPLY VOLTAGE AND R_G

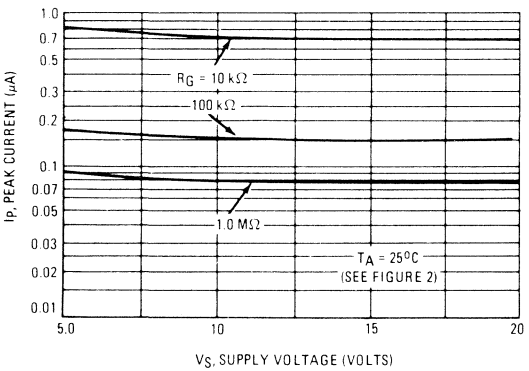
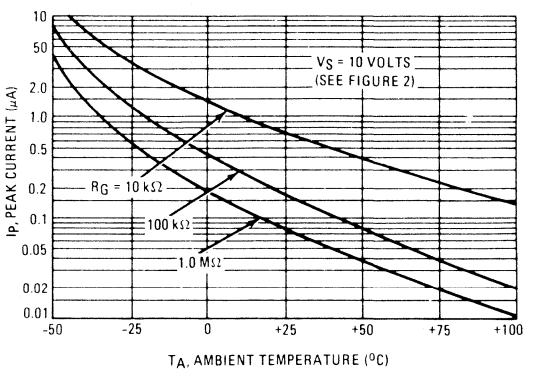
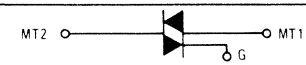


FIGURE 12 – EFFECT OF TEMPERATURE AND R_G





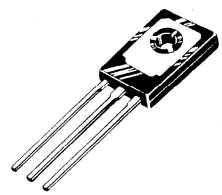
SILICON BIDIRECTIONAL THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Sensitive Gate Triggering (A and B versions) Uniquely Compatible for Direct Coupling to TTL, HTL, CMOS and Operational Amplifier Integrated Circuit Logic Functions.
- Gate Triggering 2 Mode – 2N6068 thru 2N6075
  4 Mode – 2N6068A,B thru 2N6075A,B
- Blocking Voltages to 600 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermopad Construction for Low Thermal Resistance, High Heat Dissipation and Durability

SENSITIVE GATE

TRIACS
(THYRISTORS)
4 AMPERES RMS
25 THRU 600 VOLTS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Repetitive Peak Off-State Voltage, Note 1 (T_J = 110°C) 2N6068,A,B	V_{DRM}	25	Volts
2N6069,A,B		50	
2N6070,A,B		100	
2N6071,A,B		200	
2N6072,A,B		300	
2N6073,A,B		400	
2N6074,A,B		500	
2N6075,A,B		600	
*On-State Current RMS (T_C = 85°C)	$I_{T(RMS)}$	4.0	Amp
*Peak Surge Current (One Full cycle, 60 Hz, T_J = -40 to +110°C)	I_{TSM}	30	Amp
Circuit Fusing Considerations (T_J = -40 to +110°C, t = 1.0 to 8.3 ms)	I^2t	3.6	A^2s
*Peak Gate Power	P_{GM}	10	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Gate Voltage	V_{GM}	5.0	Volts
*Operating Junction Temperature Range	T_J	-40 to +110	°C
*Storage Temperature Range	T_{stg}	-40 to +150	°C
Mounting Torque (6-32 Screw), Note 2	—	8.0	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R\theta JC$	3.5	°C/W
Thermal Resistance, Case to Ambient	$R\theta CA$	60	°C/W

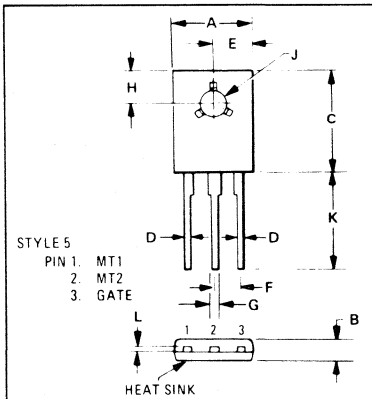
*Indicates JEDEC Registered Data

NOTES:

1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.
2. Torque rating applies with use of torque washer (Shakeproof WD19523 or equivalent). Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Main terminal 2 and heatsink contact pad are common.

   For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +200°C, for 10 seconds. Consult factory for lead bending options.

▲Trademark of Motorola Inc.



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.270	0.330	6.860	8.380
B	0.070	0.130	1.770	3.300
C	0.390	0.450	9.910	11.430
D	0.020	0.026	0.508	0.660
E	0.150 NOM		3.810 NOM	
F	0.090 TP		2.290 TP	
G	0.025	0.035	0.635	0.889
H	0.130	0.175	3.300	4.450
J	0.115	0.118	2.910	3.000
K	0.595	0.655	15.110	16.650
L	0.015	0.025	0.381	0.635

6

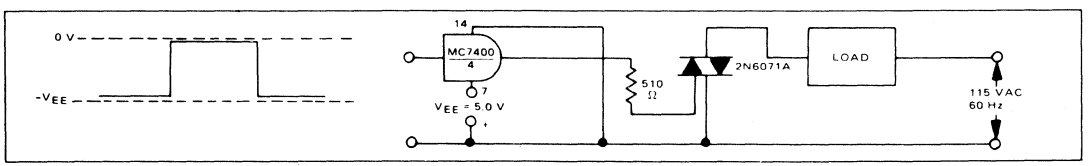
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

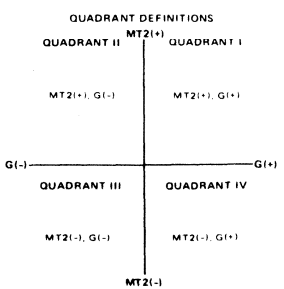
Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Blocking Current (Either Direction) Rated V_{DRM} @ T_J = 110°C, Gate Open	I_{DRM}	–	–	2.0	mA
*On-State Voltage (Either Direction) I_{TM} = 6.0 A Peak	V_{TM}	–	–	2.0	Volts
*Peak Gate Trigger Voltage	V_{GTM}				Volts
Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms, T_J = -40°C					
MT2 (+), G(+); MT2 (-), G(-) All Types		–	1.4	2.5	
MT2 (+), G(-); MT2 (-), G(+) 2N6068A,B thru 2N6075A,B		–	1.4	2.5	
Main Terminal Voltage = Rated V_{DRM}, R_L = 10 k ohms, T_J = 110°C					
MT2 (+), G(+); MT2 (-), G(-) All Types		0.2	–	–	
MT2 (+), G(-); MT2 (-), G(+) 2N6068A,B thru 2N6075A,B		0.2	–	–	
*Holding Current (Either Direction)	I_H				mA
Main Terminal Voltage = 12 Vdc, Gate Open, T_J = -40°C					
Initiating Current = 1.0 Adc					
2N6068 thru 2N6075		–	–	70	
2N6068A,B thru 2N6075A,B		–	–	30	
T_J = 25°C 2N6068 thru 2N6075		–	-	30	
2N6068A,B thru 2N6075A,B		–	–	15	
Turn-On Time (Either Direction) I_{TM} = 14 Adc, I_{GT} = 100 mAdc	t_{on}	–	1.5	–	μs
Blocking Voltage Application Rate at Commutation @ V_{DRM}, T_J = 85°C, Gate Open	dv/dt	–	5.0	–	V/μs

	Type	I_{GTM} @ T_J	QUADRANT (See Definition Below) I mA	II mA	III mA	IV mA
*Peak Gate Trigger Current Main Terminal Voltage = 12 Vdc, R_L = 100 ohms Maximum Value	2N6068 thru 2N6075	+25°C	30	–	30	–
		-40°C	60	–	60	–
	2N6068A thru 2N6075A	+25°C	5.0	5.0	5.0	10
		-40°C	20	20	20	30
	2N6068B thru 2N6075B	+25°C	3.0	3.0	3.0	5.0
		-40°C	15	15	15	20

*Indicates JEDEC Registered Data.

SAMPLE APPLICATION:
TTL-SENSITIVE GATE 4 AMPERE TRIAC TRIGGERS IN MODES II AND III





Trigger devices are recommended for gating on Triacs. They provide

1. Consistent predictable turn-on points
2. Simplified circuitry
3. Fast turn-on time for cooler, more efficient and reliable operation

For 2N6068 Thru 2N6075

ELECTRICAL CHARACTERISTICS of RECOMMENDED BIDIRECTIONAL SWITCHES

USAGE	General		Lamp Dimmer
PART NUMBER	MBS4991	MBS4992	MBS100
V_S	6.0 - 10 V	7.5 9.0 V	3.0 5.0 V
I_S	350 μA Max	120 μA Max	100 400 μA
$V_{S1} - V_{S2}$	0.5 V Max	0.2 V Max	0.35 V Max
Temperature Coefficient	0.02%/°C Typ		

See AN-526 for Theory and Characteristics of Silicon Bidirectional Switches

SENSITIVE GATE LOGIC REFERENCE

IC LOGIC FUNCTIONS	FIRING QUADRANT I	II	III	IV
TTL		2N6068A Series	2N6068A Series	
HTL		2N6068A Series	2N6068A Series	
McMOS (NAND)	2N6068B Series			2N6068B Series
McMOS (Buffer)		2N6068B Series	2N6068B Series	
Operational Amplifier	2N6068A Series			2N6068A Series
Zero Voltage Switch		2N6068A Series	2N6068A Series	

FIGURE 1 – AVERAGE CURRENT DERATING

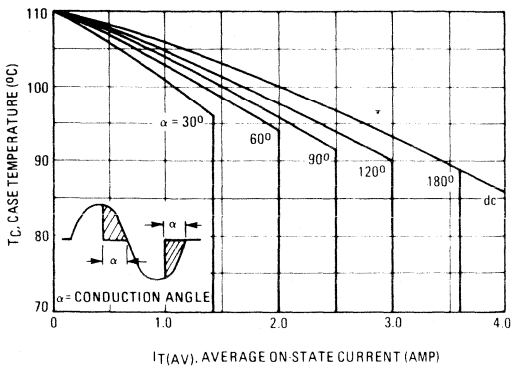


FIGURE 2 – RMS CURRENT DERATING

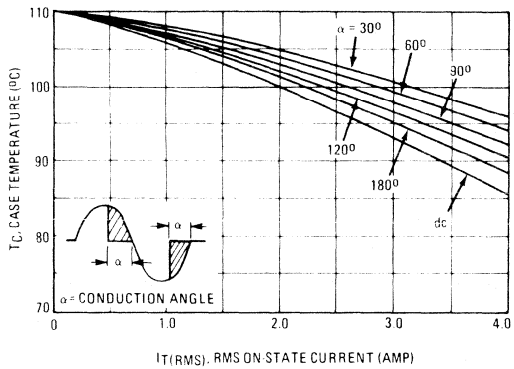


FIGURE 3 – POWER DISSIPATION

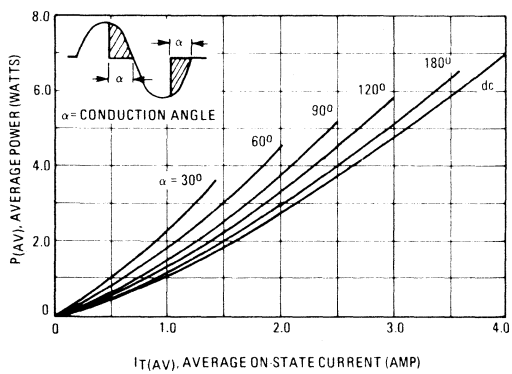


FIGURE 4 – POWER DISSIPATION

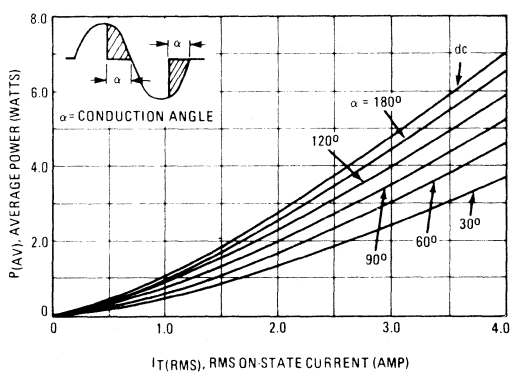


FIGURE 5 – TYPICAL GATE-TRIGGER VOLTAGE

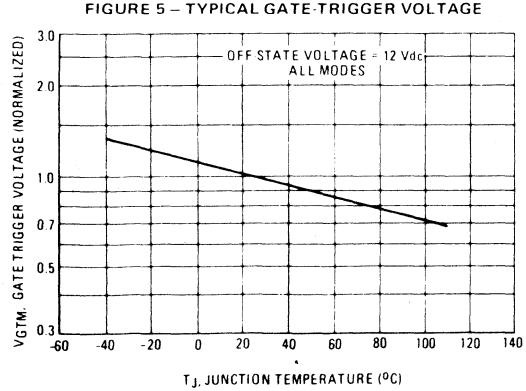
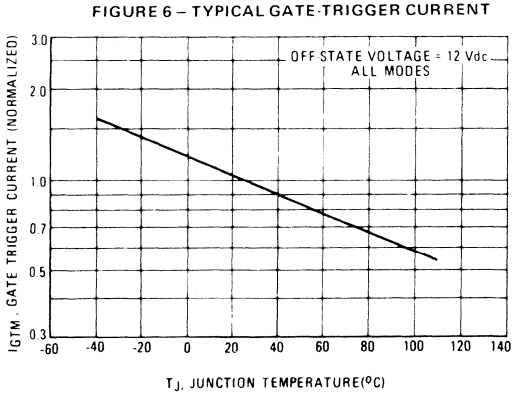


FIGURE 6 – TYPICAL GATE-TRIGGER CURRENT



6

FIGURE 7 MAXIMUM ON-STATE CHARACTERISTICS

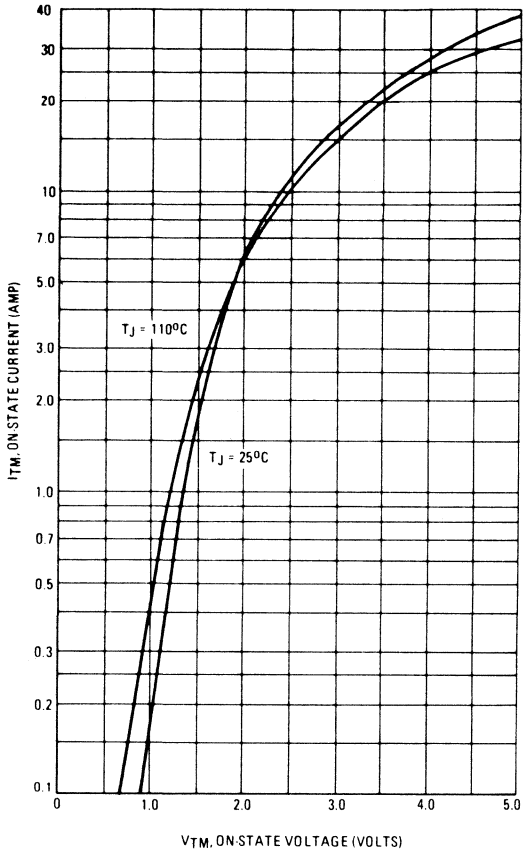


FIGURE 8 – TYPICAL HOLDING CURRENT

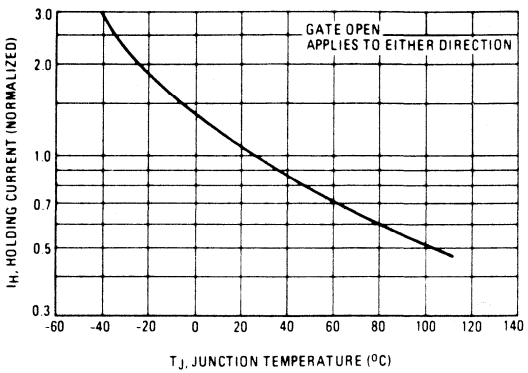


FIGURE 9 – MAXIMUM ALLOWABLE SURGE CURRENT

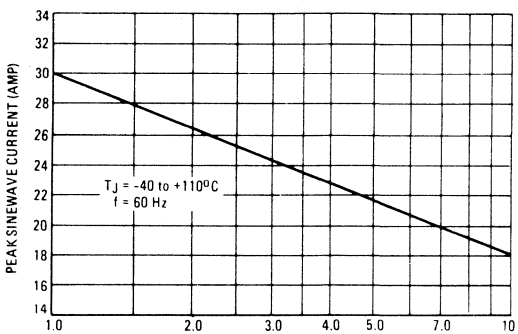
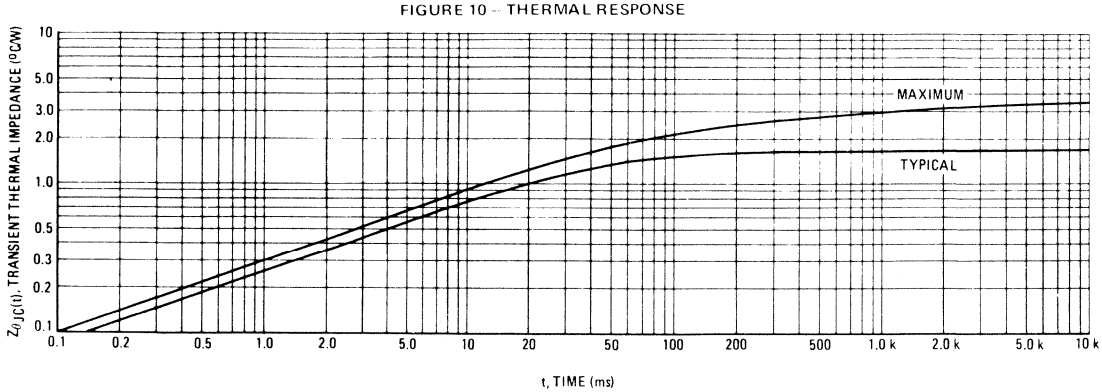


FIGURE 10 – THERMAL RESPONSE



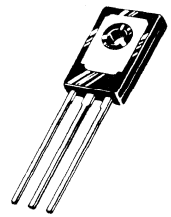
SILICON CONTROLLED RECTIFIERS

. . . PNPN devices designed for high volume consumer applications such as temperature, light, and speed control; process and remote control, and warning systems where reliability of operation is important.

- Passivated Surface for Reliability and Uniformity
- Power Rated at Economical Prices
- Practical Level Triggering and Holding Characteristics
- Flat, Rugged, Thermopad▲ Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Recommended Electrical Replacement for C 106

THYRISTORS

4.0 AMPERES RMS
30 thru 600 VOLTS



MAXIMUM RATINGS (T_J = 100°C unless otherwise noted.)

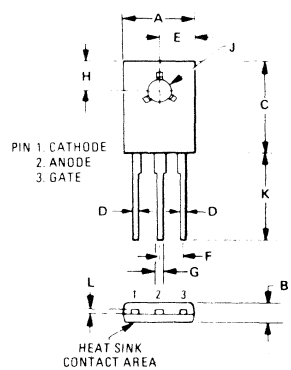
Rating		Symbol	Value	Unit
*Repetitive Peak Forward and Reverse Blocking Voltage (Note 1) (1/2 Sine Wave) (Gate Open, T_J = -40 to +110°C)	2N6236	V_{DRM}	30	Volts
	2N6237	V_{RRM}	50	
	2N6238		100	
	2N6239		200	
	2N6240		400	
	2N6241		600	
*Non-Repetitive Peak Reverse Blocking Voltage (1/2 Sine Wave, Gate Open, T_J = -40 to +110°C)	2N6236	V_{RSM}	50	Volts
	2N6237		100	
	2N6238		150	
	2N6239		250	
	2N6240		450	
	2N6241		650	
*Average On-State Current (T_C = -40 to +90°C) (T_C = +100°C)		$I_{T(AV)}$	2.6 1.6	Amp
*Surge On-State Current (1/2 Sine Wave, 60 Hz, T_C = +90°C) (1/2 Sine Wave, 1.5 ms, T_C = +90°C)		I_{TSM}	25 35	Amp
Circuit Fusing Considerations (T_J = -40 to +110°C, t = 1.0 to 8.3 ms)		I^2t	2.6	A^2s
*Peak Gate Power (Pulse Width = 10 μs)		P_{GM}	0.5	Watts
*Average Gate Power (t = 8.3 ms)		$P_{G(AV)}$	0.1	Watt
Peak Forward Gate Current		I_{GM}	0.2	Amp
Peak Reverse Gate Voltage		V_{RGM}	6.0	Volts
*Operating Junction Temperature Range		T_J	-40 to +110	°C
*Storage Temperature Range		T_{stg}	-40 to +150	°C
Mounting Torque (Note 2)		—	6.0	in.lb

THERMAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	—	3.0	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	—	75	°C/W

*Indicates JEDEC Registered Data.

▲Trademark of Motorola Inc.



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.270	0.330	6.860	8.380
B	0.070	0.130	1.770	3.300
C	0.390	0.450	9.910	11.430
D	0.020	0.026	0.508	0.660
E	0.150 NOM		3.810 NOM	
F	0.090 TP		2.290 TP	
G	0.025	0.035	0.635	0.889
H	0.130	0.175	3.300	4.450
J	0.115	0.118	2.910	3.000
K	0.595	0.655	15.110	16.650
L	0.015	0.025	0.381	0.635

CASE 77-02

6

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted, R_{GK} = 1000 ohms.)

Characteristics	Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Current (Note 1) (Rated V_{DRM}, T_J = 110°C)	I_{DRM}	–	–	200	μA
*Peak Reverse Blocking Current (Note 1) (Rated V_{RRM}, T_J = 110°C)	I_{RRM}	–	–	200	μA
*Peak Forward "On" Voltage (I_{TM} = 8.2 A Peak, Pulse Width = 1 to 2 ms, 2% Duty Cycle)	V_{TM}	–	–	2.2	Volts
Gate Trigger Current (Continuous dc) (V_{AK} = 12 Vdc, R_L = 24 Ohms) *(V_{AK} = 12 Vdc, R_L = 24 Ohms, T_C = -40°C)	I_{GT}	– –	– –	200 500	μA
Gate Trigger Voltage (Continuous dc) (Source Voltage = 12 V, R_S = 50 Ohms) *(V_{AK} = 12 Vdc, R_L = 24 Ohms, T_C = -40°C)	V_{GT}	–	–	1.0	Volts
Gate Non-Trigger Voltage (V_{AK} = Rated V_{DRM}, R_L = 100 Ohms, T_J = 110°C)	V_{GD}	0.2	–	–	Volts
Holding Current (V_{AK} = 12 Vdc, I_{GT} = 2.0 mA) T_J = 25°C *(Initiating On-State Current = 200 mA) T_J = -40°C	I_H	– –	– –	5.0 10	mA
*Total Turn-On Time (Source Voltage = 12 V, R_S = 6.0 k Ohms) (I_{TM} = 8.2 A, I_{GT} = 2.0 mA, Rated V_{DRM}) (Rise Time = 20 ns, Pulse Width = 10 μs)	t_{gt}	–	–	2.0	μs
Forward Voltage Application Rate (T_J = 110°C)	dv/dt	–	10	–	V/μs

*Indicates JEDEC Registered Data

NOTES:

1. Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode. Devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.
2. Torque rating applies with use of torque washer (Shakeproof WD19523 or equivalent). Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Anode lead and heatsink contact pad are common. (See AN-290 B)

   For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +225°C. For optimum results, an activated flux (oxide removing) is recommended.

CURRENT DERATING

FIGURE 1 – MAXIMUM CASE TEMPERATURE

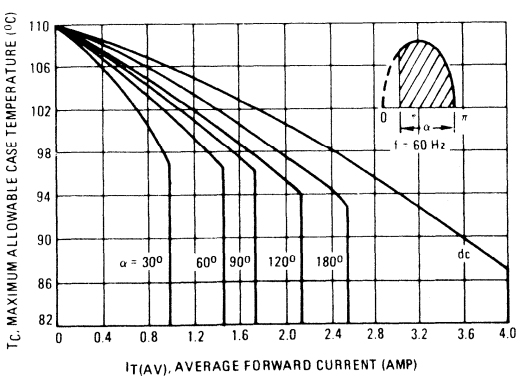
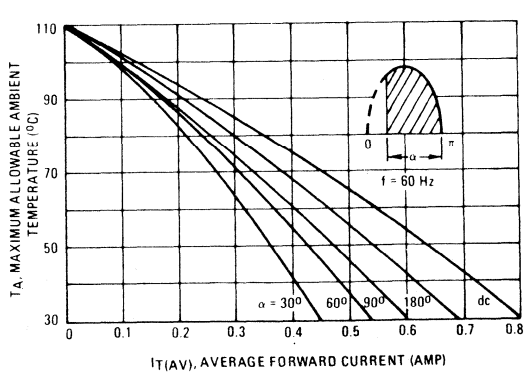
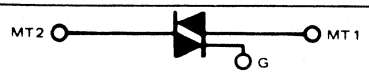


FIGURE 2 – MAXIMUM AMBIENT TEMPERATURE



2N6342 thru 2N6349
MAC220 Series • MAC221 Series

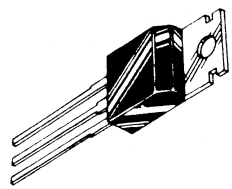


SILICON BIDIRECTIONAL THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt▲ Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Two Modes (2N6342, 2N6343, 2N6344, 2N6345, MAC220 Series) or Four Modes (2N6346, 2N6347, 2N6348,2N6349,MAC221 Series)
- For 400 Hz Operation, Consult Factory
- 12 Ampere Devices Available as 2N6342A thru 2N6349A

TRIACS
(THYRISTORS)
8 AMPERES RMS
200-800 VOLTS



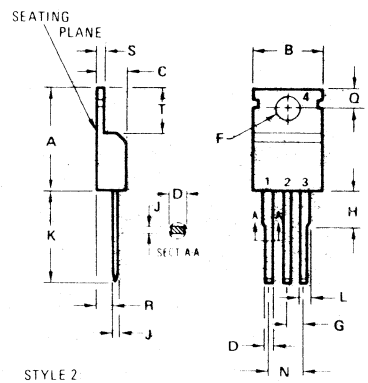
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
* Repetitive Peak Off-State Voltage, Note 1 (T_J = -40 to +100°C) ½ Sine Wave 50 to 60 Hz, Gate Open	V_{DRM}		Volts
MAC220-2,MAC221-2		50	
MAC220-3,MAC221-3		100	
2N6342,2N6346		200	
MAC220-5,MAC221-5		300	
2N6343,2N6347		400	
MAC220-7,MAC221-7		500	
2N6344,2N6348		600	
MAC220-9,MAC221-9		700	
2N6345,2N6349		800	
*Peak Gate Voltage	V_{GM}	10	Volts
*On-State Current RMS (T_C = +80°C) Full Cycle Sine Wave 50 to 60 Hz (T_C = +90°C)	$I_{T(RMS)}$	8.0 4.0	Amp
*Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T_J = +80°C) preceded and followed by 10 Rated Current	I_{TSM}	100	Amp
Circuit Fusing Considerations (T_J = -40 to +100°C, t = 1.0 to 8.3 ms)	I^2t	40	A^2s
*Peak Gate Power (T_C = +80°C, Pulse Width = 2.0 μs)	P_{GM}	20	Watts
*Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
*Peak Gate Current	I_{GM}	2.0	Amp
*Operating Junction Temperature Range	T_J	-40 to +100	°C
*Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
* Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W

*Indicates JEDEC Registered Data
▲Trademark of Motorola Inc.



STYLE 2
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	—	6.35	—	0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

CASE 221-02
TO-220 AB

All JEDEC dimensions and notes apply

6

ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted)

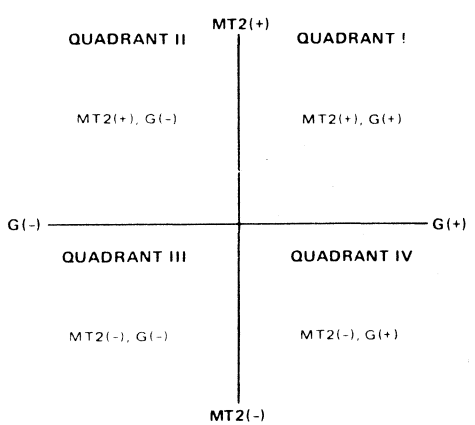
Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Blocking Current (Either Direction) Rated V_{DRM} @ T_J = 100°C, Gate Open	I_{DRM}	–	–	2.0	mA
*Peak On-State Voltage (Either Direction) I_{TM} = 11 A Peak; Pulse Width = 1.0 to 2.0 ms, Duty Cycle ≤ 2.0 %	V_{TM}	–	1.3	1.55	Volts
Gate Trigger Current, Continuous dc Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 μs	I_{GT}				mA
MT2 (+), G(+) All Types		–	12	50	
MT2 (+), G(–) 2N6346 thru 49,MAC221		–	12	75	
MT2 (–), G(–) All Types		–	20	50	
MT2 (–), G(+) 2N6346 thru 49,MAC221		–	35	75	
*MT2 (+), G(+); MT2 (–), G(–) T_C = -40°C All Types		–	–	100	
*MT2 (+), G(–); MT2 (–), G(+) T_C = -40°C 2N6346 thru 49,MAC221		–	–	125	
Gate Trigger Voltage, Continuous dc Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 μs	V_{GT}				Volts
MT2 (+), G(+) All Types		–	0.9	2.0	
MT2 (+), G(–) 2N6346 thru 49, MAC221		–	0.9	2.5	
MT2 (–), G(–) All Types		–	1.1	2.0	
MT2 (–), G(+) 2N6346 thru 49, MAC221		–	1.4	2.5	
*MT2 (+), G(+), MT2 (–), G(–) T_C = -40°C All Types		–	–	2.5	
*MT2 (+), G(–); MT2 (–), G(+) T_C = -40°C 2N6346 thru 49, MAC221		–	–	3.0	
Main Terminal Voltage = Rated V_{DRM}, R_L = 10 k ohms, T_J = 100°C					
*MT2 (+), G(+); MT2 (–), G(–) All Types		0.2	–	–	
*MT2 (+), G(–), MT2 (–), G(–) 2N6346 thru 49, MAC221		0.2	–	–	
Holding Current (Either Direction) Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current = 200 mA — T_C = 25°C	I_H	–	6.0	40	mA
— T_C = -40°C		–	–	75*	
*Turn-On Time Rated V_{DRM}, I_{TM} = 11 A, I_{GT} = 120 mA, Rise Time = 0.1 μs, Pulse Width = 2.0 μs	tgt	–	1.5	2.0	μs
Critical Rate of Rise of Commutation Voltage Rated V_{DRM}, I_{TM} = 11 A, Commutating di/dt = 4.3 A/ms, Gate Unenergized, T_C = 80°C	dv/dt	–	5.0	–	V/μs

*Indicates JEDEC Registered Data

NOTES:

1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

QUADRANT DEFINITIONS



Trigger devices are recommended for gating on Triacs. They provide:

1. Consistent predictable turn-on points.
2. Simplified circuitry.
3. Fast turn-on time for cooler, more efficient and reliable operation.

ELECTRICAL CHARACTERISTICS of RECOMMENDED BIDIRECTIONAL SWITCHES

USAGE	General	
PART NUMBER	MBS4991	MBS4992
V_S	6.0 – 10 V	7.5 – 9.0 V
I_S	350 μA Max	120 μA Max
$V_{S1} - V_{S2}$	0.5 V Max	0.2 V Max
Temperature Coefficient	0.02%/°C Typ	

See AN-526 for Theory and Characteristics of Silicon Bidirectional Switches.

FIGURE 1 – AVERAGE CURRENT DERATING

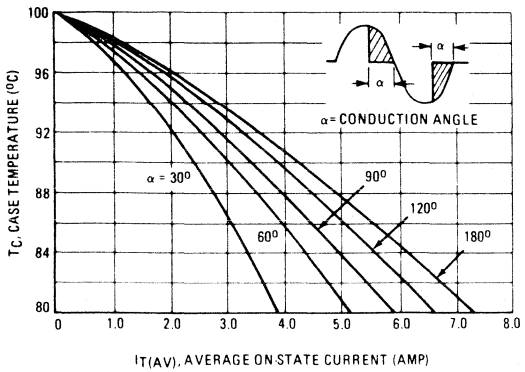


FIGURE 2 – RMS CURRENT DERATING

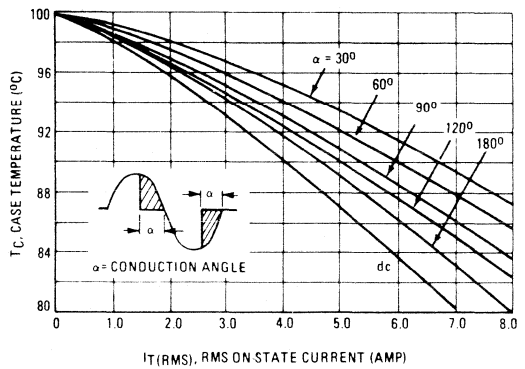


FIGURE 3 – ON-STATE POWER DISSIPATION

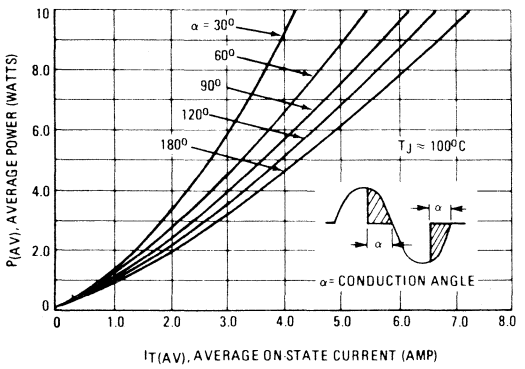


FIGURE 4 – ON-STATE POWER DISSIPATION

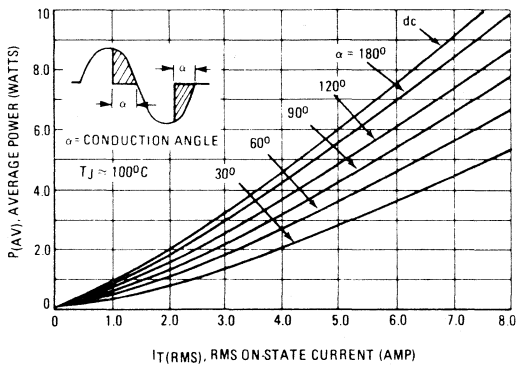


FIGURE 5 – TYPICAL GATE TRIGGER VOLTAGE

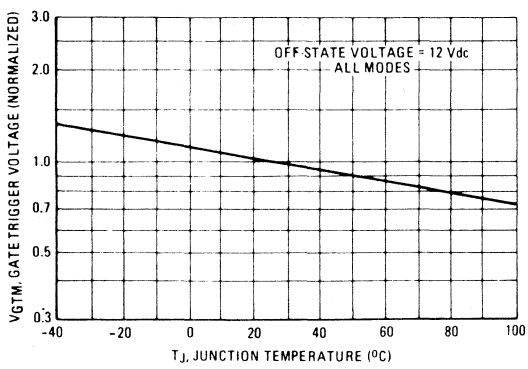


FIGURE 6 – TYPICAL GATE TRIGGER CURRENT

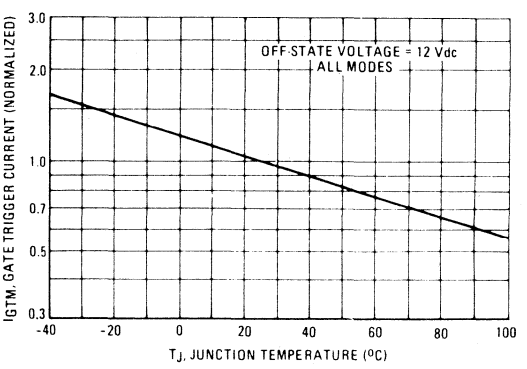


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FIGURE 7 – MAXIMUM ON-STATE CHARACTERISTICS

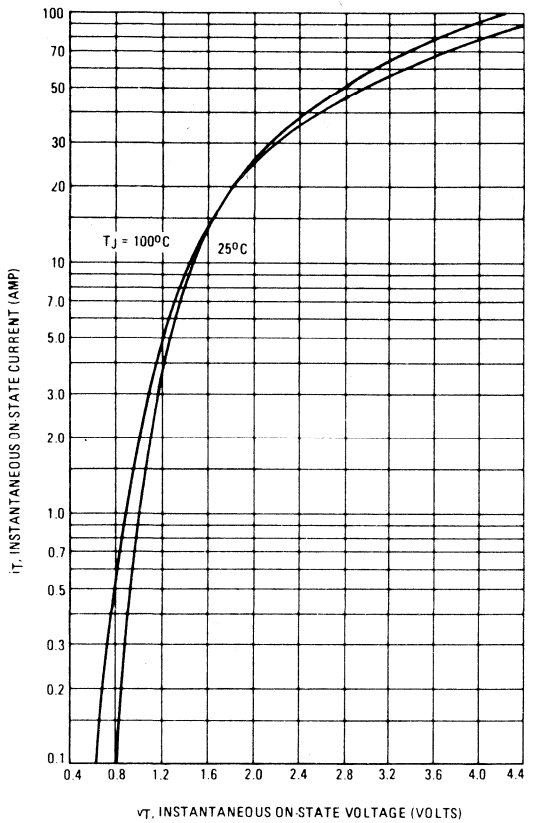


FIGURE 8 – TYPICAL HOLDING CURRENT

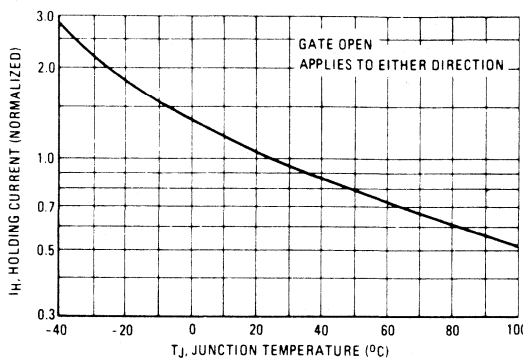


FIGURE 9 – MAXIMUM NON-REPETITIVE SURGE CURRENT

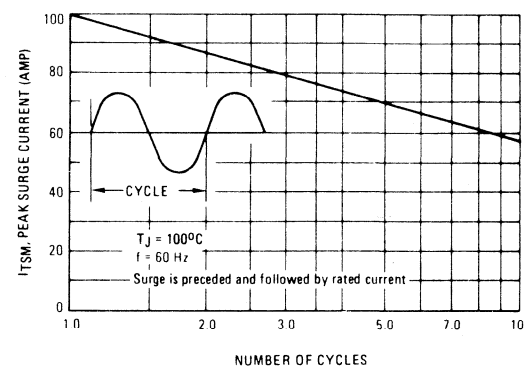
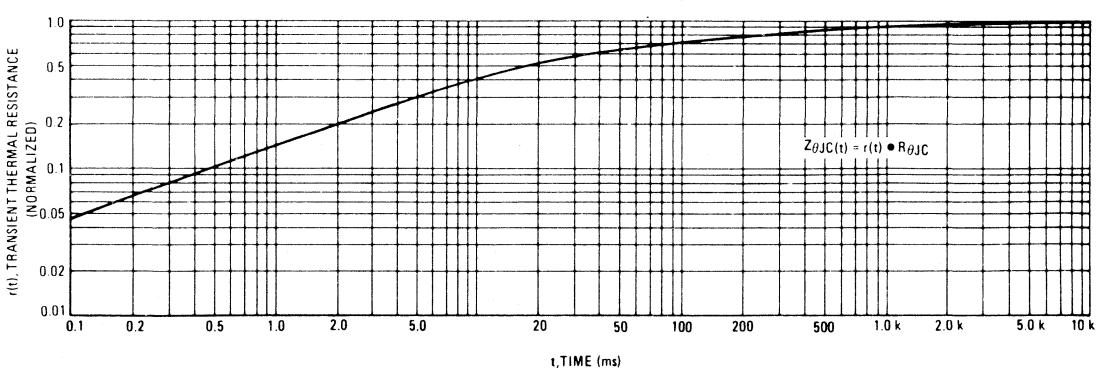
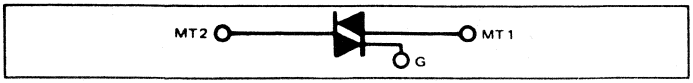


FIGURE 10 – THERMAL RESPONSE



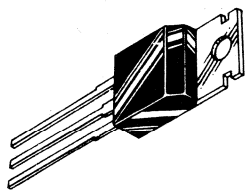


SILICON BIDIRECTIONAL THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Two Modes (2N6342A, 2N6343A, 2N6344A, 2N6345A) or Four Modes (2N6346A, 2N6347A, 2N6348A, 2N6349A)
- For 400 Hz Operation, Consult Factory
- 8 Ampere Devices Available as 2N6342 thru 2N6349

TRIACS
(THYRISTORS)
12 AMPERES RMS
200 – 800 VOLTS



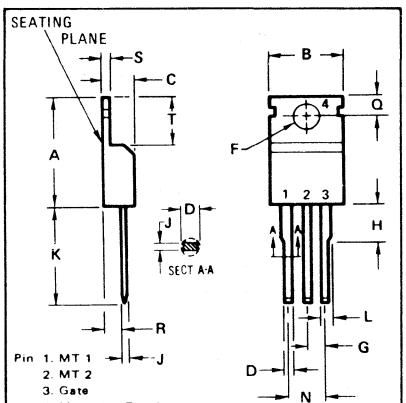
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Repetitive Peak Off-State Voltage, Note 1 (T_J = -40 to +110°C) ½ Sine Wave 50 to 60 Hz, Gate Open	V_{DRM}		Volts
2N6342A, 2N6346A		200	
2N6343A, 2N6347A		400	
2N6344A, 2N6348A		600	
2N6345A, 2N6349A		800	
*Peak Gate Voltage	V_{GM}	10	Volts
*On-State Current RMS (T_C = +80°C) Full Cycle Sine Wave 50 to 60 Hz (T_C = +95°C)	$I_{T(RMS)}$	12 6.0	Amp
*Peak Surge Current (One Full Cycle, 60 Hz, T_C = +80°C) preceded and followed by rated current	I_{TSM}	120	Amp
Circuit Fusing Considerations (T_J = -40 to +110°C, t = 1.0 to 8.3 ms)	I^2t	40	A^2s
*Peak Gate Power (T_C = +80°C, Pulse Width = 2.0 μs	P_{GM}	20	Watts
*Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
*Peak Gate Current	I_{GM}	2.0	Amp
*Operating Junction Temperature Range	T_J	-40 to +110	°C
*Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTIC

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R\theta_{JC}$	2.0	°C/W

*Indicates JEDEC Registered Data.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	–	6.35	–	0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

CASE 221-02
TO 220 AB
All JEDEC dimensions and notes apply

6

ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted)

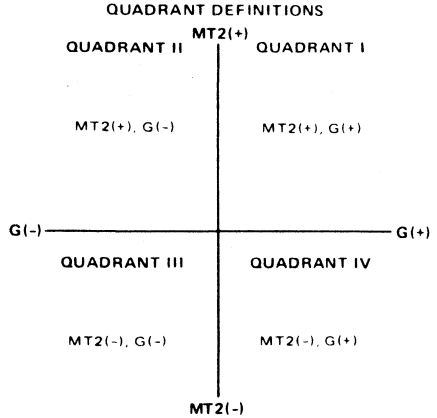
Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Blocking Current (Either Direction) Rated V_{DRM} @ T_J = 110°C, Gate Open	I_{DRM}	–	–	2.0	mA
*Peak On-State Voltage (Either Direction) I_{TM} = 17 A Peak; Pulse Width = 1.0 to 2.0 ms, Duty Cycle ≤ 2.0 %	V_{TM}	–	1.3	1.75	Volts
Peak Gate Trigger Current Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 μs	I_{GTM}				mA
MT2 (+), G(+) All Types		–	6.0	50	
MT2 (+), G(–) 2N6346A thru 2N6349A		–	6.0	75	
MT2 (–), G(–) All Types		–	10	50	
MT2 (–), G(+) 2N6346A thru 2N6349A		–	25	75	
*MT2 (+), G(+); MT2 (–), G(–) T_C = -40°C All Types		–	–	100	
*MT2 (+), G(–); MT2 (–), G(+) T_C = -40°C 2N6346A thru 2N6349A		–	–	125	
Peak Gate Trigger Voltage Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 μs	V_{GTM}				Volts
MT2 (+), G(+) All Types		–	0.9	2.0	
MT2 (+), G(–) 2N6346A thru 2N6349A		–	0.9	2.5	
MT2 (–), G(–) All Types		–	1.1	2.0	
MT2 (–), G(+) 2N6346A thru 2N6349A		–	1.4	2.5	
*MT2 (+), G(+); MT2 (–), G(–) T_C = -40°C All Types		–	–	2.5	
*MT2 (+), G(–); MT2 (–), G(+) T_C = -40°C 2N6346A thru 2N6349A		–	–	3.0	
Main Terminal Voltage = Rated V_{DRM}, R_L = 10 k ohms, T_J = 110°C					
*MT2 (+), G(+), MT2 (–), G(–) All Types		0.2	–	–	
*MT2 (+), G(–); MT2 (–), G(+) 2N6346A thru 2N6349A		0.2	–	–	
Holding Current (Either Direction) Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current = 200 mA	I_H				mA
T_C = 25°C		–	6.0	40	
T_C = -40°C		–	–	75*	
*Turn-On Time Rated V_{DRM}, I_{TM} = 17A I_{GT} = 120 mA, Rise Time = 0.1 μs, Pulse Width = 2.0 μs	tgt	–	1.5	2.0	μs
Critical Rate of Rise of Commutation Voltage Rated V_{DRM}, I_{TM} = 17A, Commutating di/dt = 6.5 A/ms, Gate Unenergized T_C = 80°C	dv/dt	–	5.0	–	V/μs

*Indicates JEDEC Registered Data

NOTES:

1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

QUADRANT DEFINITIONS



Trigger devices are recommended for gating on Triacs. They provide:

1. Consistent predictable turn-on points.
2. Simplified circuitry.
3. Fast turn-on time for cooler, more efficient and reliable operation.

ELECTRICAL CHARACTERISTICS of RECOMMENDED BIDIRECTIONAL SWITCHES

USAGE	General		Lamp Dimmer
PART NUMBER	MBS4991	MBS4992	MBS100
V_S	6.0 – 10 V	7.5 – 9.0 V	3.0 – 5.0 V
I_S	350 μA Max	120 μA Max	100 – 400 μA
$V_{S1} - V_{S2}$	0.5 V Max	0.2 V Max	0.35 V Max
Temperature Coefficient	0.02%/°C Typ		

See AN-526 for Theory and Characteristics of Silicon Bidirectional Switches.

FIGURE 1 – AVERAGE CURRENT DERATING

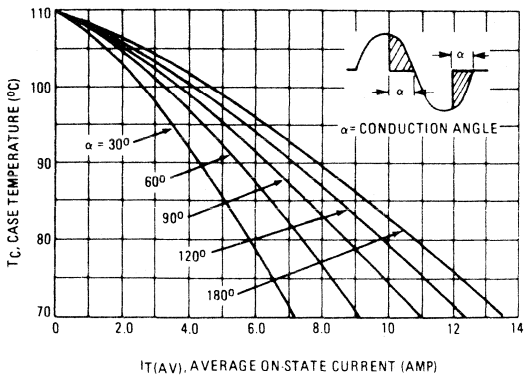


FIGURE 2 – RMS CURRENT DERATING

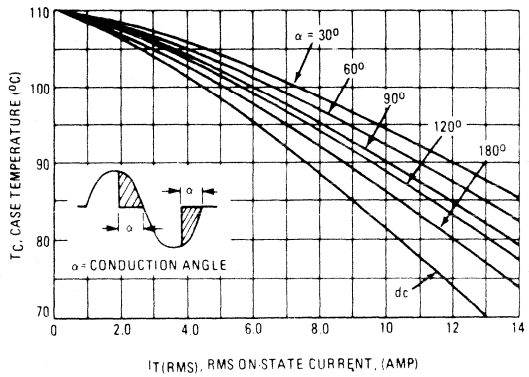


FIGURE 3 – ON-STATE POWER DISSIPATION

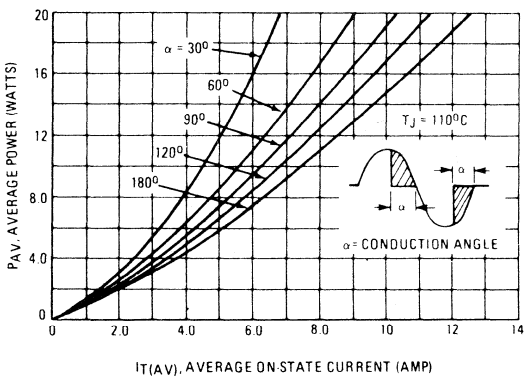


FIGURE 4 – ON-STATE POWER DISSIPATION

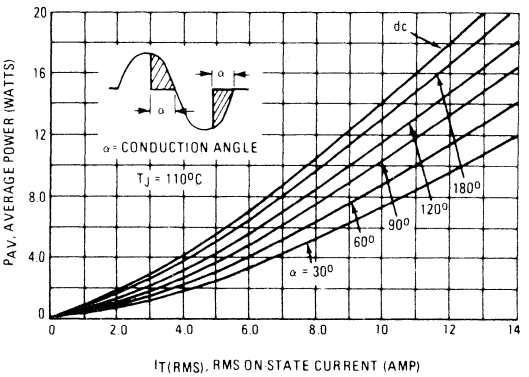


FIGURE 5 – TYPICAL GATE TRIGGER VOLTAGE

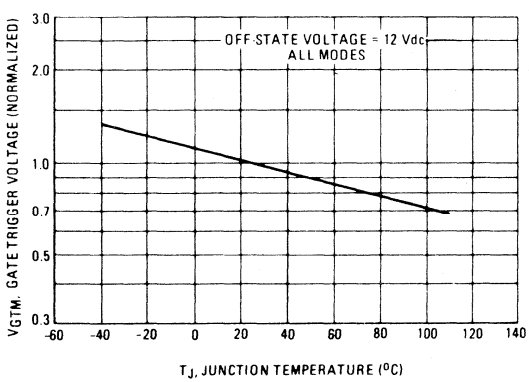


FIGURE 6 – TYPICAL GATE TRIGGER CURRENT

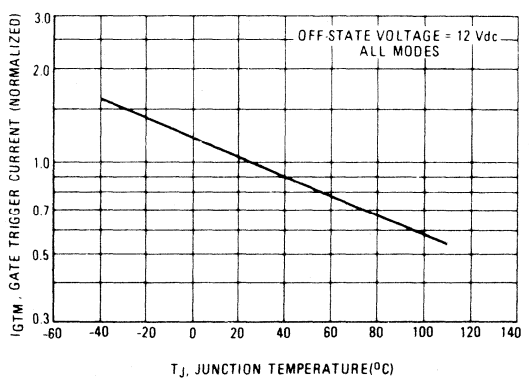


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FIGURE 7 – MAXIMUM ON-STATE CHARACTERISTICS

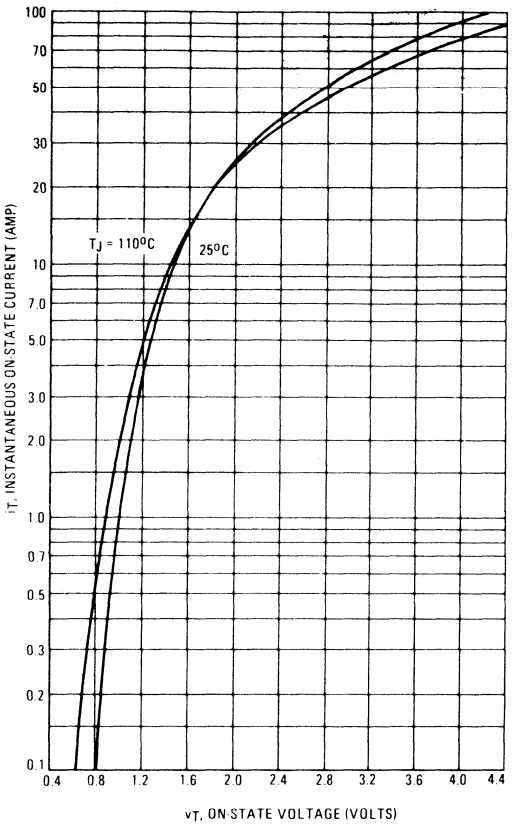


FIGURE 8 – TYPICAL HOLDING CURRENT

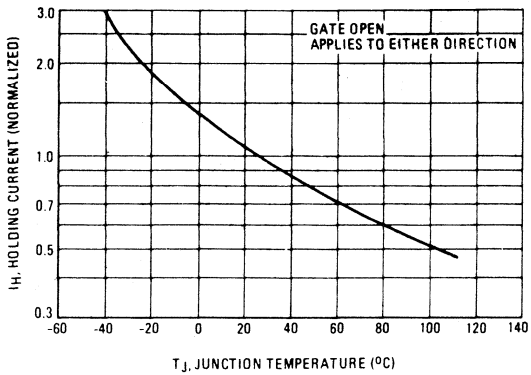


FIGURE 9 – MAXIMUM NON-REPETITIVE SURGE CURRENT

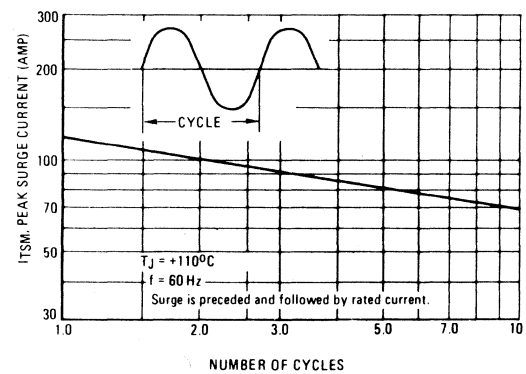
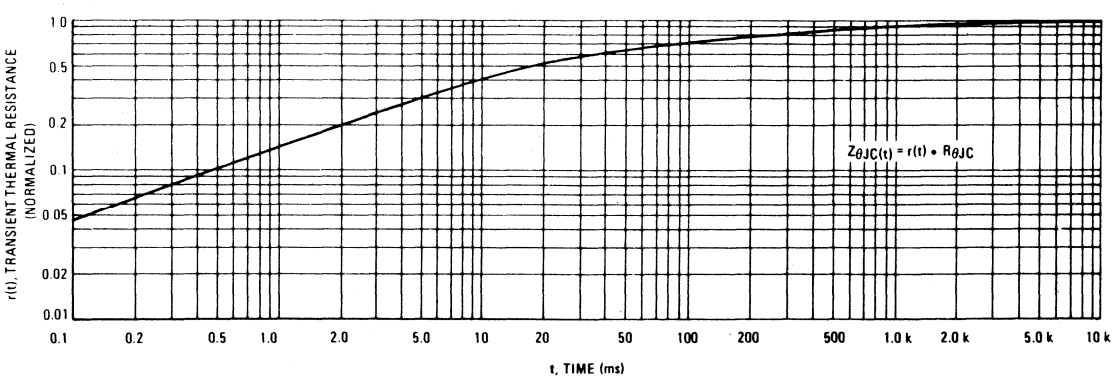
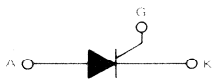


FIGURE 10 – THERMAL RESPONSE



2N6504 thru 2N6509



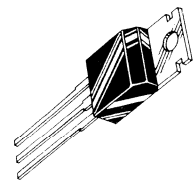
THYRISTORS

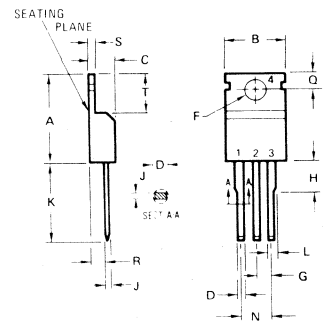
25 AMPERES RMS
50—800 VOLTS

25 AMPERES RMS SILICON CONTROLLED RECTIFIERS

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies.

- Glass Passivated Junctions with Center Gate Fire for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt▲ Constructed for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 800 Volts





STYLE 1:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H		6.35		0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.93	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

CASE 221-02
TO-220 AB

All JEDEC dimensions and notes apply.

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage (1)	V_{RRM}		Volts
2N6504		50	
2N6505		100	
2N6506		200	
2N6507		400	
2N6508		600	
2N6509		800	
Forward Current (T_C = 85°C)	$I_{T(RMS)}$	25	Amps
(All Conduction Angles)	$I_{T(AV)}$	16	
Peak Non-Repetitive Surge Current — 8.3 ms	I_{TSM}	300	Amps
(1/2 Cycle, Sine Wave) 1.5 ms		350	
Forward Peak Gate Power	P_{GM}	20	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watt
Forward Peak Gate Current	I_{GM}	2	Amps
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W

(1) V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

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* Indicates JEDEC Registered Data.

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DS6590

6

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Voltage (T_J = 125°C)		V_{DRM}				Volts
	2N6504		50	–	–	
	2N6505		100	–	–	
	2N6506		200	–	–	
	2N6507		400	–	–	
	2N6508		600	–	–	
	2N6509		800	–	–	
*Peak Forward Blocking Current (Rated V_{DRM} @ T_J = 125°C)		I_{DRM}			2	mA
*Peak Reverse Blocking Current (Rated V_{RRM} @ T_J = 125°C)		I_{RRM}			2	mA
*Forward "On" Voltage (1) (I_{TM} = 50 A)		V_{TM}			1.8	Volts
*Gate Trigger Current (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms, T_C = -40°C)		I_{GT}		25	40	mA
*Gate Trigger Voltage (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms, T_C = -40°C)		V_{GT}		1	1.5	Volts
Gate Non-Trigger Voltage (Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms, T_J = 125°C)		V_{GD}	0.2			Volts
*Holding Current (Anode Voltage = 12 Vdc, T_C = -40°C)		I_H		35	40	mA
*Turn-On Time (I_{TM} = 25 A, I_{GT} = 50 mAdc)		t_{gt}		1.5	2	μs
Turn-Off Time (V_{DRM} = rated voltage) (I_{TM} = 25 A, I_R = 25 A)		t_q		15		μs
(I_{TM} = 25 A, I_R = 25 A, T_J = 125°C)				35		
Critical Rate of Rise of Off-State Voltage (Gate Open, Rated V_{DRM}, Exponential Waveform)		dv/dt		50		V/μs

*Indicates JEDEC Registered Data.

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

FIGURE 1 – AVERAGE CURRENT DERATING

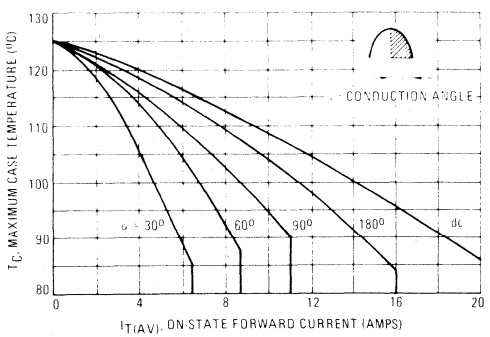


FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION

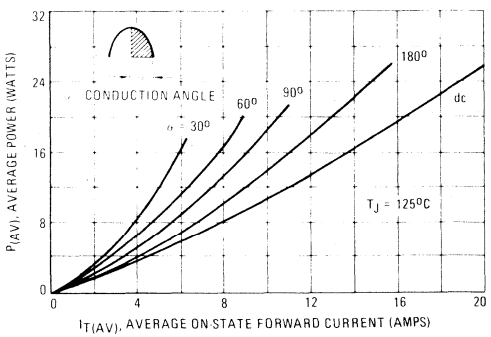


FIGURE 3 – MAXIMUM FORWARD VOLTAGE

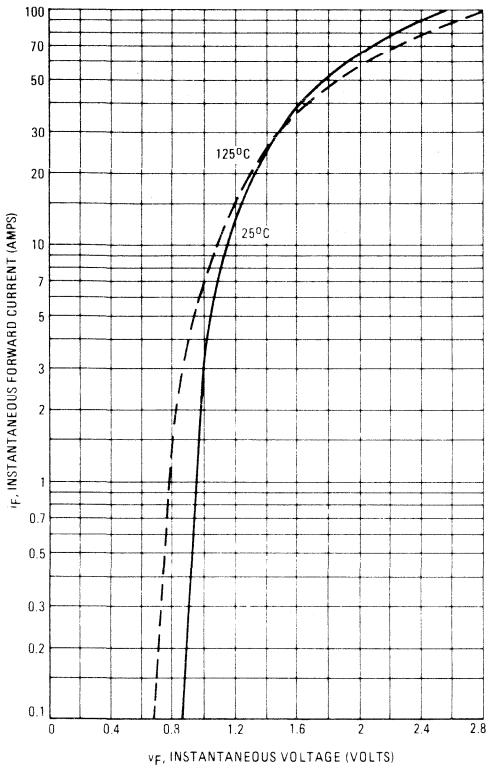


FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE CURRENT

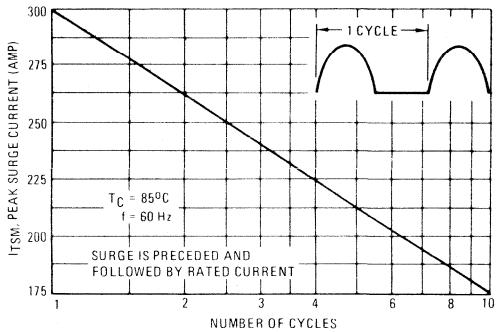


FIGURE 5 – CHARACTERISTICS AND SYMBOLS

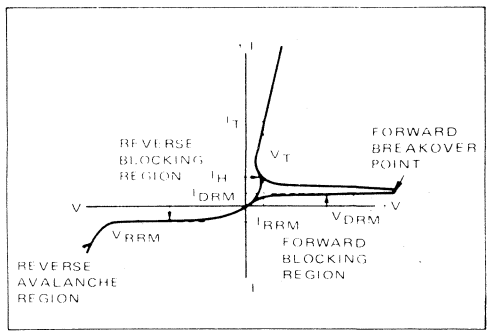
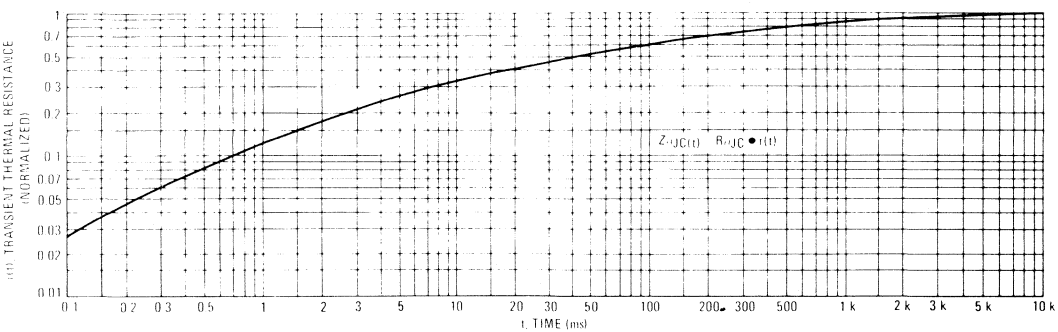


FIGURE 6 – THERMAL RESPONSE



TYPICAL TRIGGER CHARACTERISTICS

FIGURE 7 – GATE TRIGGER CURRENT

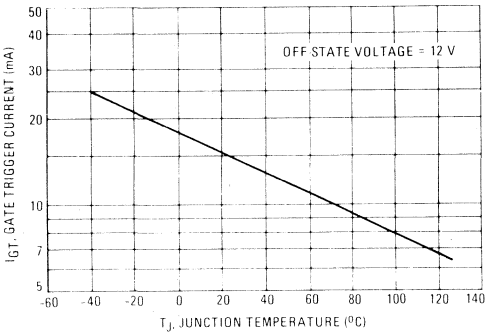


FIGURE 8 – GATE TRIGGER VOLTAGE

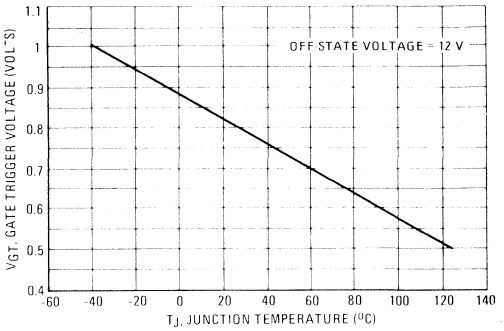
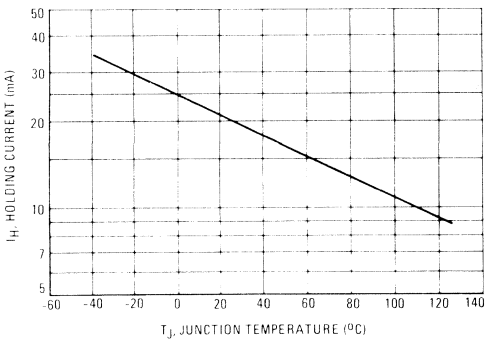


FIGURE 9 – HOLDING CURRENT



THYRISTOR APPLICATION NOTES

AN-189 Solid State Pulse Width Modulation DC Motor Control

AN-240 SCR Power Control Fundamentals

AN-295 Suppressing RFI in Thyristor Circuits

AN-413 Unijunction Trigger Circuits for Gated Thyristors

AN-443 Directional and Speed Control for Series, Universal and Shunt Motors

AN-482 Electronic Speed Control of Appliance Motors

AN-526 Theory, Characteristics and Applications of Silicon Unilateral and Bilateral Switches

AN-527 Theory, Characteristics and Applications of the Programmable Unijunction Transistor

AN-568 A Fuse-Thyristor Coordinator Primer

AN-725 A Low Cost 80 V 1.5 A Color TV Power Supply

AN-734 SCR Controller for a Series Field dc Motor

To obtain copies of these notes list the AN number(s) on your company letterhead and send your request to:

Technical Information Center
Motorola Semiconductor Products, Inc.
P.O Box 20924
Phoenix, Arizona 85036

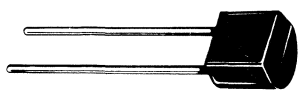
SECTION 7 — DIODES AND BRIDGES

— Rectifier diodes:
— soft, standard, fast, hot carrier, bridges, high voltage.

— Reference diodes:
— zener, voltage regulators for tuning diodes

— Variable capacitance tuning diodes.
— Hot carrier diodes.

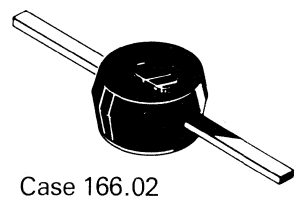
Section 7—Packages



Case 182.01
Case 182.03
Case 182.02

Case 59.04 DO 35
Case 169.02 DO 41
Case 17

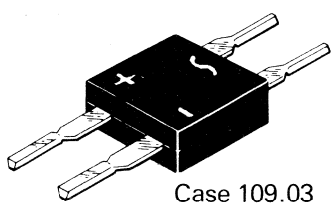
Case 226



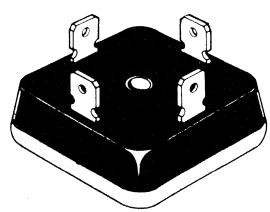
Case 166.02

Case 267
Case 267.01

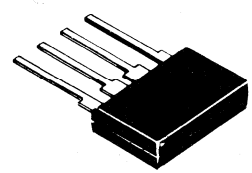
Case 194.01



Case 109.03



Case 309.01



Case 312.02

7 DIODES AND BRIDGES

Rectifier Diodes

	Device	V_{RRM} Max. V	I_{FAV} Max. A	I_{FSM} Max. A	V_F Max. V	I_R Max. µA	t_{rr} Max. µS	Package	Page
Fast, Soft and Standard Recovery	BA 157-159	400-1000	0.4	15	1.25	5	0.5	59-04	7- 4
	BY 126-127	650-1250	1	50	1.4	10	-	59-04	7- 12
	BY 196-199	100-800	1.2	70	1.3	10	0.5	59-04	7- 16
	BY 206-207	350-600	0.6	25	1.2	10	0.3	59-04	7- 22
	BY 210	400-800	1	40	1.2	10	0.3	59-04	7- 28
	BY 251-255	200-1300	3	100	1	10	-	267	7- 34
	BY 296-299	100-800	2	70	1.25	10	0.5	267	7- 39
	BY 396 Series	100-800	3	100	1.25	10	0.2	267.01	7- 43
	BY 406, 407	350-600	0.8	20	1.55	2	0.3	59.04	7- 51
	BY 500 Series	100-600	5	200	1.25	10	0.2	267.01	7- 57
	BY 601-608	50-1250	1.5	50	1.15	10	-	5904	7- 65
	BYX 10	1600	0.5	30	1.1	1	-	59.04	7- 75
	BYX 55 Series	350-600	1.2	40	1.25	10	0.35	59.04	7- 79
	MR 501, 502, 504	100-400	3	100	1.1	5	-	267.01	7-115
	MR 506, 508, 510	600-1000	3	100	1.1	5	-	267.01	7-115
	MR 751, 752, 754, 756, 758, 760	100-1000	6	400	1.25	250	-	194.01	7-121
	MR 810-814	50-400	1	30	1.2	10	0.75	59.04	7-125
	MR 816-818	500-1000	1	30	1.2	10	0.75	59.04	7-125
	MR 850-852, 854-856	50-600	3	100	1.25	10	0.2	267.01	7-131
	MR 910-914	50-400	3	100	1.25	10	0.75	267.01	7-139
	MR 916-918	600-1000	3	100	1.25	10	0.75	267.01	7-139
	1N 4001-4007	50-1000	1	30	1.1	10	-	59.04	7-157
	1N 4933-4937	50-600	1	30	1.2	5	0.2	59.04	7-158
	1N 5400-5408	50-1000	3	200	1.2	500	-	267.01	7-168
Hot Carrier	MBR 115P-140P	15-40	1	25	0.55	1000	-	59.04	7- 96
	MBR 320P-340P	20-40	3	80	0.55	2000	-	267.01	7-100
	1N 5817-5818	20.30	1	25	0.55	1000	-	59.04	7- 96
	1N 5820-5821	20-30	3	80	0.5	2000	-	267.01	7-100
Single Phase Full Wave Bridge	BYW 20 Series	50-1000	15	400	1.1	100	-	309-01	7- 72
	MDA 920A1, 920A9	25-1000	1.5	45	1.2	20	-	109-03	7-106
	MDA 200 Series	50-1000	2	60	1.1	10	-	312.02	7-104
High Voltage	MR 1-1000, 1200, 1400, 1600	1000-1600	1	30	1.1	10	25	59.04	7-110
	MR 250-1, 250-5	1000-5000	250	20	3.75	10	-	169.02	7-113

Reference Diodes

	Device	V_Z (nom) V	I_{Zr} mA	P_D Max. mW	Package	Page
Zener Diodes	BZX79 C2V4-C200	2.4-200	5	500	DO-35	7-85
	BZX83 C2V7-C33 (MZPD2.7-3.3)	2.7-33	5	500	DO-35	7-88
	MZD3.9-200	3.9-200		1300	DO-41	7-153
	1N5333-5388	3.3-200	–	5000	17	7-164
Tuning Diode Volt. Reference Diodes	MVS240	24	26	625	182-03	7-149
	MVS460	33	18	625	182-01	7-151

Variable Capitance Tuning Diodes

Device	V_R Max. V	I_F Max. mA	C_T P_F Min.	Max.	@ f MHz	V_R V	C_R Min.	@ f MHz	Q Min.	@ f MHz	V_R V	Package	Page
BB109	30	200	26	32	1	3	5	1	280	50	3	226	7-10
MV104	32	200	37	42	1	3	2.5	1	100	100	3	TO-92	7-143
MV209	30	200	26	32	1	3	5	1	200	50	3	182-02	7-147
MVAM115	18	50	440	560	1	1	15	1	150	1	1	182-03	7-147
MVAM125	28	50	440	560	1	1	15	1	150	1	1	182-03	7-147

Hot Carrier Diodes

Device	V_R Max. V	V_F @ I_F = 10 mA Max. V	C_T Max. pF	@ f MHz	V_R V	I_R Max. nA	@ V_R V	Package	Page
MBD101	4	0.6	1	1	0	250	3	182-01	7-90
MBD102	4	0.6	1	1	0	250	3	226	7-92
MBI-101	4	0.6	1	1	0	250	3	166-02	7-94

BA 157 SERIES

FAST RECOVERY POWER RECTIFIERS

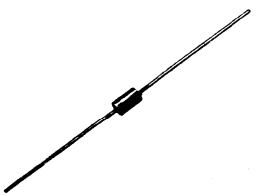
400, 600, 1000 Volts
400 mA

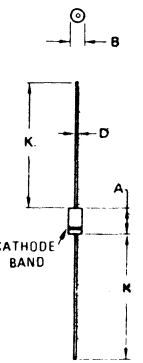
SUBMINIATURE SIZE, AXIAL LEAD MOUNTED FAST RECOVERY POWER RECTIFIERS

. . . designed for special application such as dc power supplies, inverters, converters, ultrasonic systems, choppers, low RF interference and free wheeling diodes. A complete line of fast recovery rectifiers having typical recovery time of 300 nanoseconds providing high efficiency at frequencies to 250 Hz.

DESIGNER'S DATA FOR „WORST CASE" CONDITIONS

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing device characteristic boundaries — are given to facilitate „worst case" design.





DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94	–	1.100	–

CASE 59-04

MAXIMUM RATINGS

Ratings	Symbol	BA 157	BA 158	BA 159	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RWM} V_{RRM} V_R	400	600	1000	Volts
Non Repetitive Peak Reverse Voltage	V_{RSM}	500	800	1200	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	280	420	700	Volts
Average Rectified Forward Current (Single phase, resistive load, T_A = 75° C)	I_O	400			mA
Non-Repetitive Peak Surge Current (surge applied at rated load conditions) (T_A = 75° C)	I_{FSM}	15			Amps
Operating Junction Temp. Range	T_J	−65 to +150			°C
Storage Temperature Range	T_{stg}	−65 to +175			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max.	Unit
Thermal Resistance, Junction to Ambient (Typical Primted Circuit Board Mounting)	$R_{\theta JA}$	65	°C/W

Characteristics	Symbol	Min	Typ	Max	Unit
Forward Voltage (I_F = 1,0 Amp, T_A = 25 Grad C)	V_F	—	1,0	1,25	Volts
Reverse Current (rated dc voltage) T_A = 25° C T_A = 100° C	I_R	— —	1,0 5,0	5 100	µA

REVERSE RECOVERY CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Reverse Recovery Time I_F = 10 mA to I_R = 10 mA, 1 mA	t_{rr}	—	—	500	ns

MECHANICAL CHARACTERISTICS

CASE: Void Free, Transfer Molded

FINISH: External leads are tin plated, leads are readily solderable

POLARITY: Cathode indicated by Polarity band

WEIGHT: 0.4 Grams (Approximately)

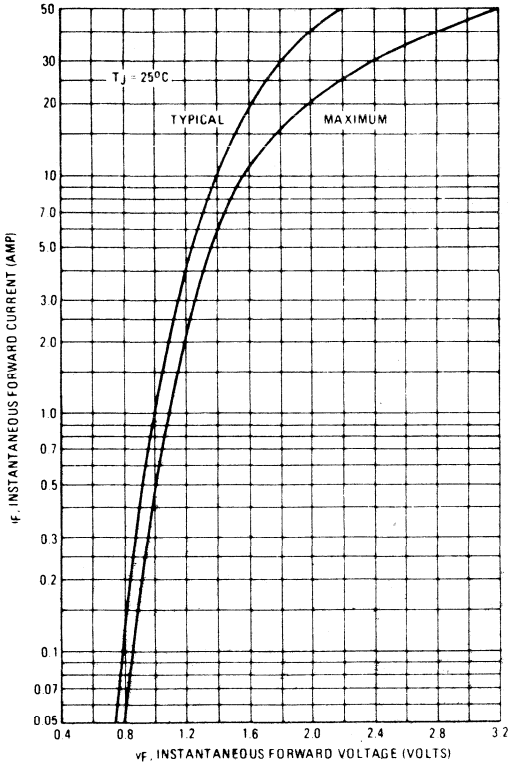


FIGURE 1 – FORWARD VOLTAGE

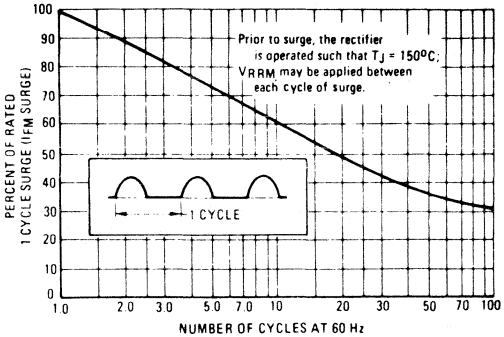


FIGURE 2 – MAXIMUM SURGE CAPABILITY

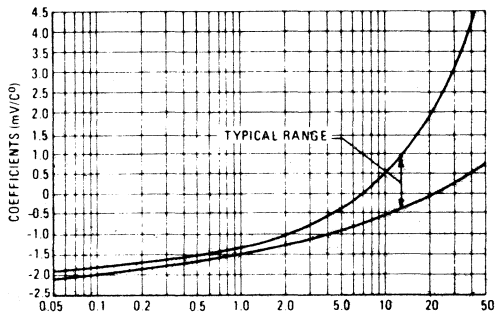


FIGURE 3 – TEMPERATURE COEFFICIENT

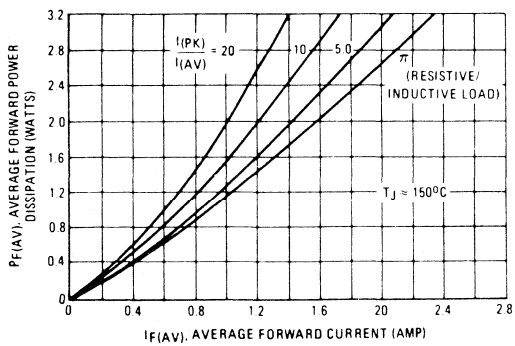


FIGURE 4 – FORWARD POWER DISSIPATION

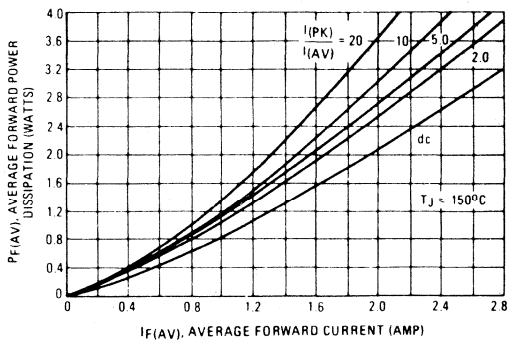


FIGURE 5 – FORWARD POWER DISSIPATION

7

MAXIMUM CURRENT RATINGS
(SEE NOTES 1 and 2)

SINE WAVE INPUT

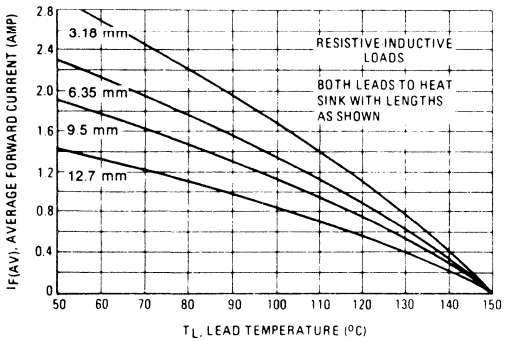


FIGURE 6 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

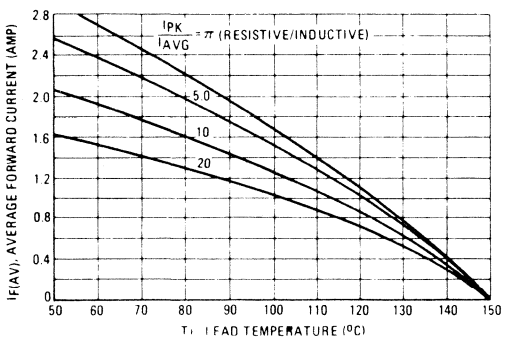


FIGURE 8 — 3.18 mm LEAD LENGTH, VARIOUS LOADS

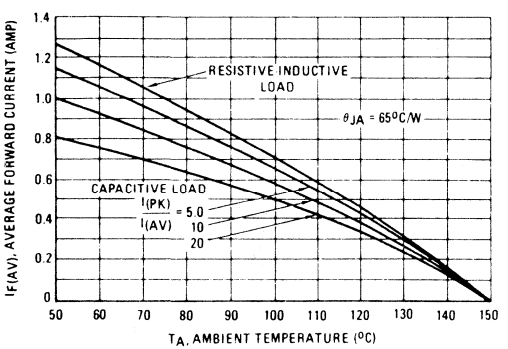


FIGURE 10 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS

SQUARE WAVE INPUT

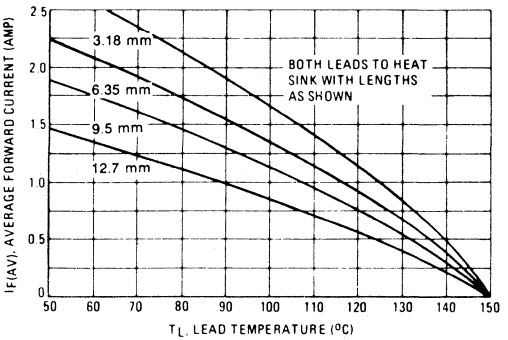


FIGURE 7 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

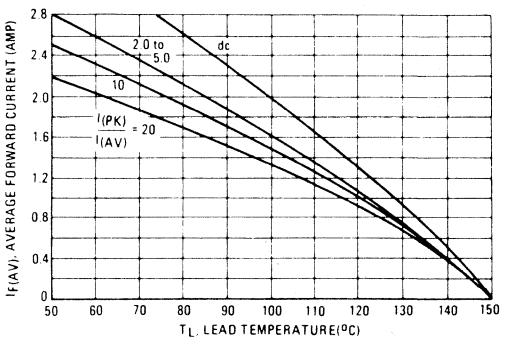


FIGURE 9 — 3.18 mm LEAD LENGTH, VARIOUS LOADS

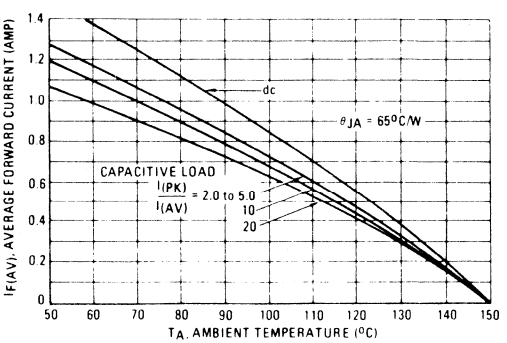


FIGURE 11 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS

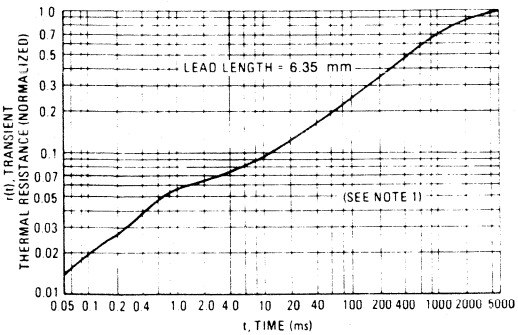


FIGURE 12 – THERMAL RESPONSE

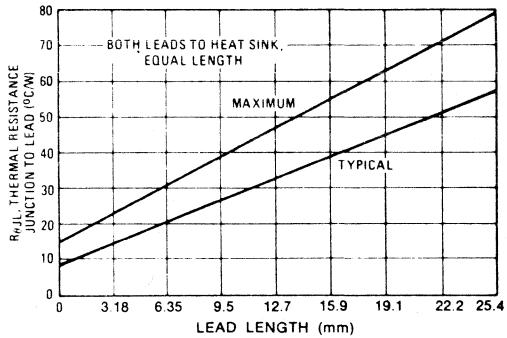
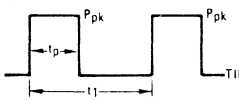


FIGURE 13 – THERMAL RESISTANCE

NOTE 1



DUTY CYCLE, D = t_p/t_1
PEAK POWER, P_{pk}, is peak of an equivalent square power pulse.

To determine maximum junction temperature of the diode in a given situation, the following procedure is recommended:

The temperature of the case should be measured using a thermocouple placed on the case as close as possible to the tie point. The thermal mass connected to the tie point is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady-state conditions are achieved. Using the measured value of T_C, the junction temperature may be determined by:

$$T_J = T_C + \triangle T_{JC}$$

where $\triangle T_{JC}$ is the increase in junction temperature above the case temperature. It may be determined by:

$$\triangle T_{JC} = P_{pk} \cdot R_{\theta JC}\left[D + (1 - D) \cdot r(t_1 + t_p) + r(t_p) - r(t_1)\right]$$

where

$r(t)$ = normalized value of transient thermal resistance at time, t, from Figure 12, i.e.:

$r(t_1 + t_p)$ = normalized value of transient thermal resistance at time $t_1 + t_p$.

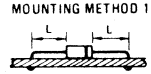
NOTE 2

Data shown for thermal resistance junction-to-ambient (θ_{JA}) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

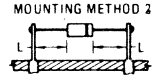
TYPICAL VALUES FOR θ_{JA} IN STILL AIR

MOUNTING METHOD	LEAD LENGTH, L(mm) 3.81	6.35	12.7	19.1	$R_{\theta JA}$
1	65	72	82	92	°C/W
2	74	81	91	101	°C/W
3	40				°C/W

MOUNTING METHOD 1

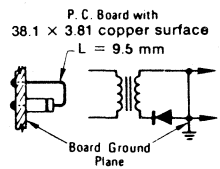


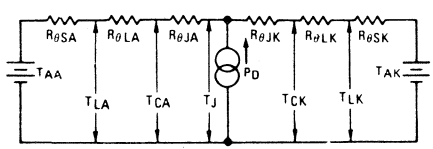
MOUNTING METHOD 2



Vector pin mounting

MOUNTING METHOD 3





Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heat sink. Terms in the model signify:

T_A = Ambient Temperature
T_L = Lead Temperature
T_C = Case Temperature
T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_D = Power Dissipation

(Subscripts A and K refer to anode and cathode sides respectively.)

Values for thermal resistance components are:

$R_{\theta L}$ = 112°C/W/IN Typically and 128°C/W/IN Maximum

$R_{\theta J}$ = 18°C/W Typically and 30°C/W Maximum

The maximum lead temperature may be calculated as follows:

$$T_L = 150^\circ - \triangle T_{JL}$$

$\triangle T_{JL}$ can be calculated as shown in NOTE 1 or it may be approximated as follows:

$\triangle T_{JL} \approx R_{\theta JL} \bullet P_F$; P_F may be formulated for sine-wave operation from Figure 3 or from Figure 4 for square-wave operation.

FIGURE 14 – THERMAL CIRCUIT MODEL

7

TYPICAL DYNAMIC CHARACTERISTICS

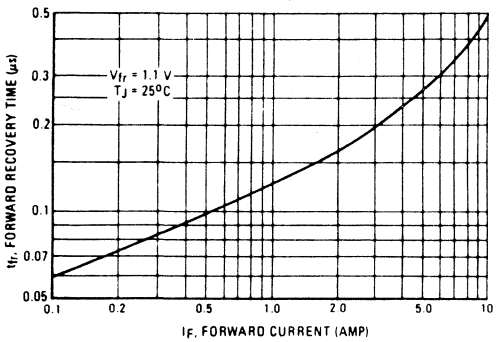


FIGURE 15 – FORWARD RECOVERY TIME

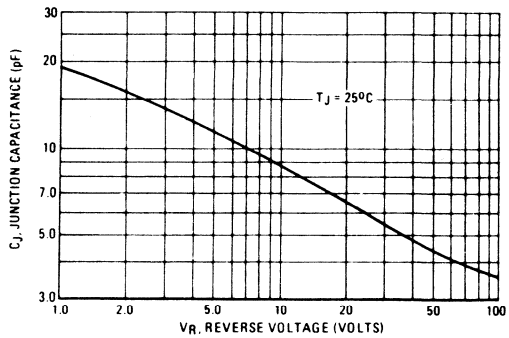


FIGURE 16 – JUNCTION CAPACITANCE

TYPICAL RECOVERED STORED CHARGE DATA
(SEE NOTE 3)

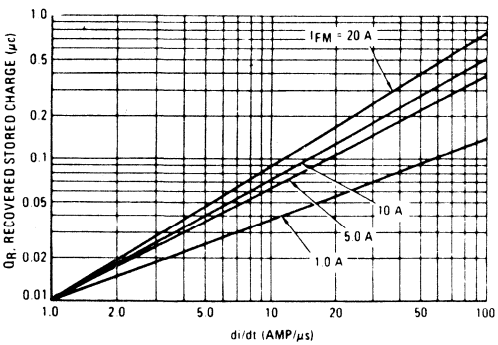


FIGURE 17 – T_J = 25°C

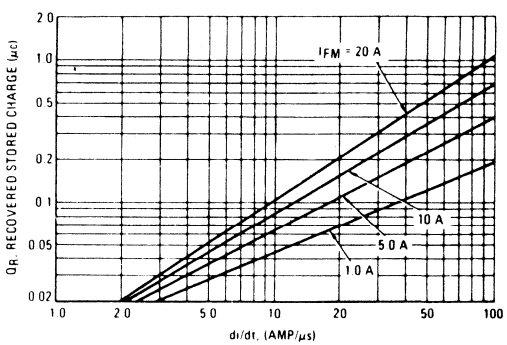


FIGURE 18 – T_J = 75°C

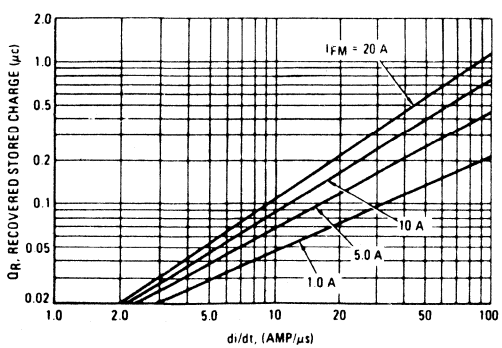


FIGURE 19 – T_J = 100°C

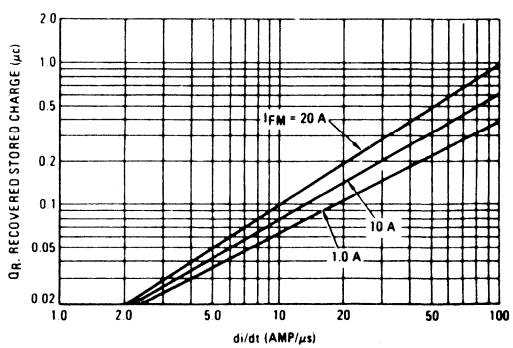


FIGURE 20 – T_J = 150°C

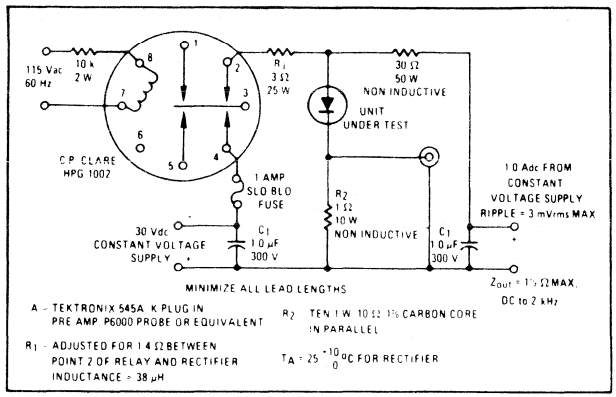


FIGURE 21 – REVERSE RECOVERY CIRCUIT

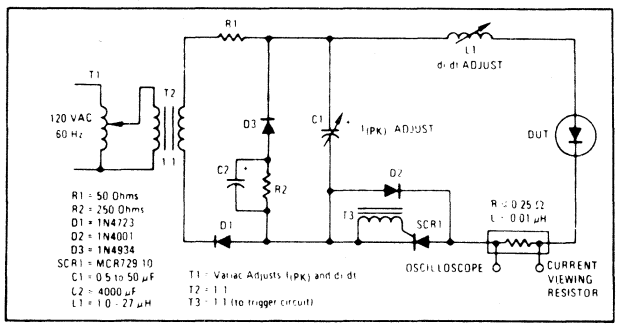


FIGURE 22 – JEDEC REVERSE RECOVERY CIRCUIT

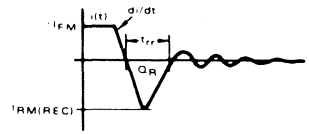
NOTE 3

Reverse recovery time is the period which elapses from the time that the current, thru a previously forward biased rectifier diode, passes thru zero going negatively until the reverse current recovers to a point which is less than 10% peak reverse current.

Reverse recovery time is a direct function of the forward current prior to the application of reverse voltage.

For any given rectifier, recovery time is very circuit dependent. Typical and maximum recovery time of all Motorola fast recovery power rectifiers are rated under a fixed set of conditions using I_F = 1.0 A, V_R = 30 V. In order to cover all circuit conditions, curves are given for typical recovered stored charge versus commutation di/dt for various levels of forward current and for junction temperatures of 25°C, 75°C, 100°C, and 150°C.

To use these curves, it is necessary to know the forward current level just before commutation, the circuit commutation di/dt, and the operating junction temperature. The reverse recovery test current waveform for all Motorola fast recovery rectifiers is shown.



From stored charge curves versus di/dt, recovery time (t_{rr}) and peak reverse recovery current ($I_{RM(REC)}$) can be closely approximated using the following formulas:

$$t_{rr} = 1.41 \times \left[\frac{Q_R}{di/dt}\right]^{1/2}$$

$$I_{RM(REC)} = 1.41 \times \left[Q_R \times di/dt\right]^{1/2}$$

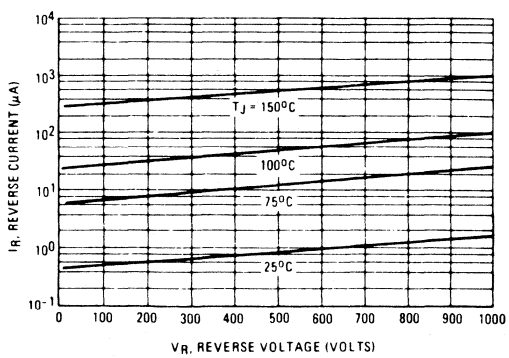


FIGURE 23 – TYPICAL REVERSE LEAKAGE

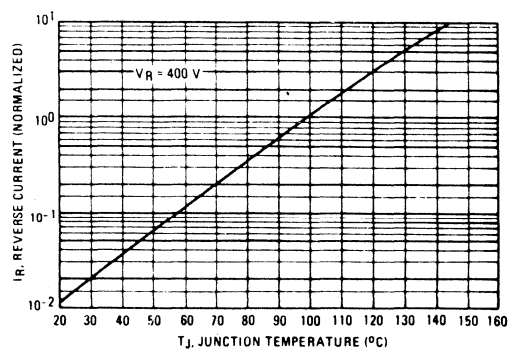


FIGURE 24 – TYPICAL REVERSE LEAKAGE

7

VVC

SILICON EPICAP▲ DIODE

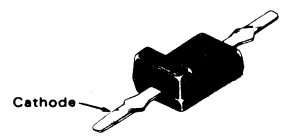
. . . designed in the new low-inductance Mini-L package for high volume requirements in VHF TV tuning, AFC, general frequency control and tuning applications; providing solid-state reliability in replacement of mechanical tuning methods.

- High Q With Guaranteed Minimum Values at VHF Frequencies
- Controlled and Uniform Tuning Ratio
- Low Inductance Mini-L Package
- Guaranteed Matching* Tolerance From Diode to Diode and Group to Group

*Upon request, diodes are available in matched sets of any number or in matched groups.

VOLTAGE VARIABLE CAPACITANCE DIODE

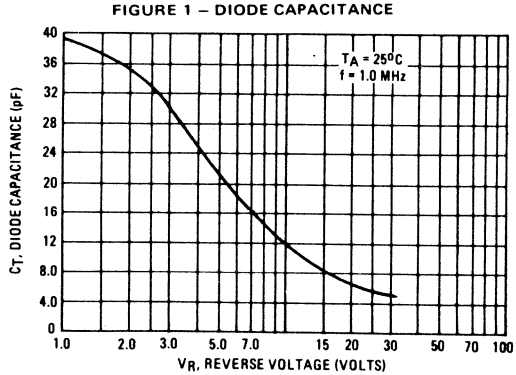
26–32 pF

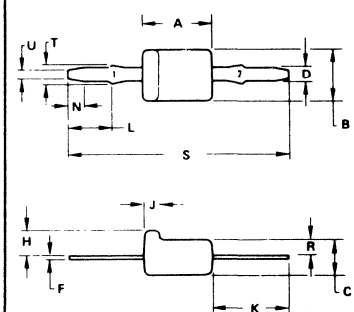


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	30	Volts
Forward Current	I_F	200	mA
Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	400 4.0	mW mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 1 – DIODE CAPACITANCE





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	3.86	4.11	0.152	0.162
B	2.92	3.18	0.115	0.125
C	1.91	2.16	0.075	0.085
D	0.64	0.89	0.025	0.035
F	0.08	0.18	0.003	0.007
H	1.30	1.55	0.051	0.061
J	0.64	0.89	0.025	0.035
K	4.06	4.32	0.160	0.170
L	2.36	2.62	0.093	0.103
N	1.12	1.37	0.044	0.054
R	0.79	1.04	0.031	0.041
S	11.99	12.75	0.472	0.502
T	1.14	1.40	0.045	0.055
U	0.43	0.69	0.017	0.027

PIN 1. CATHODE
2. ANODE

CASE 226

▲Trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic–All Types	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	BV_R	30	–	–	Vdc
Reverse Voltage Leakage Current (V_R = 28 Vdc, T_A = 25°C)	I_R	–	–	50	nA
Series Inductance (f = 250 MHz, Measured at Lead Stop≈1/8")	L_S	–	3.0	–	nH
Case Capacitance (f = 1.0 MHz)	C_C	–	0.1	–	pF
Diode Capacitance Temperature Coefficient (V_R = 3.0 Vdc, f = 1.0 MHz)	TC_C	–	300	400	ppm/°C

	C_T, Diode Capacitance V_R = 3.0 Vdc, f = 1.0 MHz pF			Q, Figure of Merit V_R = 3.0 Vdc f = 50 MHz	C_R, Capacitance Ratio C_3/C_{25} f = 1.0 MHz		Package Stripe
Device	Min	Nom	Max	Min	Min	Max	Color
BB109	26	29	32	280	5.0	6.5	RED

FIGURE 2 – FIGURE OF MERIT

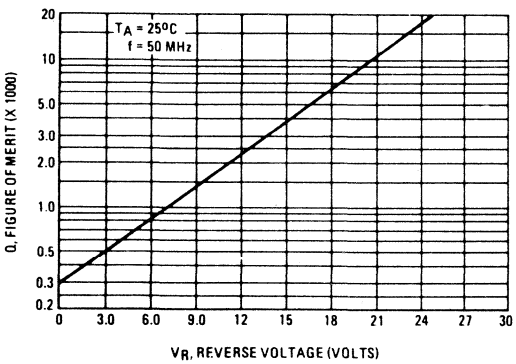


FIGURE 3 – LEAKAGE CURRENT

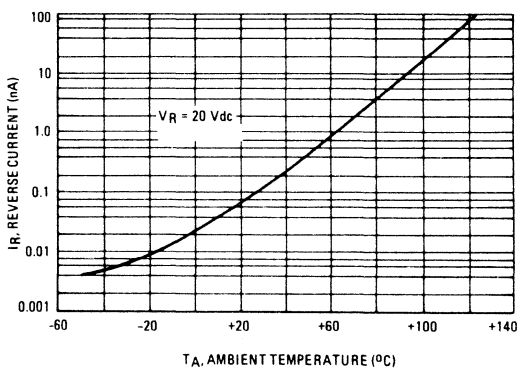
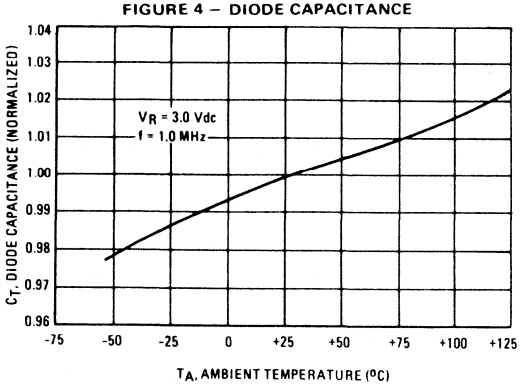


FIGURE 4 – DIODE CAPACITANCE



NOTES ON TESTING AND SPECIFICATIONS

1. L_S is measured on a package having a short instead of a die, using an impedance bridge (Boonton Radio Model 250A RX Meter).
2. C_C is measured on a package without a die, using a capacitance bridge (Boonton Electronics Model 75A or equivalent).
3. Q is calculated by taking the G and C readings of an admittance bridge, such as Boonton Electronics Model 33AS8, at the specified frequency and substituting in the following equation:

$$Q = \frac{2\pi fC}{G}$$

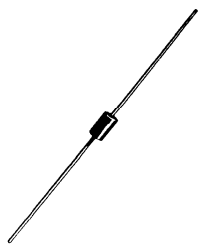
4. C_R is the ratio of C_T measured at 3.0 Vdc divided by C_T measured at 25 Vdc.

7

BY 126, 127, BY 133 SERIES

LEAD-MOUNTED SILICON RECTIFIERS

650—1300 VOLTS
DIFFUSED JUNCTION



"SURMETIC" RECTIFIERS

. . . subminiature size, axial lead-mounted rectifiers for general-purpose, low-power applications.

Designers Data for "Worst Case" Conditions

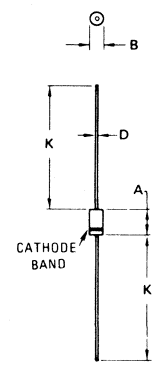
The Designers Data Sheets permit the design of most circuits entirely from the information presented. Limits curves—representing boundaries on device characteristics—are given to facilitate "worst-case" design.

MAXIMUM RATINGS

Rating	Symbol	BY 126	BY 127	BY 133	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	650	1250	1300	Volts
Nonrepetitive Peak Reverse Voltage (Halfwave, Single Phase, 60 Hz)	V_{RSM}	650	1250	1300	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	460	880	920	Volts
Average Rectified Forward Current (Single Phase, Resistive Load, 60 Hz, T_L = 70°C, 1/2" From Body)	I_O	1,0			Amp
Nonrepetitive Peak Surge Current (Surge Applied at Rated Load Conditions, See Figure 2)	I_{FSM}	50 (for 1 cycle)			Amp
Storage Temperature Range	T_{stg}	-65 to +175			°C
Operating Temperature Range	T_L	-65 to +170			°C
DC Blocking Voltage Temperature	T_L	150			°C

ELECTRICAL CHARACTERISTICS

Characteristic and Conditions	Symbol	Typ	Max	Unit
Maximum Instantaneous Forward Voltage Drop (i_F = 4.7 Amp Peak, T_L = 170°C, 1/2 Inch Leads)	v_F	—	1.4	Volts
Maximum Reverse Current (Rated dc Voltage) (T_L = 150°C)	I_{R1}	250	300	μA
Maximum Reverse Current T_L = 25° C	I_{R2}	—	10	μA



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94	–	1.100	–

CASE 59-04
Dimensions Within JEDEC DO-15 Outline.

MECHANICAL CHARACTERISTICS

CASE: Void free, transfer molded

MAXIMUM LEAD TEMPERATURE FOR SOLDERING PURPOSES: 240°C, 1/8" from case for 10 seconds at 5 lbs. tension

FINISH: All external surfaces are corrosion-resistant, leads are readily solderable

POLARITY: Cathode indicated by color band

WEIGHT: 0.40 grams (approximately)

FIGURE 1 – FORWARD VOLTAGE

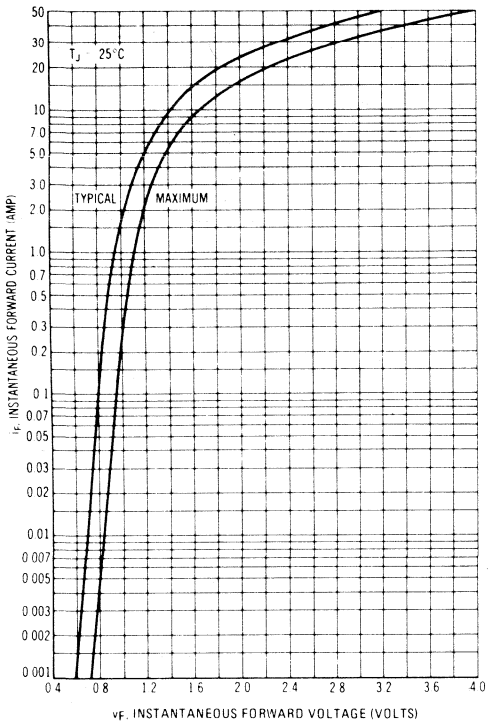


FIGURE 2 – MAXIMUM NONREPETITIVE SURGE CURRENT

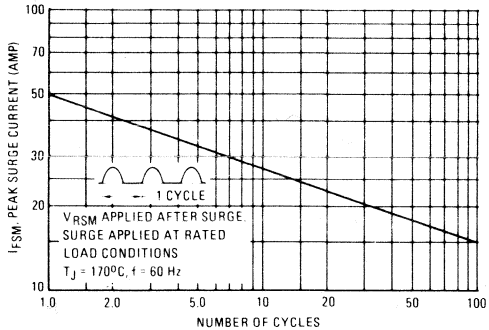


FIGURE 3 – FORWARD VOLTAGE TEMPERATURE COEFFICIENT

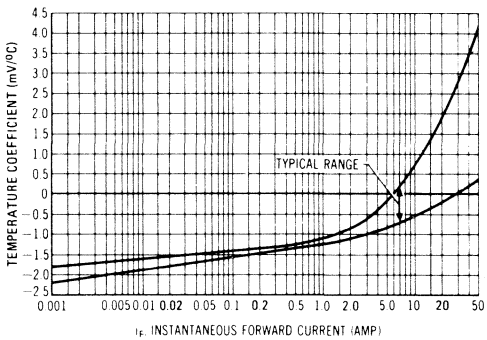
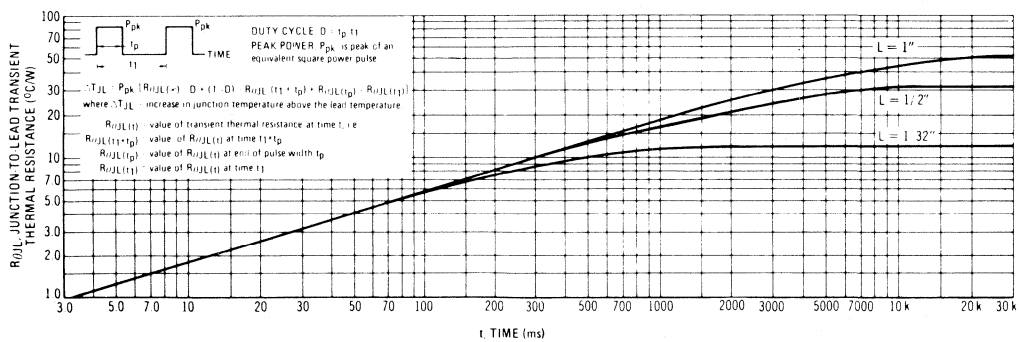


FIGURE 4 – TYPICAL TRANSIENT THERMAL RESISTANCE



The temperature of the lead should be measured using a thermocouple placed on the lead as close as possible to the tie point. The thermal mass connected to the tie point is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady-state conditions are achieved. Using the measured value of T_L, the junction temperature may be determined by:

$$T_J = T_L + \Delta T_{JL}.$$

FIGURE 5 – FORWARD POWER DISSIPATION

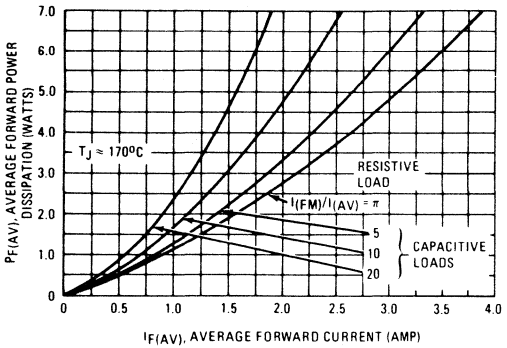


FIGURE 6 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

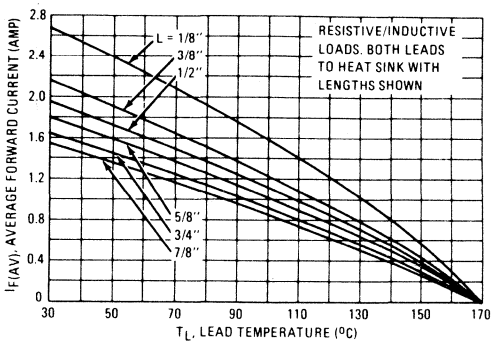


FIGURE 7 – 1/2" LEAD LENGTH, VARIOUS LOADS

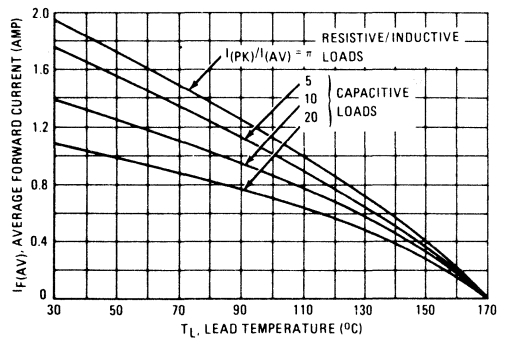


FIGURE 8 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS

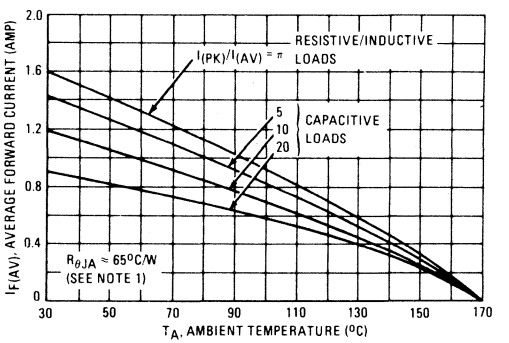
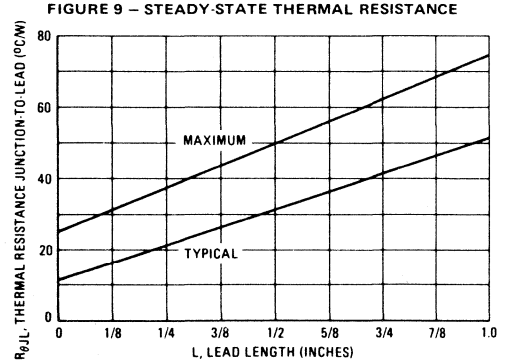


FIGURE 9 – STEADY-STATE THERMAL RESISTANCE



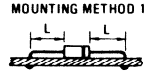
NOTE 1

Data shown for thermal resistance junction-to-ambient (θ_{JA}) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

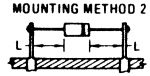
TYPICAL VALUES FOR θ_{JA} IN STILL AIR

MOUNTING METHOD	LEAD LENGTH, L (IN)				$R_{\theta JA}$
	1/8	1/4	1/2	3/4	
1	65	72	82	92	$^oC/W$
2	74	81	91	101	$^oC/W$
3	40				$^oC/W$

MOUNTING METHOD 1



MOUNTING METHOD 2



Vector pin mounting

MOUNTING METHOD 3

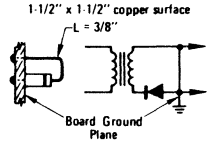


FIGURE 10 – FORWARD RECOVERY TIME

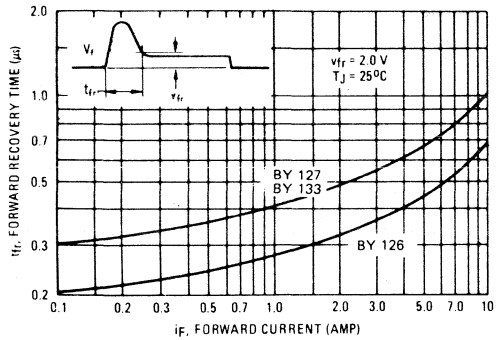


FIGURE 11 – REVERSE RECOVERY TIME

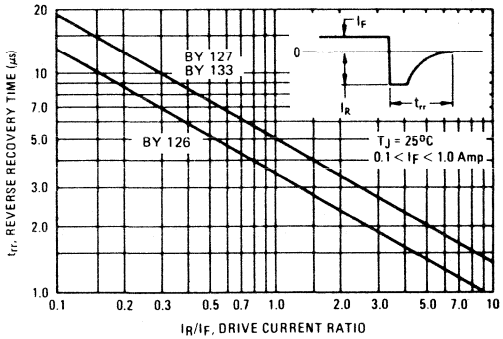


FIGURE 12 – JUNCTION CAPACITANCE

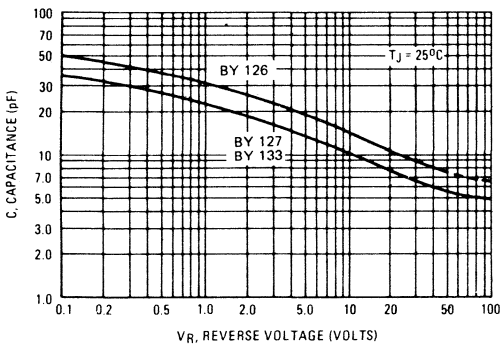


FIGURE 13 – RECTIFICATION WAVEFORM EFFICIENCY FOR SINE WAVE

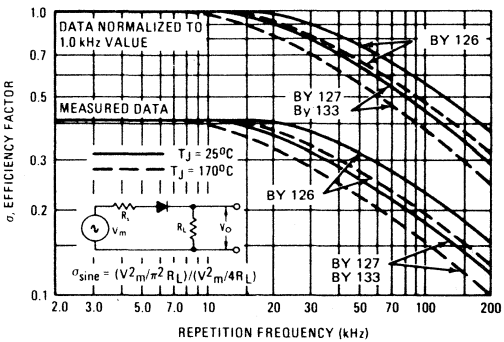
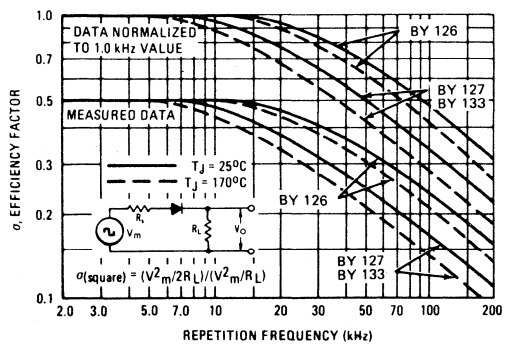


FIGURE 14 – RECTIFICATION WAVEFORM EFFICIENCY FOR SQUARE WAVE



RECTIFIER EFFICIENCY NOTE

The rectification efficiency factor σ shown in Figures 13 and 14 was calculated using the formula:

$$\sigma = \frac{P_{dc}}{P_{rms}} = \frac{\frac{V^2_{O(dc)}}{R_L}}{\frac{V^2_{O(rms)}}{R_L}} \bullet 100\% = \frac{V^2_{O(dc)}}{V^2_{O(ac)} + V^2_{O(dc)}} \bullet 100\% \quad (1)$$

For a sine wave input $V_m \sin(\omega t)$ to the diode, assumed lossless, the maximum theoretical efficiency factor becomes 40%; for a square wave input of amplitude V_m, the efficiency factor becomes 50%. (A full wave circuit has twice these efficiencies).

As the frequency of the input signal is increased, the reverse recovery time of the diode (Figure 11) becomes significant, resulting in an increasing ac voltage component across R_L which is opposite in polarity to the forward current thereby reducing the value of the efficiency factor σ, as shown in Figures 13 and 14.

It should be emphasized that Figures 13 and 14 show waveform efficiency only; they do not account for diode losses. Data was obtained by measuring the ac component of V_O with a true rms voltmeter and the dc component with a dc voltmeter. The data was used in Equation 1 to obtain points for the Figures.

7

BY 196 SERIES

SOFT RECOVERY POWER RECTIFIERS

100, 200, 400, 800 VOLTS
1.2 AMPERE

SUBMINIATURE SIZE, AXIAL LEAD MOUNTED SOFT RECOVERY POWER RECTIFIERS

. . . designed for special applications such as dc power supplies, inverters, converters, ultrasonic systems, choppers, low RF interference and free wheeling diodes. A complete line of fast recovery rectifiers having typical recovery time of 500 nanoseconds providing high efficiency at frequencies to 250 Hz.

DESIGNER'S DATA FOR „WORST CASE" CONDITIONS

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit curves – representing device characteristic boundaries – are given to facilitate „worst case" design.

MAXIMUM RATINGS

Ratings	Symbol	BY196	BY197	BY198	BY199	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RWM} V_{RRM} V_R	100	200	400	800	Volts
Non Repetitive Peak Reverse Voltage	V_{RSM}	200	300	500	1000	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	70	140	280	560	Volts
Average Rectified Forward Current (Single phase, resistive load, T_A = 75° C)	I_O	1.2 (1)				Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions) (T_A = 25° C)	I_{FSM}	70				Amps
Operating Junction Temp. Range	T_J	-65 to +150				°C
Storage Temperature Range	T_{stg}	-65 to +175				°C

1. Valid with leads at ambient Temperature at a Distance of 10 mm from case

THERMAL CHARACTERISTICS

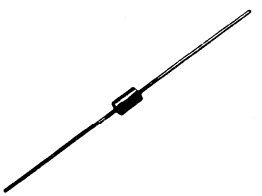
Characteristics	Symbol	Max.	Unit
Thermal Resistance, Junction to Ambient (Typical Printed Circuit Board Mounting)	$R_{\theta JA}$	65	°C/W

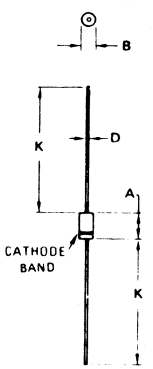
ELECTICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Forward Voltage (I_F = 3,0 Amp. T_A = 25 °C)	V_F	—	1.1	1.3	Volts
Reverse Current (rated dc voltage) T_A = 25° C T_A = 100° C	I_R	— —	1.0 50	10 100	μA

REVERSE RECOVERY CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Reverse Recovery Time I_F = 10 mA through I_R = 10 mA to I_R = 1 mA	t_{rr}	—	—	500	ns
I_F = 1 Amp. to V_R = 30 V_{DC} (figure 21)	t_{rr}	—	350	750	ns





	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94		1.100	

CASE 59-04

MECHANICAL CHARACTERISTICS

CASE: Void Free, Transfer Molded

FINISH: External leads are tin plated, leads are readily solderable

POLARITY: Cathode indicated by Polarity band

WEIGHT: 0.4 Grams (Approximately)

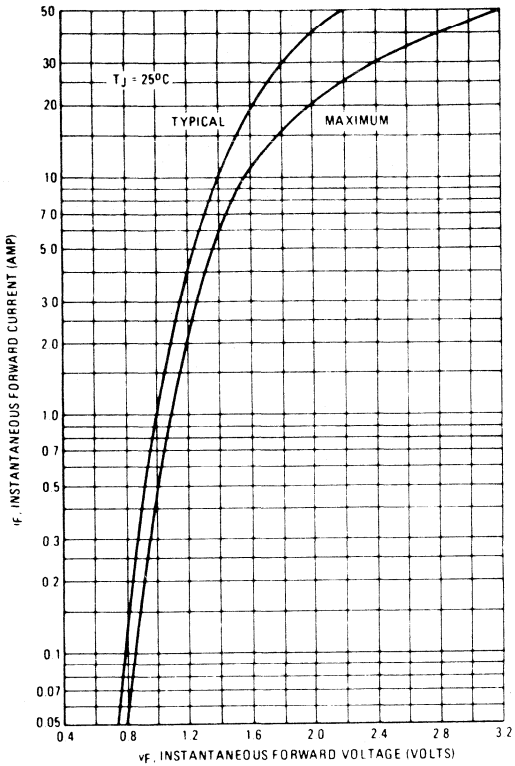


FIGURE 1 – FORWARD VOLTAGE

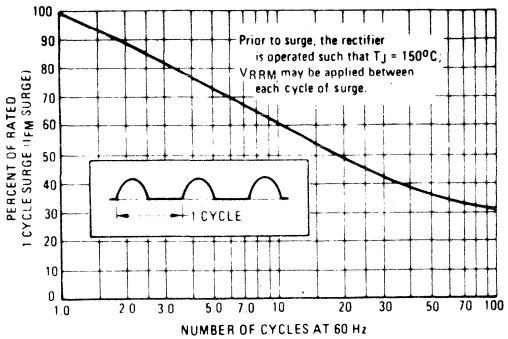


FIGURE 2 – MAXIMUM SURGE CAPABILITY

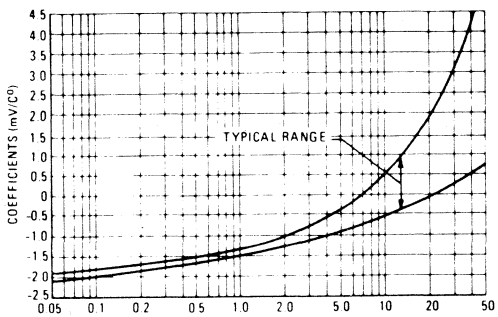


FIGURE 3 – TEMPERATURE COEFFICIENT

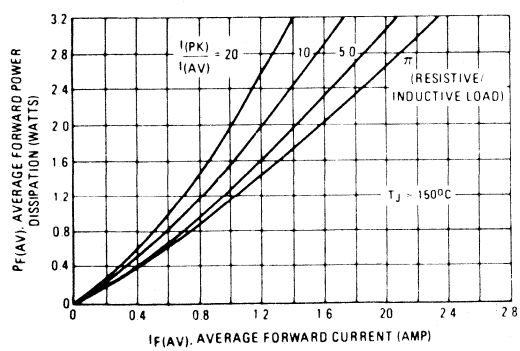


FIGURE 4 – FORWARD POWER DISSIPATION

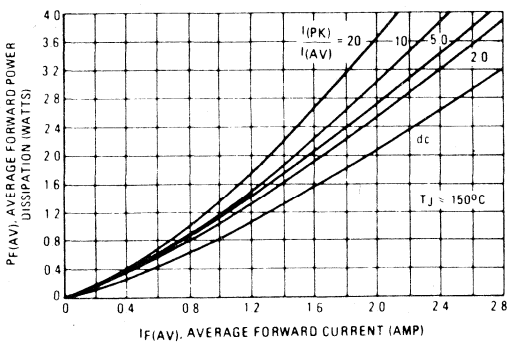


FIGURE 5 – FORWARD POWER DISSIPATION

7

MAXIMUM CURRENT RATINGS
(SEE NOTES 1 and 2)

SINE WAVE INPUT

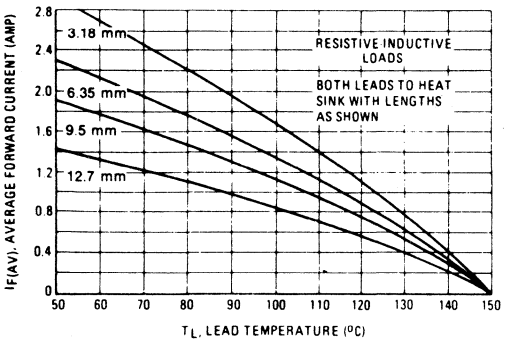


FIGURE 6 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

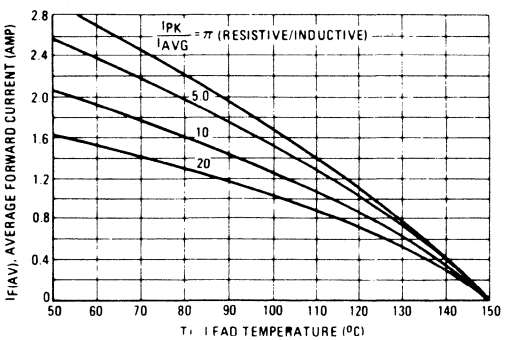


FIGURE 8 — 3.18 mm LEAD LENGTH, VARIOUS LOADS

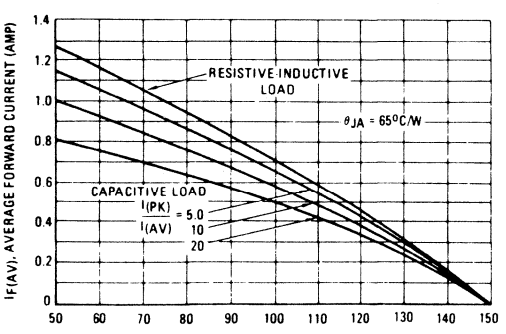


FIGURE 10 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS

SQUARE WAVE INPUT

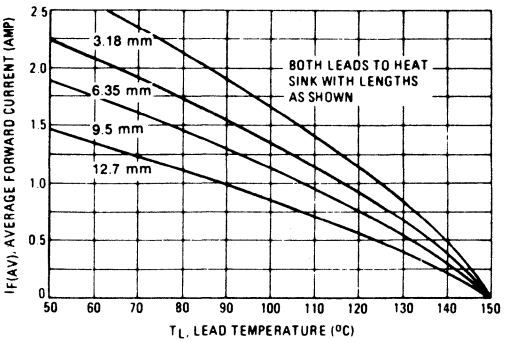


FIGURE 7 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

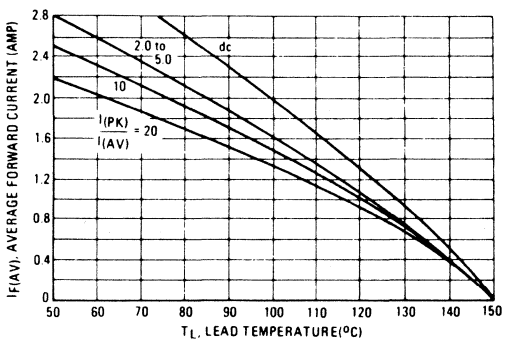


FIGURE 9 — 3.18 mm LEAD LENGTH, VARIOUS LOADS

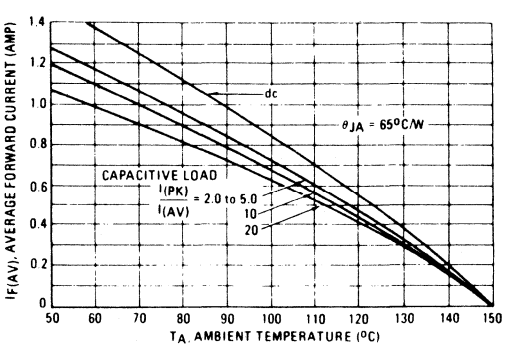


FIGURE 11 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS

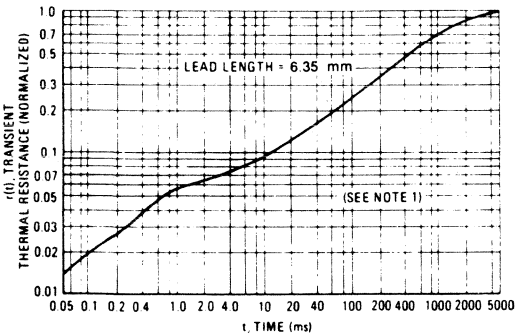


FIGURE 12 – THERMAL RESPONSE

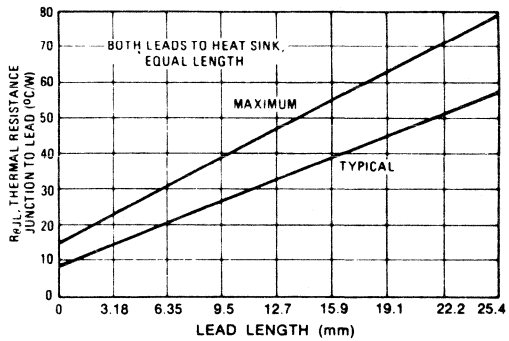
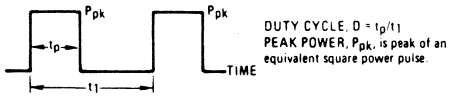


FIGURE 13 – THERMAL RESISTANCE

NOTE 1



DUTY CYCLE, D = t_p/t_1
PEAK POWER, P_{pk}, is peak of an equivalent square power pulse.

To determine maximum junction temperature of the diode in a given situation, the following procedure is recommended:

The temperature of the case should be measured using a thermocouple placed on the case as close as possible to the tie point. The thermal mass connected to the tie point is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady-state conditions are achieved. Using the measured value of T_C, the junction temperature may be determined by:

$$T_J = T_C + \Delta T_{JC}$$

where ΔT_{JC} is the increase in junction temperature above the case temperature. It may be determined by:

$$\Delta T_{JC} = P_{pk} \cdot R_{\theta JC}\left[D + (1 - D) \cdot r(t_1 + t_p) + r(t_p) - r(t_1)\right]$$

where

r(t) = normalized value of transient thermal resistance at time, t, from Figure 12, i.e.:

$r(t_1 + t_p)$ = normalized value of transient thermal resistance at time $t_1 + t_p$.

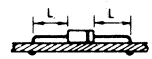
NOTE 2

Data shown for thermal resistance junction-to-ambient (θ_{JA}) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

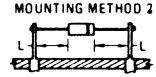
TYPICAL VALUES FOR θ_{JA} IN STILL AIR

MOUNTING METHOD	LEAD LENGTH, L(mm) 3.81	6.35	12.7	19.1	$R_{\theta JA}$
1	65	72	82	92	°C/W
2	74	81	91	101	°C/W
3	40				°C/W

MOUNTING METHOD 1

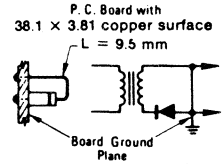


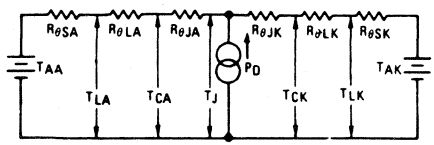
MOUNTING METHOD 2



Vector pin mounting

MOUNTING METHOD 3





Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heat sink. Terms in the model signify:

T_A = Ambient Temperature
T_L = Lead Temperature
T_C = Case Temperature
T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_D = Power Dissipation

(Subscripts A and K refer to anode and cathode sides respectively.)

Values for thermal resistance components are:

$R_{\theta L}$ = 112°C/W/IN. Typically and 128°C/W/IN Maximum

$R_{\theta J}$ = 18°C/W Typically and 30°C/W Maximum

The maximum lead temperature may be calculated as follows:

$T_L = 150° - \Delta T_{JL}$

ΔT_{JL} can be calculated as shown in NOTE 1 or it may be approximated as follows:

$\Delta T_{JL} \approx R_{\theta JL} \cdot P_F$. P_F may be formulated for sine-wave operation from Figure 3 or from Figure 4 for square-wave operation.

FIGURE 14 – THERMAL CIRCUIT MODEL

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TYPICAL DYNAMIC CHARACTERISTICS

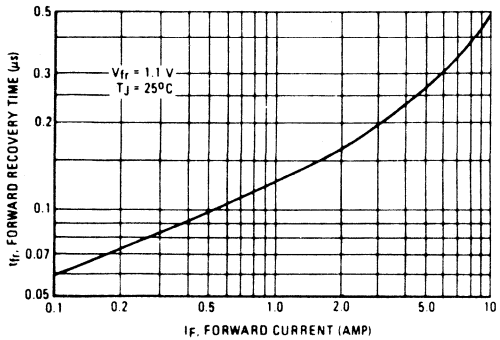


FIGURE 15 – FORWARD RECOVERY TIME

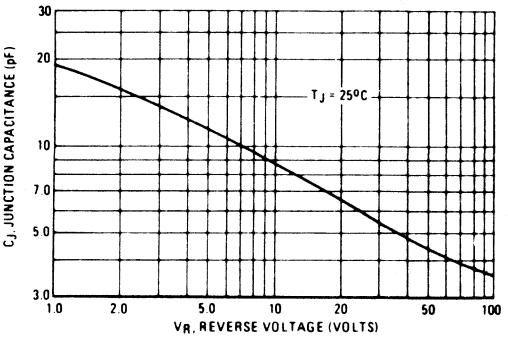


FIGURE 16 – JUNCTION CAPACITANCE

TYPICAL RECOVERED STORED CHARGE DATA
(SEE NOTE 3)

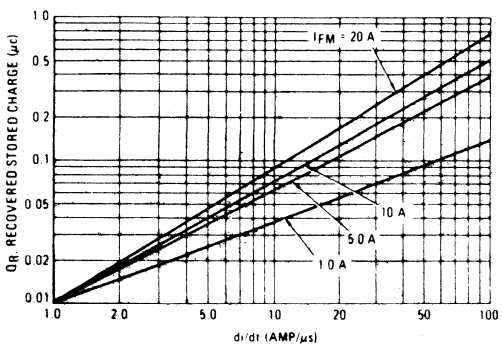


FIGURE 17 – T_J = 25°C

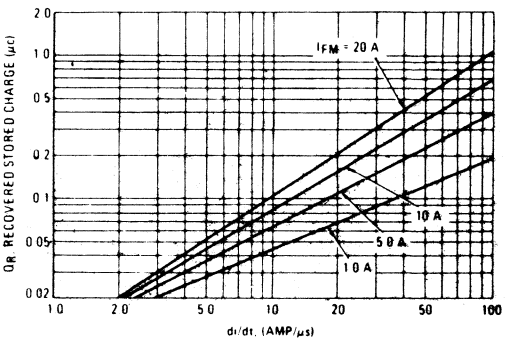


FIGURE 18 – T_J = 75°C

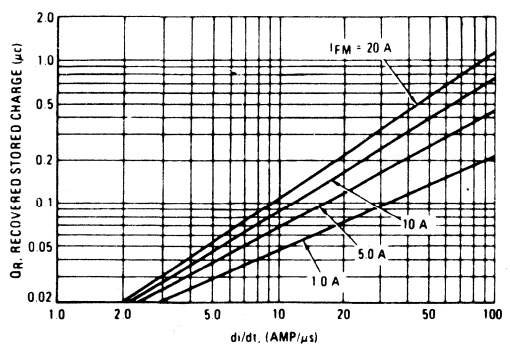


FIGURE 19 – T_J = 100°C

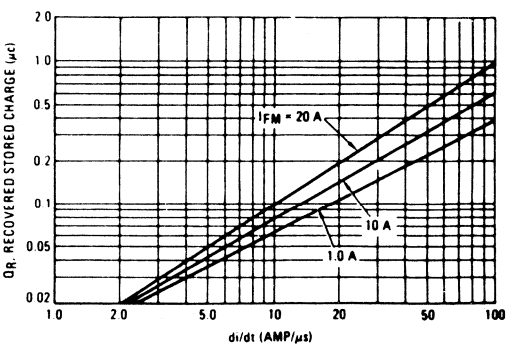


FIGURE 20 – T_J = 150°C

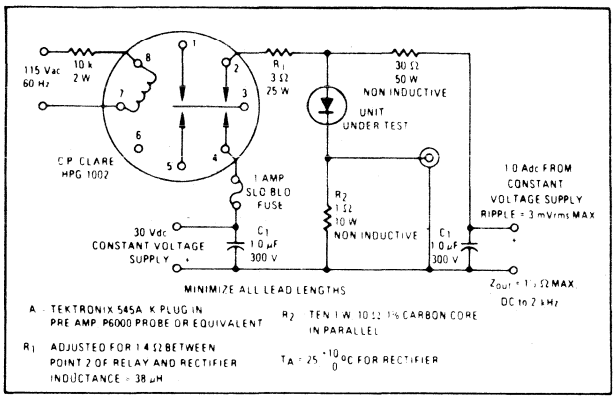


FIGURE 21 – REVERSE RECOVERY CIRCUIT

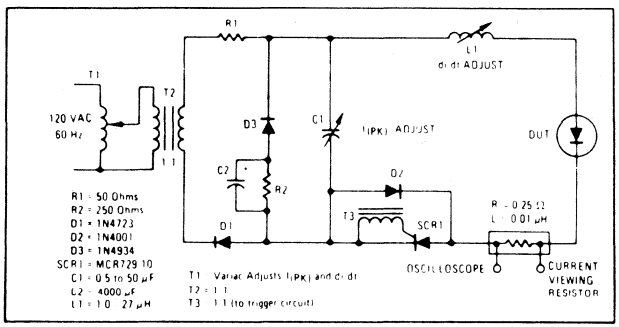


FIGURE 22 – JEDEC REVERSE RECOVERY CIRCUIT

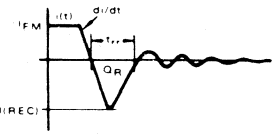
NOTE 3

Reverse recovery time is the period which elapses from the time that the current, thru a previously forward biased rectifier diode, passes thru zero going negatively until the reverse current recovers to a point which is less than 10% peak reverse current.

Reverse recovery time is a direct function of the forward current prior to the application of reverse voltage.

For any given rectifier, recovery time is very circuit dependent. Typical and maximum recovery time of all Motorola fast recovery power rectifiers are rated under a fixed set of conditions using I_F = 1.0 A, V_R = 30 V. In order to cover all circuit conditions, curves are given for typical recovered stored charge versus commutation di/dt for various levels of forward current and for junction temperatures of 25°C, 75°C, 100°C, and 150°C.

To use these curves, it is necessary to know the forward current level just before commutation, the circuit commutation di/dt, and the operating junction temperature. The reverse recovery test current waveform for all Motorola fast recovery rectifiers is shown.



From stored charge curves versus di/dt, recovery time (t_{rr}) and peak reverse recovery current ($I_{RM(REC)}$) can be closely approximated using the following formulas

$$t_{rr} = 1.41 \times \left[\frac{Q_R}{di/dt}\right]^{1/2}$$

$$I_{RM(REC)} = 1.41 \times \left[Q_R \times di/dt\right]^{1/2}$$

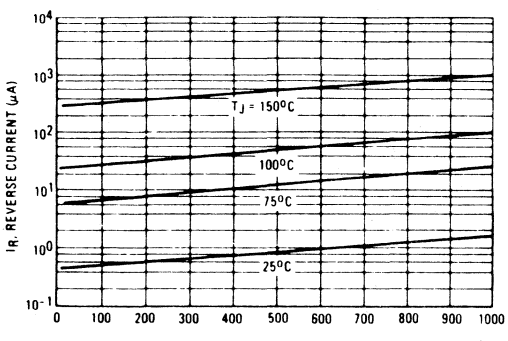


FIGURE 23 – TYPICAL REVERSE LEAKAGE

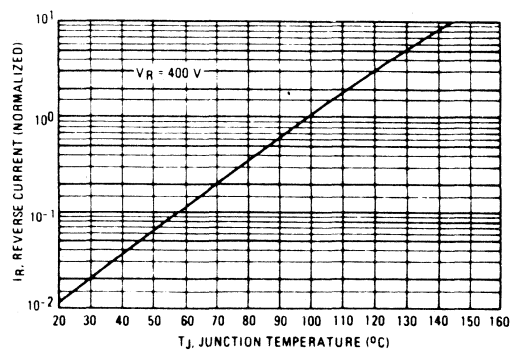


FIGURE 24 – TYPICAL REVERSE LEAKAGE

7

BY 206/207

SUBMINIATURE SIZE, AXIAL LEAD MOUNTED FAST RECOVERY POWER RECTIFIERS

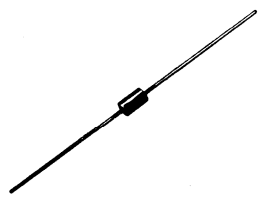
. . . designed for special applications such as dc power supplies, inverters, converters, ultrasonic systems, choppers, low RF interference and free wheeling diodes. A complete line of fast recovery rectifiers having typical recovery time of 200 nanoseconds providing high efficiency at frequencies to 250 Hz.

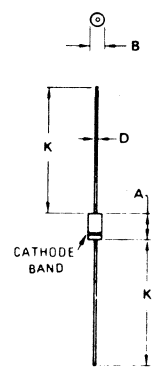
DESIGNER'S DATA FOR „WORST CASE" CONDITIONS

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit curves – representing device characteristic boundaries – are given to facilitate „worst case" design.

FAST RECOVERY POWER RECTIFIERS

350, 600 VOLTS
0.6 AMPERE





	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94	-	1.100	-

CASE 59-04

MAXIMUM RATINGS

Ratings	Symbol	BY206	BY207	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RWM} V_{RRM} V_R	350	600	Volts
Non Repetitive Peak Reverse Voltage	V_{RSM}	450	800	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	250	420	Volts
Average Rectified Forward Current (Single phase, resistive load, T_A = 75° C)	I_O	0.6		Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions) (T_A = 25° C)	I_{FSM}	25		Amps
Operating Junction Temp. Range	T_J	–65 to +150		°C
Storage Temperature Range	T_{stg}	–65 to +175		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max.	Unit
Thermal Resistance, Junction to Ambient (Typical Printed Circuit Board Mounting)	$R_{\theta JA}$	65	°C/W

ELECTICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Forward Voltage (I_F = 2,0 Amp., T_A = 125 °C)	V_F	—	1.1	1.2	Volts
Reverse Current (Rated dc Voltage) T_A = 25° C T_A = 100° C	I_R	— —	1.0 5.0	10 125	μA

REVERSE RECOVERY CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Reverse Recovery Time I_F = 10 mA to V_R = 50 V	t_{rr}	—	—	300	ns

MECHANICAL CHARACTERISTICS

CASE: Void Free, Transfer Molded

FINISH: External leads are tin plated, leads are readily solderable

POLARITY: Cathode indicated by Polarity band

WEIGHT: 0.4 Grams (Approximately)

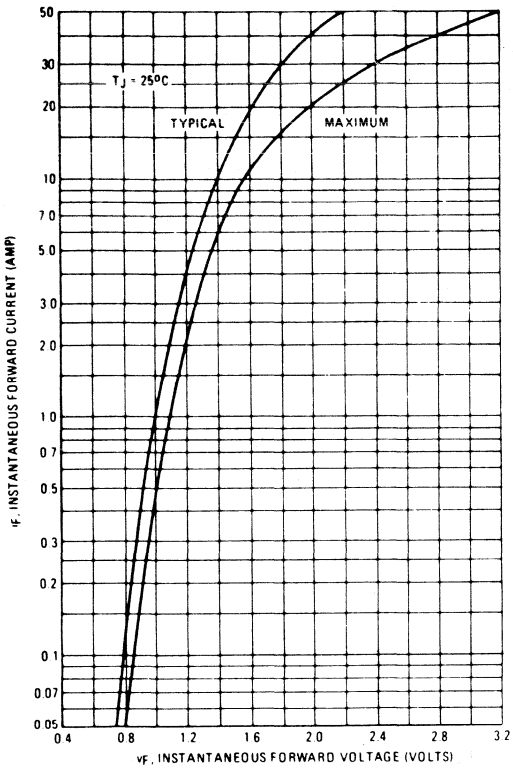


FIGURE 1 – FORWARD VOLTAGE

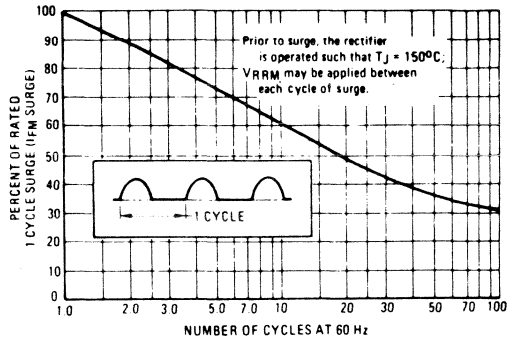


FIGURE 2 – MAXIMUM SURGE CAPABILITY

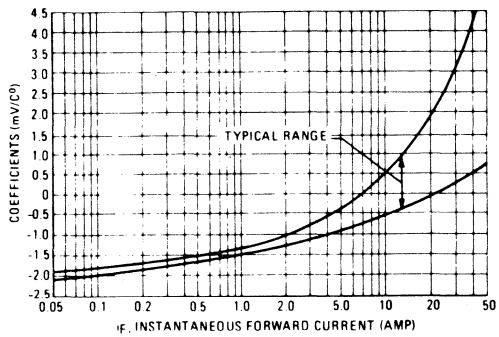


FIGURE 3 – TEMPERATURE COEFFICIENT

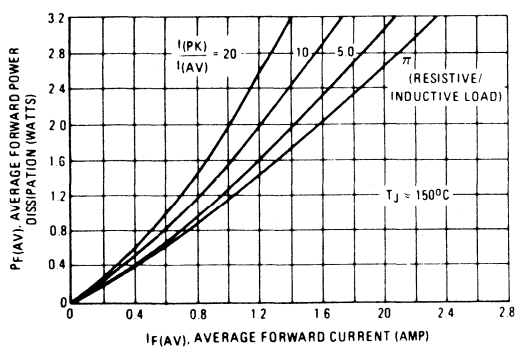


FIGURE 4 – FORWARD POWER DISSIPATION

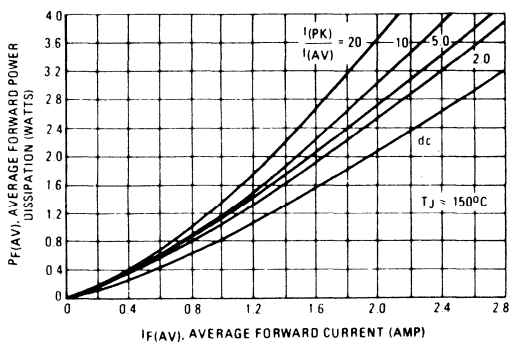


FIGURE 5 – FORWARD POWER DISSIPATION

7

MAXIMUM CURRENT RATINGS
(SEE NOTES 1 and 2)

SINE WAVE INPUT

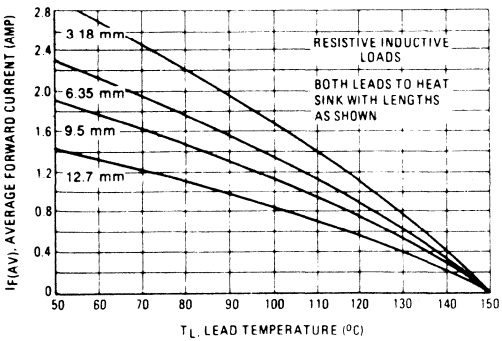


FIGURE 6 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

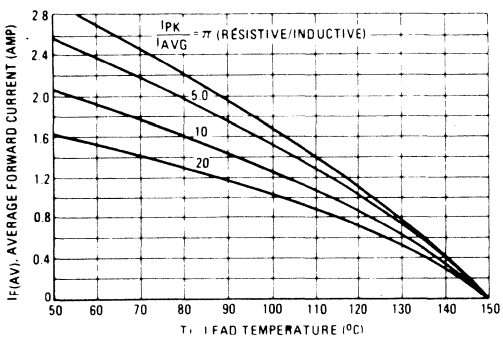


FIGURE 8 — 3.18 mm LEAD LENGTH, VARIOUS LOADS

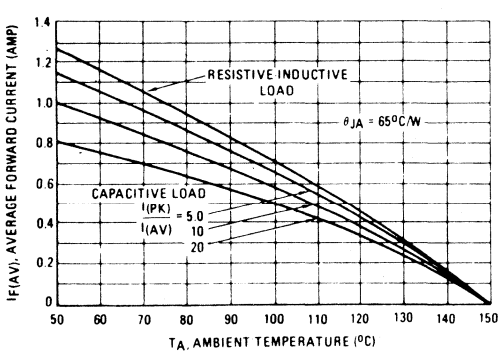


FIGURE 10 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS

SQUARE WAVE INPUT

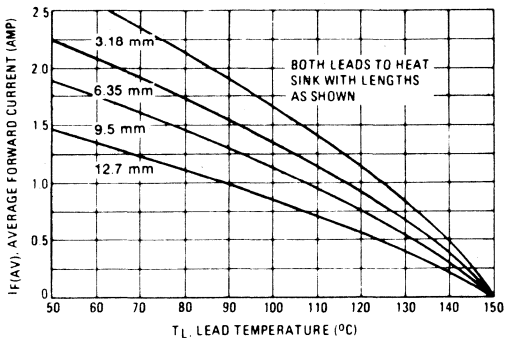


FIGURE 7 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

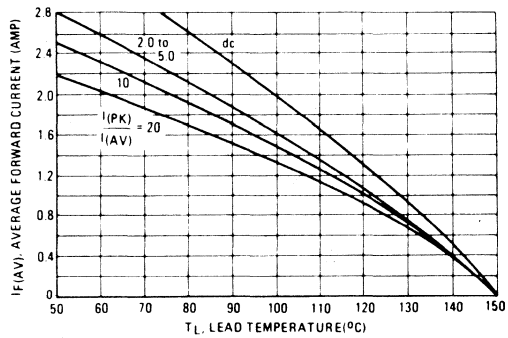


FIGURE 9 — 3.18 mm LEAD LENGTH, VARIOUS LOADS

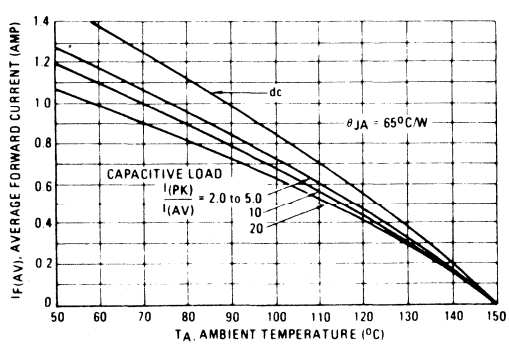


FIGURE 11 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS

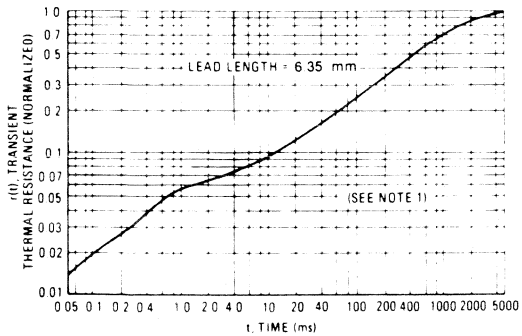


FIGURE 12 – THERMAL RESPONSE

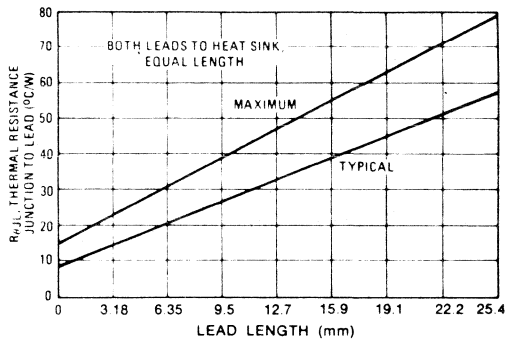
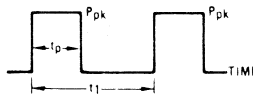


FIGURE 13 – THERMAL RESISTANCE

NOTE 1



DUTY CYCLE: $D = t_p / t_1$
PEAK POWER, P_{pk}, is peak of an equivalent square power pulse.

To determine maximum junction temperature of the diode in a given situation, the following procedure is recommended:

The temperature of the case should be measured using a thermocouple placed on the case as close as possible to the tie point. The thermal mass connected to the tie point is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady-state conditions are achieved. Using the measured value of T_C, the junction temperature may be determined by:

$$T_J = T_C + \Delta T_{JC}$$

where ΔT_{JC} is the increase in junction temperature above the case temperature. It may be determined by:

$$\Delta T_{JC} = P_{pk} \cdot R_{\theta JC} \left[D + (1 - D) \cdot r(t_1 + t_p) + r(t_p) - r(t_1) \right]$$

where:

$r(t)$ = normalized value of transient thermal resistance at time, t, from Figure 12, i.e.:

$r(t_1 + t_p)$ = normalized value of transient thermal resistance at time $t_1 + t_p$

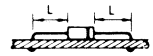
NOTE 2

Data shown for thermal resistance junction-to-ambient (θ_{JA}) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

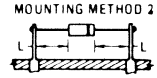
TYPICAL VALUES FOR θ_{JA} IN STILL AIR

MOUNTING METHOD	LEAD LENGTH, L(mm) 3.81	6.35	12.7	19.1	$R_{\theta JA}$
1	65	72	82	92	°C/W
2	74	81	91	101	°C/W
3	40				°C/W

MOUNTING METHOD 1

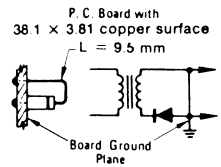


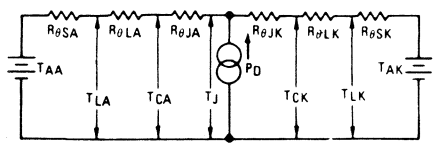
MOUNTING METHOD 2



Vector pin mounting

MOUNTING METHOD 3





Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heat sink. Terms in the model signify:

T_A = Ambient Temperature
T_L = Lead Temperature
T_C = Case Temperature
T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_D = Power Dissipation

(Subscripts A and K refer to anode and cathode sides respectively.)

Values for thermal resistance components are:

$R_{\theta L}$ = 112°C/W/IN Typically and 128°C/W/IN Maximum
$R_{\theta J}$ = 18°C/W Typically and 30°C/W Maximum

The maximum lead temperature may be calculated as follows:

$$T_L = 150^\circ - \Delta T_{JL}$$

ΔT_{JL} can be calculated as shown in NOTE 1 or it may be approximated as follows:

$\Delta T_{JL} \approx R_{\theta JL} \cdot P_F$. P_F may be formulated for sine-wave operation from Figure 3 or from Figure 4 for square-wave operation.

FIGURE 14 – THERMAL CIRCUIT MODEL

7

TYPICAL DYNAMIC CHARACTERISTICS

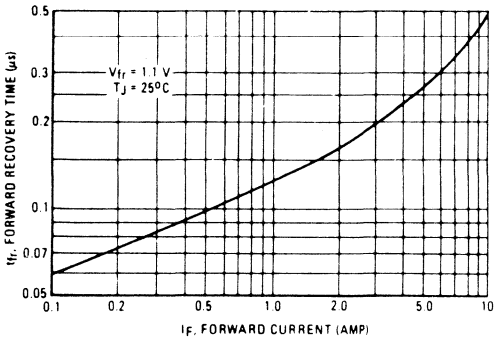


FIGURE 15 – FORWARD RECOVERY TIME

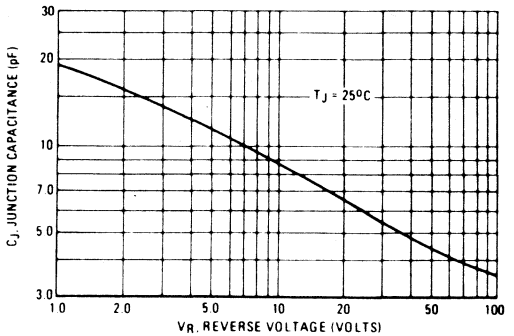


FIGURE 16 – JUNCTION CAPACITANCE

TYPICAL RECOVERED STORED CHARGE DATA
(SEE NOTE 3)

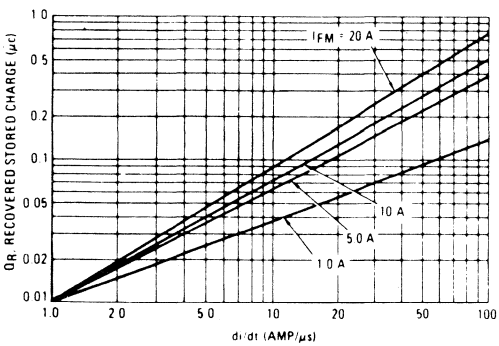


FIGURE 17 – T_J = 25°C

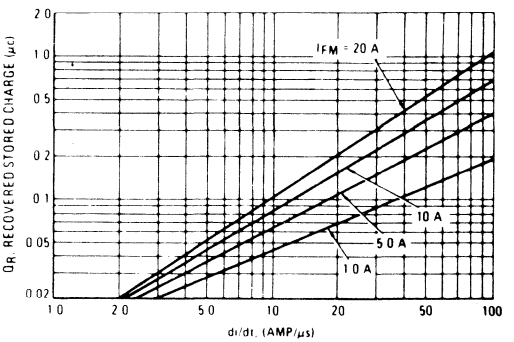


FIGURE 18 – T_J = 75°C

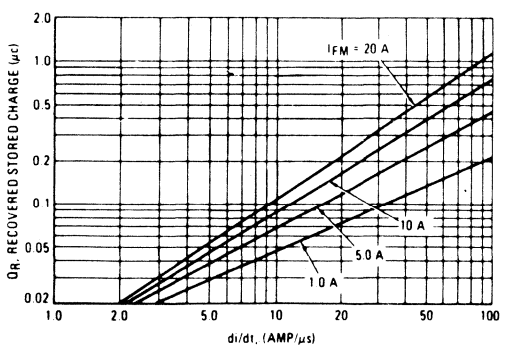


FIGURE 19 – T_J = 100°C

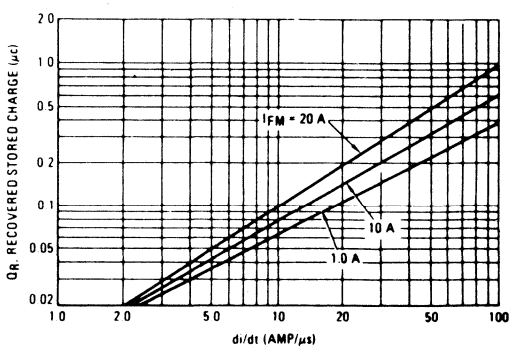


FIGURE 20 – T_J = 150°C

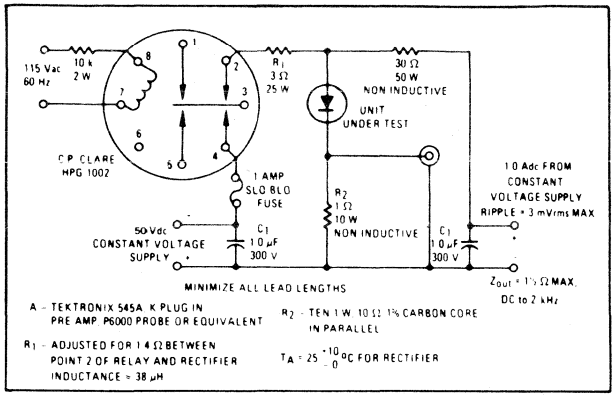


FIGURE 21 – REVERSE RECOVERY CIRCUIT

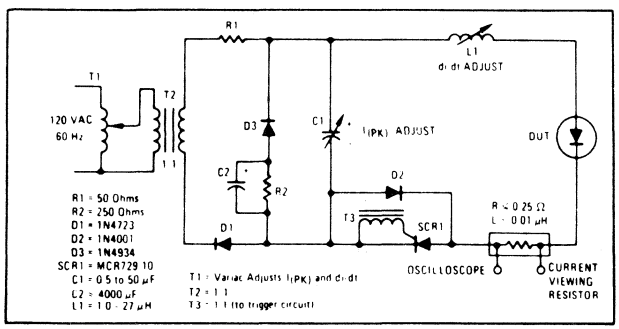


FIGURE 22 – JEDEC REVERSE RECOVERY CIRCUIT

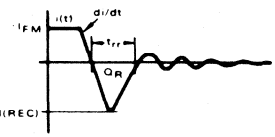
NOTE 3

Reverse recovery time is the period which elapses from the time that the current, thru a previously forward biased rectifier diode, passes thru zero going negatively until the reverse current recovers to a point which is less than 10% peak reverse current.

Reverse recovery time is a direct function of the forward current prior to the application of reverse voltage.

For any given rectifier, recovery time is very circuit dependent. Typical and maximum recovery time of all Motorola fast recovery power rectifiers are rated under a fixed set of conditions using I_F = 1.0 A, V_R = 30 V. In order to cover all circuit conditions, curves are given for typical recovered stored charge versus commutation di/dt for various levels of forward current and for junction temperatures of 25°C, 75°C, 100°C, and 150°C.

To use these curves, it is necessary to know the forward current level just before commutation, the circuit commutation di/dt, and the operating junction temperature. The reverse recovery test current waveform for all Motorola fast recovery rectifiers is shown.



From stored charge curves versus di/dt, recovery time (t_{rr}) and peak reverse recovery current ($I_{RM(REC)}$) can be closely approximated using the following formulas:

$$t_{rr} = 1.41 \times \left[\frac{Q_R}{di/dt}\right]^{1/2}$$

$$I_{RM(REC)} = 1.41 \times \left[Q_R \times di/dt\right]^{1/2}$$

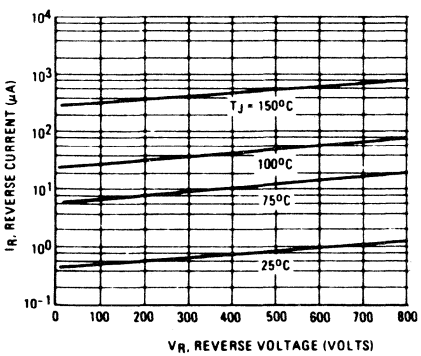


FIGURE 23 – TYPICAL REVERSE LEAKAGE

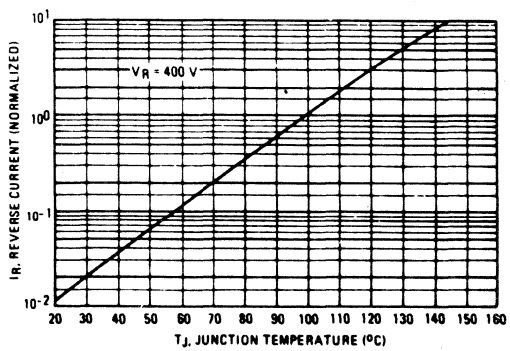


FIGURE 24 – TYPICAL REVERSE LEAKAGE

7

BY 210—400 SERIES

SUBMINIATURE SIZE, AXIAL LEAD MOUNTED FAST RECOVERY POWER RECTIFIERS

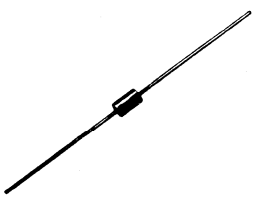
. . . designed for special applications such as dc power supplies, inverters, converters, ultrasonic systems, choppers, low RF interference and free wheeling diodes. A complete line of fast recovery rectifiers having typical recovery time of 300 nanoseconds providing high efficiency at frequencies to 250 Hz.

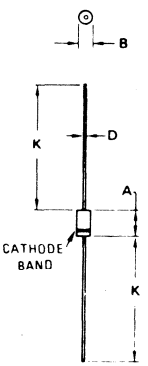
DESIGNER'S DATA FOR „WORST CASE" CONDITIONS

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing device characteristic boundaries — are given to facilitate „worst case" design.

FAST RECOVERY POWER RECTIFIERS

400, 600, 800 VOLTS
1 AMPERE





	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94	–	1.100	–

CASE 59-04

MAXIMUM RATINGS

Ratings	Symbol	BY 210—400	BY 210—600	BY 210—800	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RWM} V_{RRM} V_R	400	600	800	Volts
Non Repetitive Peak Reverse Voltage	V_{RSM}	500	800	1000	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	280	420	560	Volts
Average Rectified Forward Current (Single phase, resistive load, T_A = 75° C)	I_O	1,0			Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions) (T_A = 75° C)	I_{FSM}	40			Amps
Operating Junction Temp. Range	T_J	–65 to +150			°C
Storage Temperature Range	T_{stg}	–65 to +175			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max.	Unit
Thermal Resistance, Junction to Ambient (Typical Printed Circuit Board Mounting)	$R_{\theta JA}$	65	°C/W

ELECTICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Forward Voltage (I_F = 2,0 Amp., T_A = 25 °C)	V_F	—	1,1	1,2	Volts
Reverse Current (rated dc voltage) T_A = 25° C T_A = 100° C	I_R	— —	1,0 5,0	10 100	μA

REVERSE RECOVERY CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Reverse Recovery Time I_F = 10 mA to V_R = 50 V	t_{rr}	—	—	300	ns

MECHANICAL CHARACTERISTICS

CASE: Void Free, Transfer Molded

FINISH: External leads are tin plated, leads are readily solderable

POLARITY: Cathode indicated by Polarity band

WEIGHT: 0.4 Grams (Approximately)

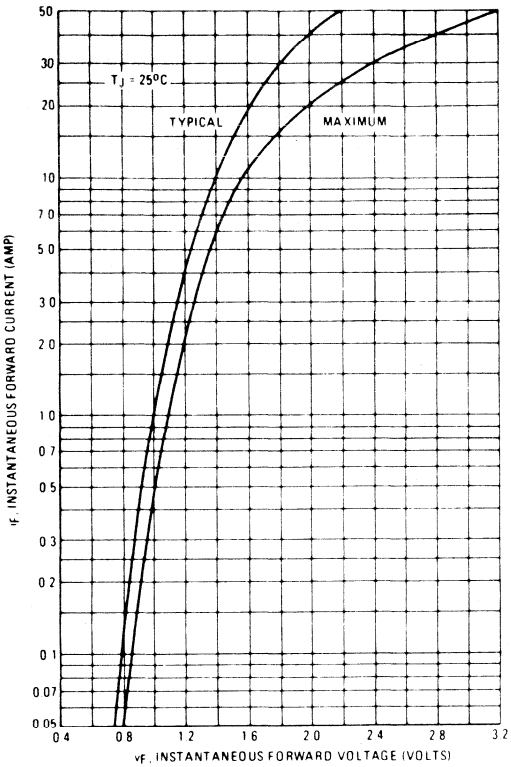


FIGURE 1 – FORWARD VOLTAGE

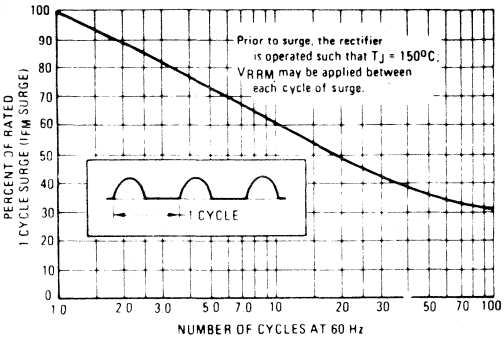


FIGURE 2 – MAXIMUM SURGE CAPABILITY

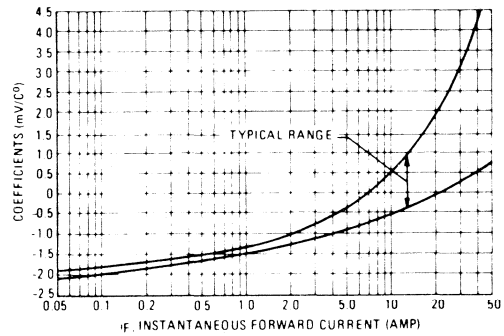


FIGURE 3 – TEMPERATURE COEFFICIENT

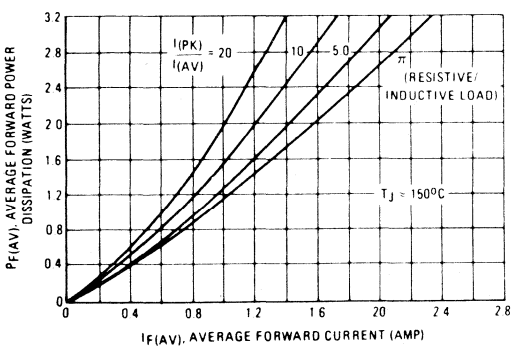


FIGURE 4 – FORWARD POWER DISSIPATION

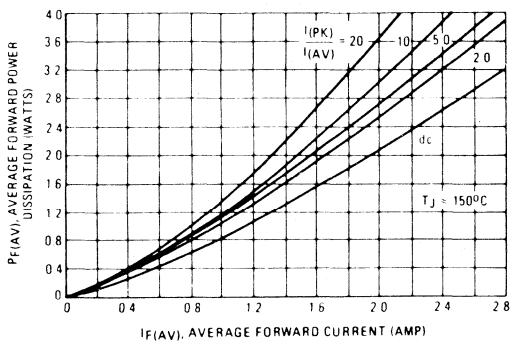


FIGURE 5 – FORWARD POWER DISSIPATION

7

MAXIMUM CURRENT RATINGS
(SEE NOTES 1 and 2)

SINE WAVE INPUT

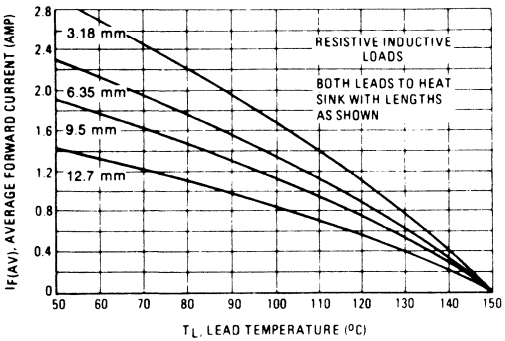


FIGURE 6 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

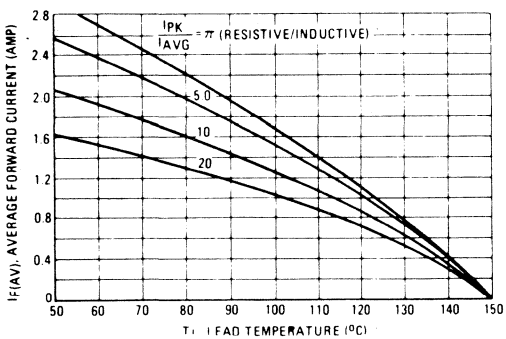


FIGURE 8 — 3.18 mm LEAD LENGTH, VARIOUS LOADS

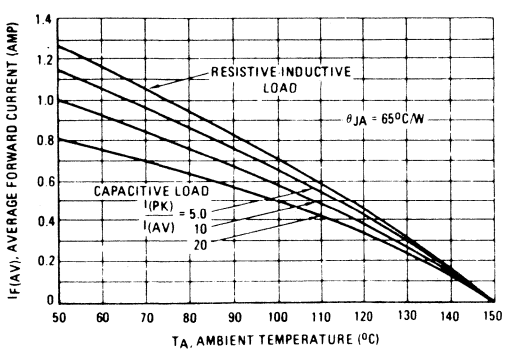


FIGURE 10 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS

SQUARE WAVE INPUT

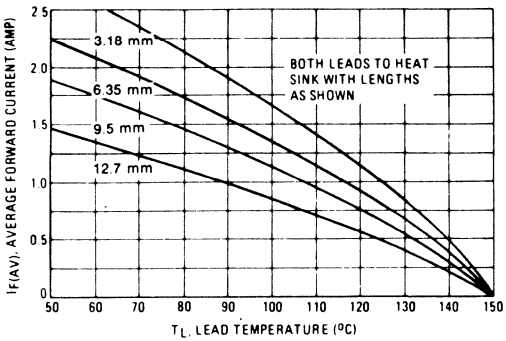


FIGURE 7 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

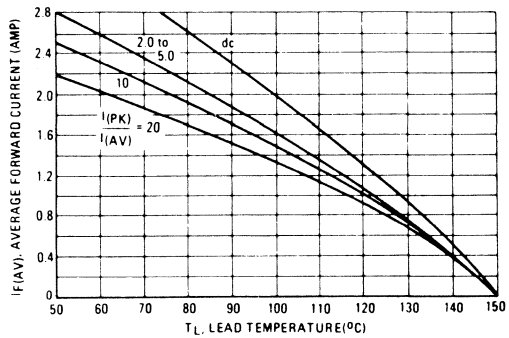


FIGURE 9 — 3.18 mm LEAD LENGTH, VARIOUS LOADS

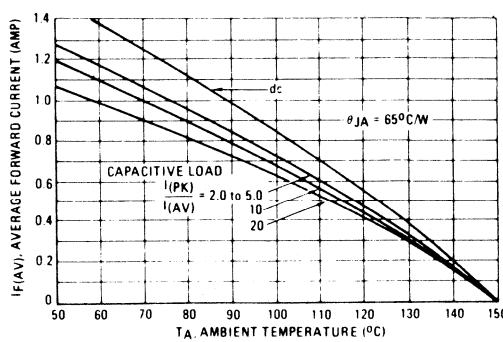


FIGURE 11 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS

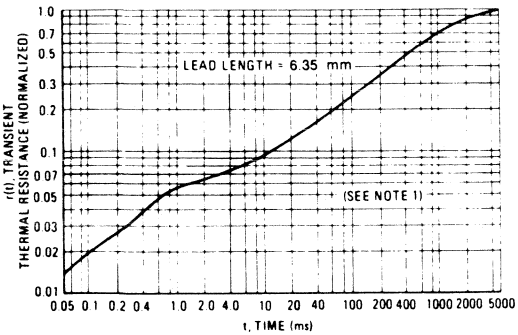


FIGURE 12 – THERMAL RESPONSE

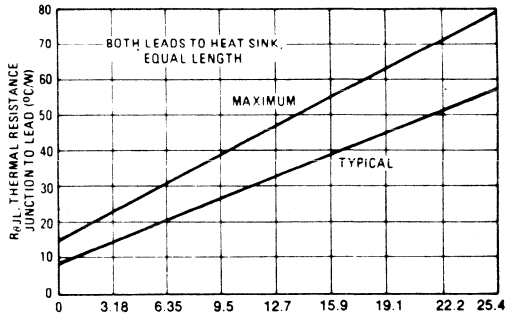
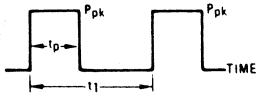


FIGURE 13 – THERMAL RESISTANCE

NOTE 1



DUTY CYCLE, $D = t_p/t_1$
PEAK POWER, P_{pk}, is peak of an equivalent square power pulse.

To determine maximum junction temperature of the diode in a given situation, the following procedure is recommended.

The temperature of the case should be measured using a thermocouple placed on the case as close as possible to the tie point. The thermal mass connected to the tie point is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady-state conditions are achieved. Using the measured value of T_C, the junction temperature may be determined by:

$$T_J = T_C + \Delta T_{JC}$$

where ΔT_{JC} is the increase in junction temperature above the case temperature. It may be determined by:

$$\Delta T_{JC} = P_{pk} \cdot R_{\theta JC}\left[D + (1 - D) \cdot r(t_1 + t_p) + r(t_p) - r(t_1)\right]$$

where

$r(t)$ = normalized value of transient thermal resistance at time, t, from Figure 12, i.e.:

$r(t_1 + t_p)$ = normalized value of transient thermal resistance at time $t_1 + t_p$.

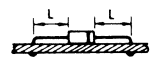
NOTE 2

Data shown for thermal resistance junction-to-ambient (θ_{JA}) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

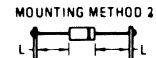
TYPICAL VALUES FOR θ_{JA} IN STILL AIR

MOUNTING METHOD	LEAD LENGTH, L (mm) 3.81	6.35	12.7	19.1	$R_{\theta JA}$
1	65	72	82	92	°C/W
2	74	81	91	101	°C/W
3			40		°C/W

MOUNTING METHOD 1

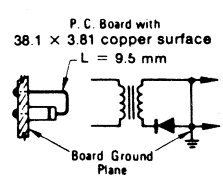


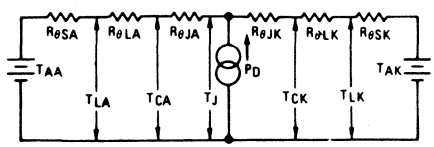
MOUNTING METHOD 2



Vector pin mounting

MOUNTING METHOD 3





Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heat sink. Terms in the model signify:

T_A = Ambient Temperature
T_L = Lead Temperature
T_C = Case Temperature
T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_D = Power Dissipation

(Subscripts A and K refer to anode and cathode sides respectively.)

Values for thermal resistance components are:

$R_{\theta L}$ = 112°C/W/IN. Typically and 128°C/W/IN Maximum

$R_{\theta J}$ = 18°C/W Typically and 30°C/W Maximum

The maximum lead temperature may be calculated as follows:

$T_L = 150^{\circ} - \Delta T_{JL}$

ΔT_{JL} can be calculated as shown in NOTE 1 or it may be approximated as follows:

$\Delta T_{JL} \approx R_{\theta JL} \cdot P_F$; P_F may be formulated for sine-wave operation from Figure 3 or from Figure 4 for square-wave operation.

FIGURE 14 – THERMAL CIRCUIT MODEL

TYPICAL DYNAMIC CHARACTERISTICS

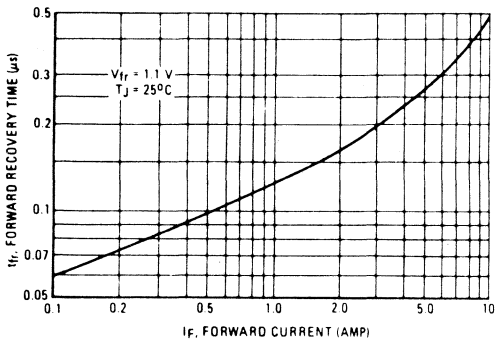


FIGURE 15 – FORWARD RECOVERY TIME

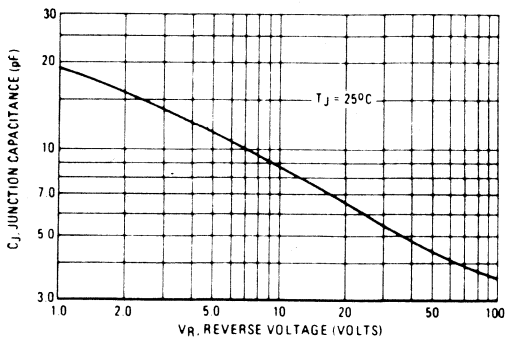


FIGURE 16 – JUNCTION CAPACITANCE

TYPICAL RECOVERED STORED CHARGE DATA
(SEE NOTE 3)

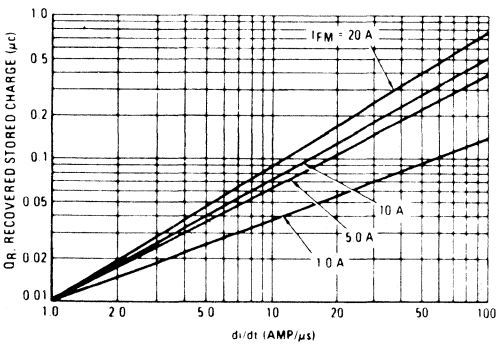


FIGURE 17 – T_J = 25°C

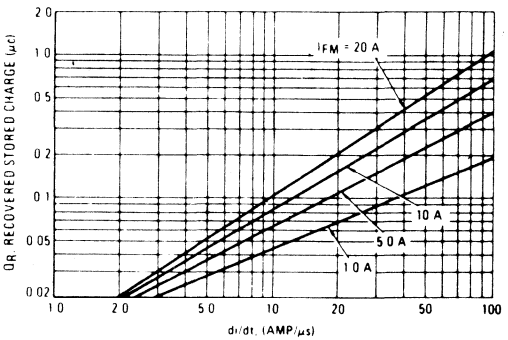


FIGURE 18 – T_J = 75°C

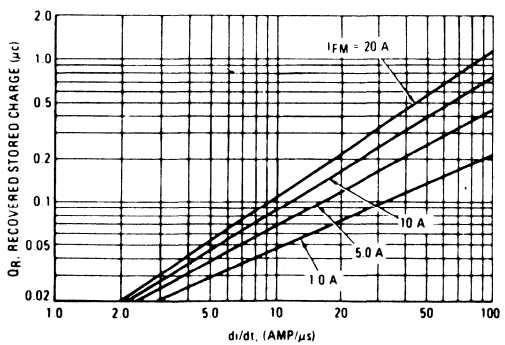


FIGURE 19 – T_J = 100°C

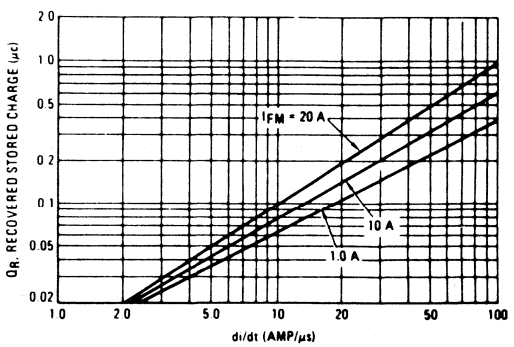


FIGURE 20 – T_J = 150°C

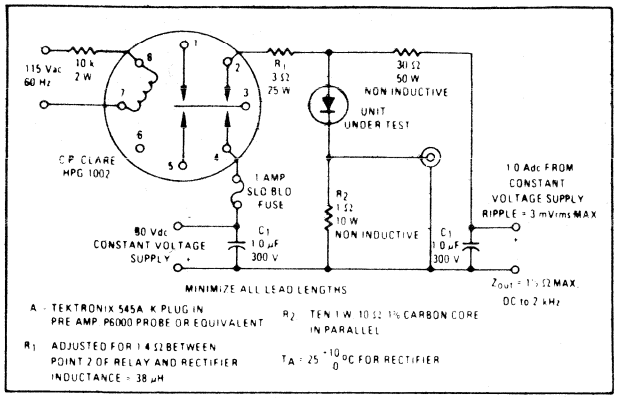


FIGURE 21 – REVERSE RECOVERY CIRCUIT

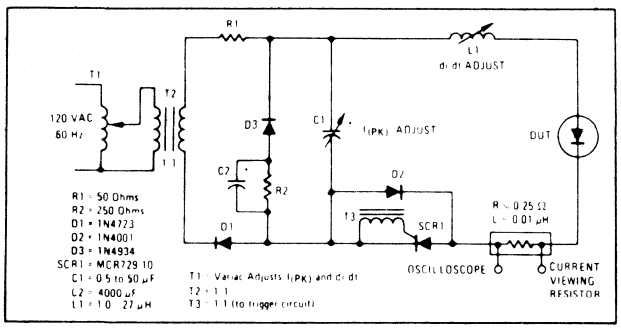


FIGURE 22 – JEDEC REVERSE RECOVERY CIRCUIT

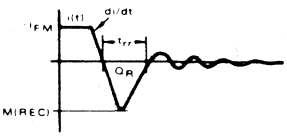
NOTE 3

Reverse recovery time is the period which elapses from the time that the current, thru a previously forward biased rectifier diode, passes thru zero going negatively until the reverse current recovers to a point which is less than 10% peak reverse current.

Reverse recovery time is a direct function of the forward current prior to the application of reverse voltage.

For any given rectifier, recovery time is very circuit dependent. Typical and maximum recovery time of all Motorola fast recovery power rectifiers are rated under a fixed set of conditions using I_F = 1.0 A, V_R = 50 V. In order to cover all circuit conditions, curves are given for typical recovered stored charge versus commutation di/dt for various levels of forward current and for junction temperatures of 25°C, 75°C, 100°C, and 150°C.

To use these curves, it is necessary to know the forward current level just before commutation, the circuit commutation di/dt, and the operating junction temperature. The reverse recovery test current waveform for all Motorola fast recovery rectifiers is shown.



From stored charge curves versus di/dt, recovery time (t_{rr}) and peak reverse recovery current ($I_{RM(REC)}$) can be closely approximated using the following formulas:

$$t_{rr} = 1.41 \times \left[\frac{Q_R}{di/dt}\right]^{1/2}$$

$$I_{RM(REC)} = 1.41 \times \left[Q_R \times di/dt\right]^{1/2}$$

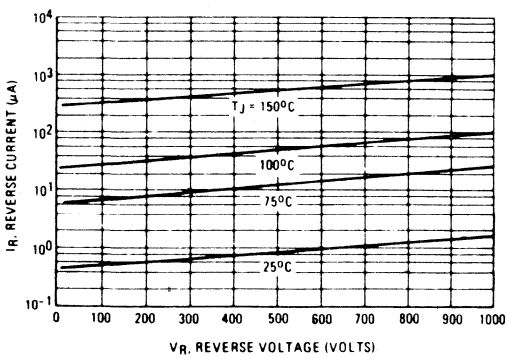


FIGURE 23 – TYPICAL REVERSE LEAKAGE

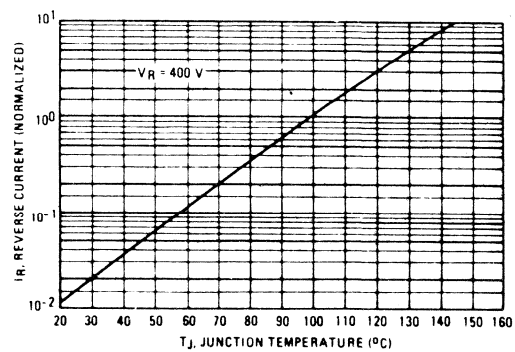


FIGURE 24 – TYPICAL REVERSE LEAKAGE

BY 251 SERIES

MINIATURE SIZE, AXIAL LEAD MOUNTED STANDARD RECOVERY POWER RECTIFIERS

. . . designed for use in T. V. line deflection, power supplies and other applications having need of a device with the following features:

- High Current to Small Size
- High Surge Current Capability
- Low Forward Voltage Drop
- Void-Free Economical Plastic Package
- Available in Volume Quantities

Designer's Data for "Worst Case" Conditions

The Designers Data sheets permit the design of most circuits entirely from the information presented Limit curves representing boundaries on device characteristics are given to facilitate "worst case" design

STANDARD RECOVERY POWER RECTIFIERS

200–1300 VOLTS
3 AMPERES

MAXIMUM RATINGS

Rating	Symbol	BY 251	BY 252	BY 253	BY 254	BY 255	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	200	400	600	800	1300	Volts
Non-Repetitive Peak Reverse Voltage	V_{RSM}	250	450	650	850	1350	Volts
Average Rectified Forward Current (Single phase resistive load, T_A = 95°C, PC Board Mounting) (1) (EIA Standard Conditions L = 1/32", T_L = 85°C)	I_O	← 3.0 → ← 8.0 →					Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions)	I_{FSM}	← 100 → (one cycle)					Amp
Operating and Storage Junction Temperature Range (2)	T_J, T_{stg}	← −65 to +175 →					°C

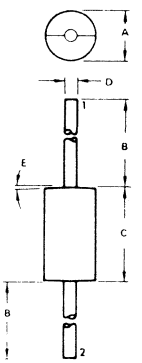
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient (Recommended Printed Circuit Board Mounting, See Note 2 on Page 4)	$R_{\theta JA}$	28	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Instantaneous Forward Voltage (3) (I_F = 9.4 Amp, T_J = 175°C) (I_F = 3.0 Amp, T_J = 25°C)	v_F	- -	0.9 0.9	1.0 1.0	Volts
Reverse Current (rated dc voltage) (3) T_J = 25°C T_J = 100°C	I_R		0.1 2.8	10 500	μA

(1) Derate for reverse power dissipation See Note on Page 2.
(2) Derate as shown in Figure 1
(3) Pulse Test Pulse Width = 300 μs, Duty Cycle = 2.0%



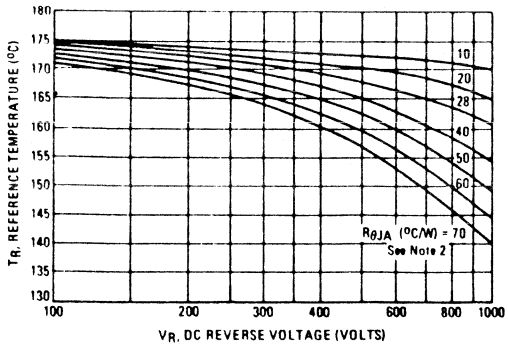
	INCHES		MILLIMETERS	
A	0.190	0.210	4.83	5.33
B	1.062	1.072	26.97	27.23
C	0.370	0.380	9.40	9.65
D	0.048	0.052	1.22	1.32
E	2°		2°	

CASE 267

MECHANICAL CHARACTERISTICS

Case: Void Free, Transfer Molded
Finish: External Leads are Plated, Leads are readily Solderable
Polarity: Indicated by Cathode Band
Weight: 1.1 Grams (Approximately)
Maximum Lead Temperature for Soldering Purposes:
300°C, 1/8" from case for 10 s at 5.0 lb. tension

FIGURE 1 – MAXIMUM REFERENCE TEMPERATURE



CURRENT DERATING
(Reverse Power Loss Neglected)

FIGURE 3 – PC BOARD MOUNTING

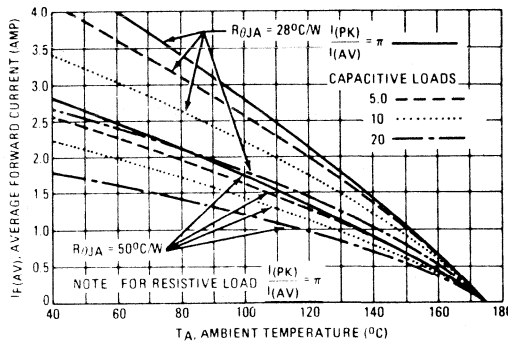


FIGURE 2 – MAXIMUM SURGE CAPABILITY

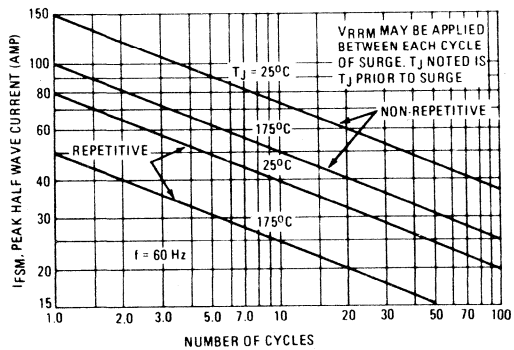
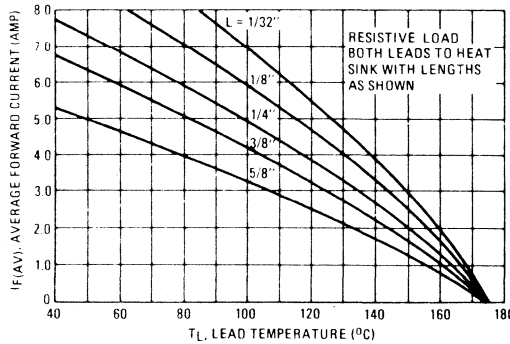


FIGURE 4 – SEVERAL LEAD LENGTHS



7

FIGURE 5 – 1/8" LEAD LENGTH

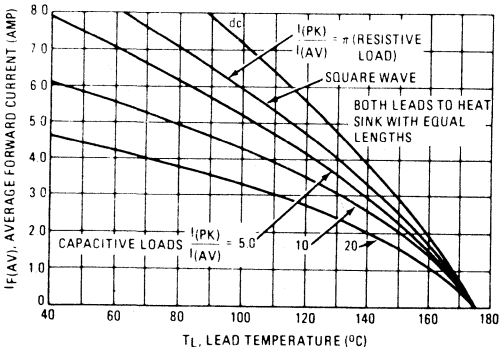


FIGURE 6 – MAXIMUM FORWARD VOLTAGE

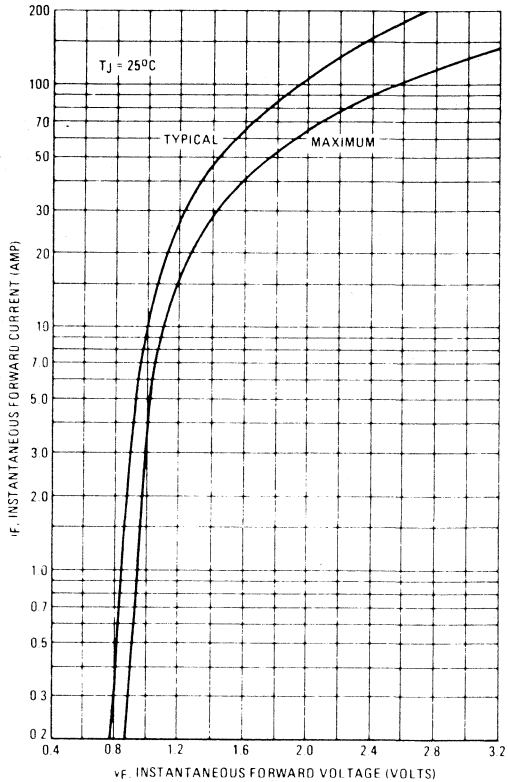


FIGURE 7 – FORWARD VOLTAGE TEMPERATURE COEFFICIENT

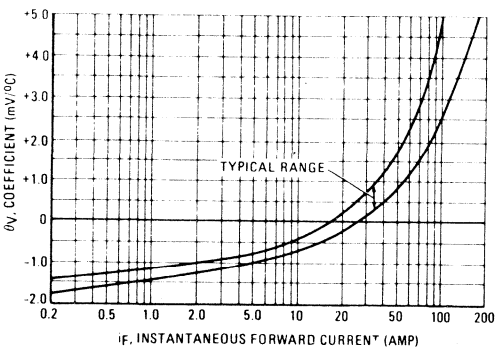


FIGURE 8 – FORWARD POWER DISSIPATION

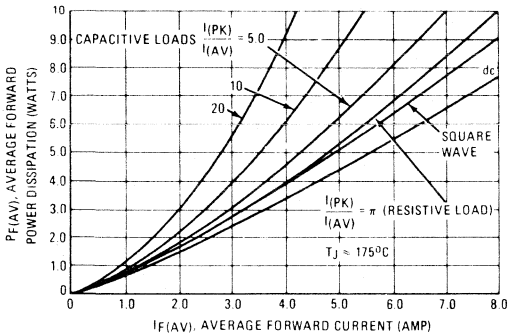
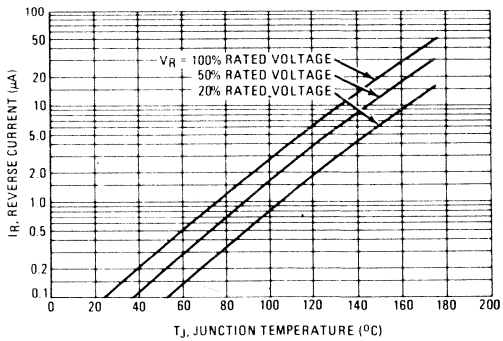


FIGURE 9 – TYPICAL REVERSE CURRENT



THERMAL CHARACTERISTICS

FIGURE 10 – THERMAL RESPONSE

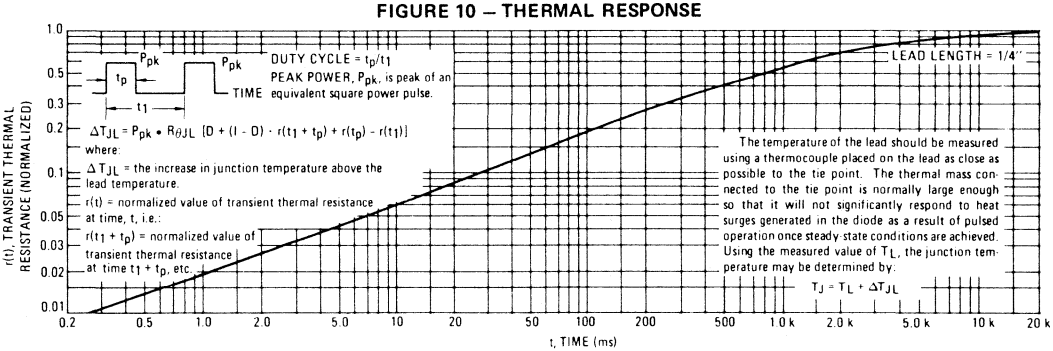
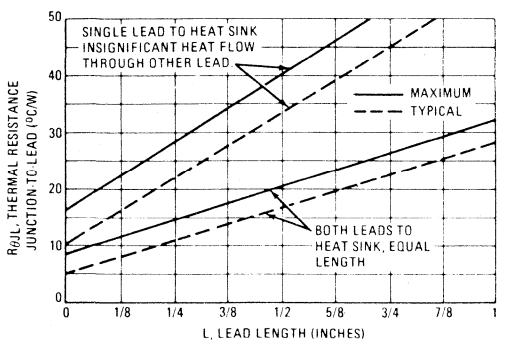


FIGURE 11 – STEADY-STATE THERMAL RESISTANCE



NOTE 1 – AMBIENT MOUNTING DATA

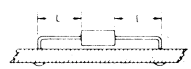
Data shown for thermal resistance junction-to-ambient ($R_{\theta JA}$) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

TYPICAL VALUES FOR $R_{\theta JA}$ IN STILL AIR

MOUNTING METHOD	LEAD LENGTH, L (IN)				$R_{\theta JA}$
	1/8	1/4	1/2	3/4	
1	50	51	53	55	°C/W
2	58	59	61	63	°C/W
3	28				°C/W

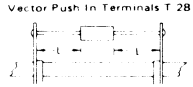
MOUNTING METHOD 1

P.C. Board Where Available Copper Surface area is small.



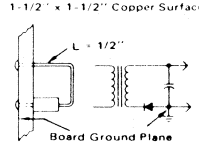
MOUNTING METHOD 2

Vector Push In Terminals T 28



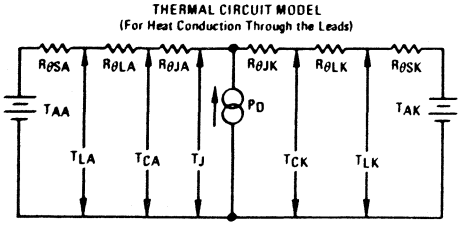
MOUNTING METHOD 3

P.C. Board with 1-1/2" x 1-1/2" Copper Surface



7

FIGURE 12 – APPROXIMATE THERMAL CIRCUIT MODEL



Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heat sink. Terms in the model signify:

T_A = Ambient Temperature
T_L = Lead Temperature
T_C = Case Temperature
T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_D = Total Power Dissipation = $P_F + P_R$
P_F = Forward Power Dissipation
P_R = Reverse Power Dissipation

(Subscripts A and K refer to anode and cathode sides respectively.) Values for thermal resistance components are:

$R_{\theta L}$ = 46°C/W/IN. Typically and 48°C/W/IN Maximum.
$R_{\theta J}$ = 10°C/W Typically and 16°C/W Maximum.

The maximum lead temperature may be found as follows:

$$T_L = T_{J(max)} - \Delta T_{JL}$$

where $\Delta T_{JL} \approx R_{\theta JL}$

TYPICAL DYNAMIC CHARACTERISTICS

(T_J = 25°C)

FIGURE 13 – FORWARD RECOVERY TIME

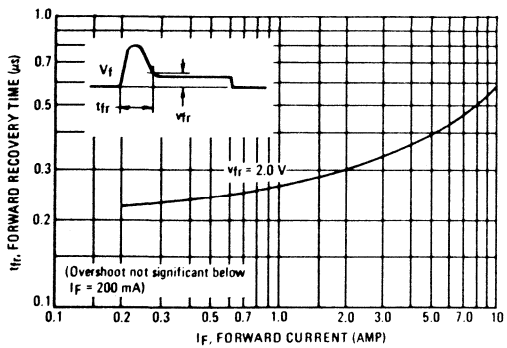


FIGURE 14 – REVERSE RECOVERY TIME

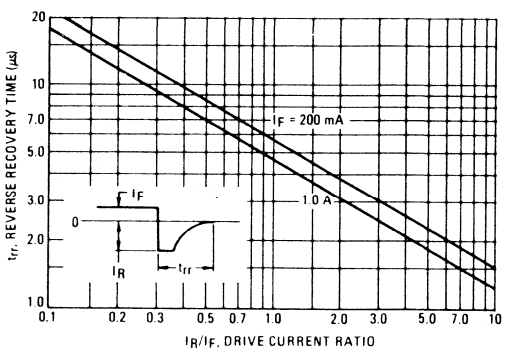


FIGURE 15 – RECTIFICATION WAVEFORM EFFICIENCY

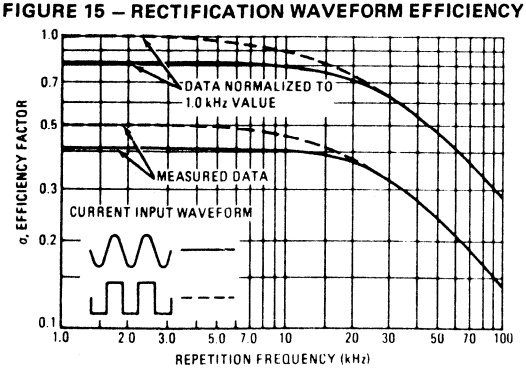
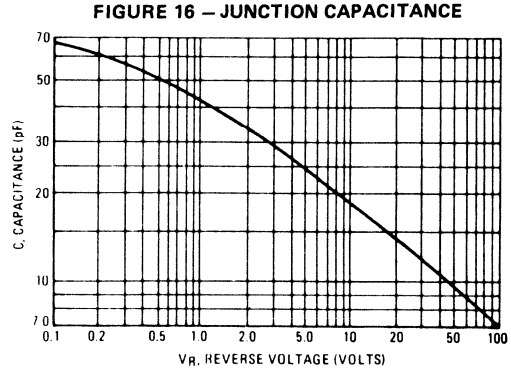


FIGURE 16 – JUNCTION CAPACITANCE



BY 296 SERIES

SOFT RECOVERY POWER RECTIFIERS

100–800 VOLTS
2,0 AMPERES

SUBMINIATURE SIZE, AXIAL LEAD MOUNTED SOFT RECOVERY POWER RECTIFIERS

. . . designed for special applications such as dc power supplies, inverters, converters, ultrasonic systems, choppers, low RF interference and free wheeling diodes. A complete line of fast recovery rectifiers having typical recovery time of 300 nanoseconds providing high efficiency at frequencies to 250 Hz.

DESIGNER'S DATA FOR „WORST CASE" CONDITIONS

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit curves – representing device characteristic bounderies – are given to facilitate „worst case" design.

MAXIMUM RATINGS

Ratings	Symbol	BY296	BY297	BY298	BY299	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RWM} V_{RRM} V_R	100	200	400	800	Volts
Non Repetitive Peak Reverse Voltage	V_{RSM}	200	300	500	1000	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	70	140	280	560	Volts
Average Rectified Forward Current (Single phase, resistive load, T_A = 90° C)	I_O	2 0				Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions)	I_{FSM}	70 (one cycle)				Amp
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +175				°C

THERMAL CHARACTERISTICS

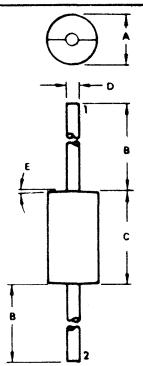
Characteristics	Symbol	Max.	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	28	°C

ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Forward Voltage (I_F = 3,0 Amp., T_J = 25° C)	V_F	—		1,25	Volts
Reverse Current (rated dc voltage) T_J = 25° C	I_R	—		10	μA

REVERSE RECOVERY CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Reverse Recovery Time I_F = 10 mA, to I_{RM} = 10 mA, 1 mA	t_{rr}	—	—	500	ns
I_F = 1 Amp. to V_R = 30 V_{DC}	t_{rr}			300	ns



	INCHES		MILLIMETERS	
A	0.190	0.210	4.83	5.33
B	1.062	1.072	26.97	27.23
C	0.370	0.380	9.40	9.65
D	0.048	0.052	1.22	1.32
E	2°		2°	

CASE 267

MECHANICAL CHARACTERISTICS

CASE . . . . . Void free, transfer molded

FINISH . . . . . .All external surfaces corrosion-resistant and the terminal leads are readily solderable

POLARITY . . . . . Cathode indicated by polarity band

MOUNTING POSITIONS . . . . . Any

SOLDERING . . . . . .220°C 1/16" from case for ten seconds

7

FIGURE 1 – FORWARD VOLTAGE

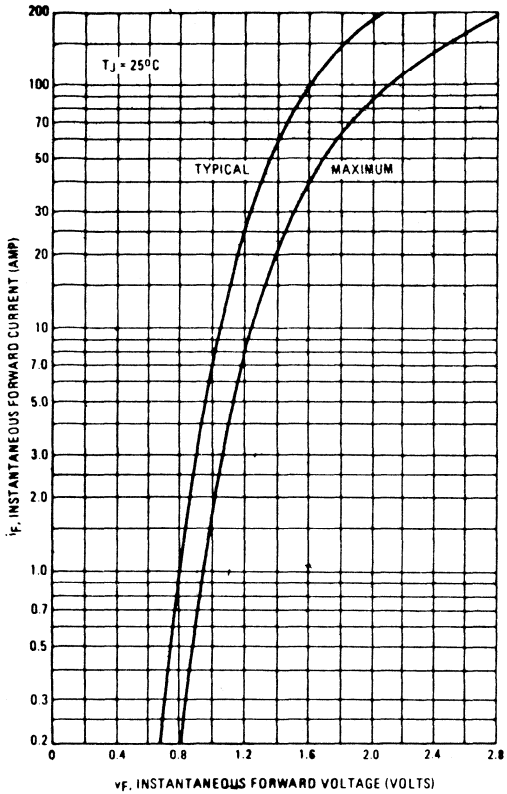


FIGURE 3 – REVERSE POWER DISSIPATION, SINE WAVE

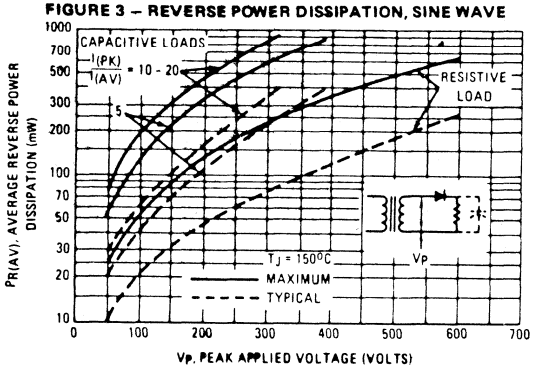


FIGURE 4 – REVERSE POWER DISSIPATION, SQUARE WAVE

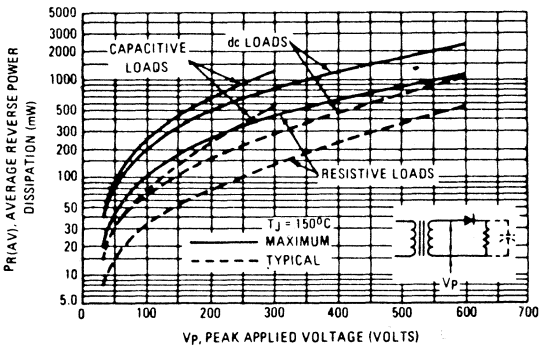
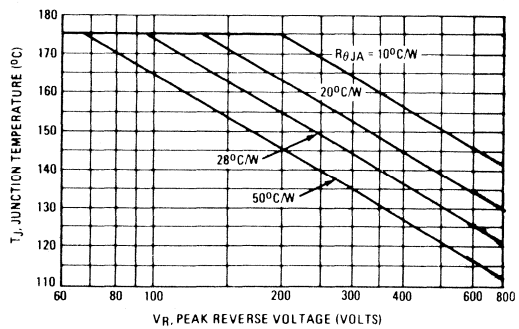


FIGURE 2 – MAXIMUM ALLOWABLE JUNCTION TEMPERATURE



NOTE 1
MAXIMUM JUNCTION TEMPERATURE DERATING

When operating this rectifier at junction temperatures over 120° C, reverse power dissipation and the possibility of thermal runaway must be considered. The data of Figure 2 is based upon worst case reverse power and should be used to derate $T_{J(max)}$ from its maximum value of 175° C.

FIGURE 5 – NORMALIZED REVERSE CURRENT

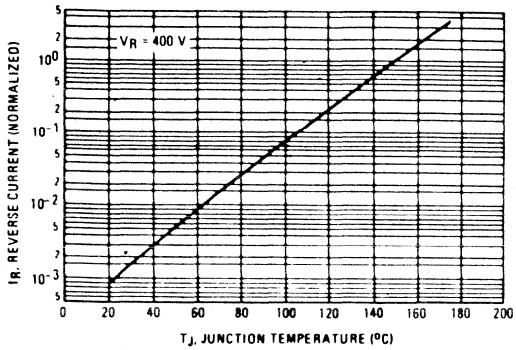
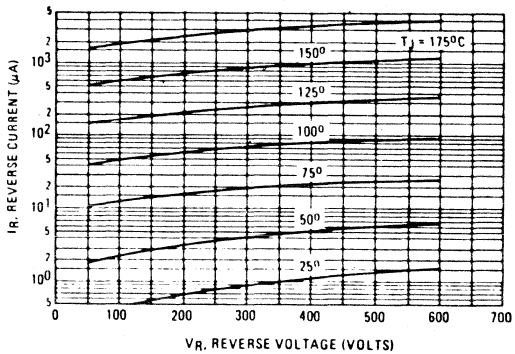


FIGURE 6 – TYPICAL REVERSE CURRENT



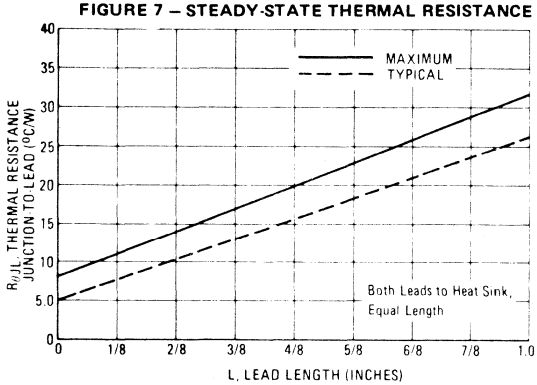
NOTE 2 – MOUNTING DATA

Data shown for thermal resistance junction-to-ambient ($R_{\theta}JA$) for the mountings shown is to be used as typical guideline values for preliminary engineering, or in case the tie point temperature cannot be measured.

TYPICAL VALUES FOR $R_{\theta}JA$ IN STILL AIR

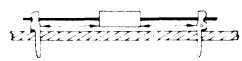
Mounting Method	Lead Length, L (in) 1/8	1/4	1/2	3/4	$R_{\theta}JA$
1	50	51	53	55	°C/W
2	58	59	61	63	°C/W
3	28				°C/W

FIGURE 7 – STEADY-STATE THERMAL RESISTANCE

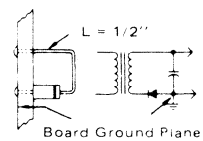


Mounting Method 1
P.C. Board where available copper surface is small.

Mounting Method 2
Vector Push-In Terminals T-28

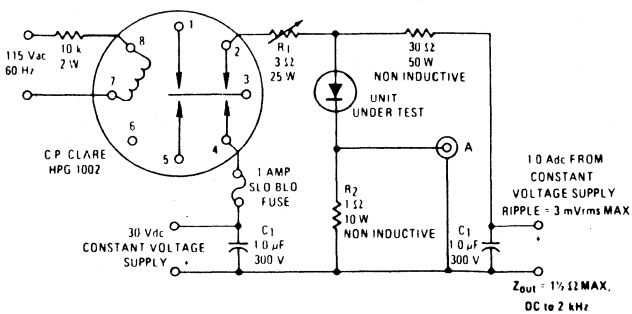


Mounting Method 3
P.C. Board with with 2-1/2" X 2-1/2" copper surface.



DYNAMIC CHARACTERISTICS

FIGURE 8 – REVERSE RECOVERY CIRCUIT



MINIMIZE ALL LEAD LENGTHS

A – TEKTRONIX 545A, K PLUG IN PRE AMP, P6000 PROBE OR EQUIVALENT

R_1 – ADJUSTED FOR 1.4 Ω BETWEEN POINT 2 OF RELAY AND RECTIFIER INDUCTANCE ≈ 38 μH

R_2 – TEN 1 W, 10 Ω, 1% CARBON CORE IN PARALLEL

T_A = 25 $^{+10}_{-0}$ °C FOR RECTIFIER

7

RECOVERY STORED CHARGE

FIGURE 9 – T_J = 25°C

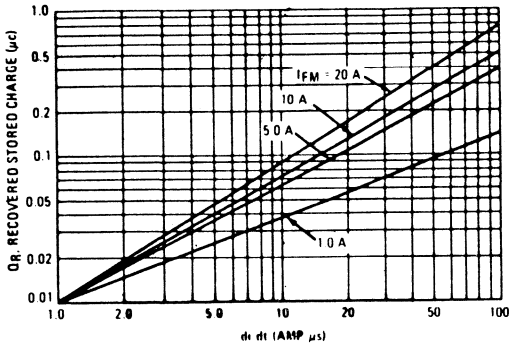
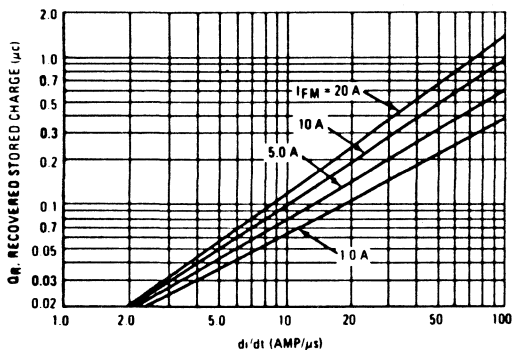


FIGURE 10 – T_J = 150°C



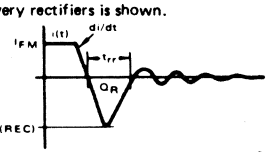
NOTE 3

Reverse recovery time is the period which elapses from the time that the current, thru a previously forward biased rectifier diode, passers thru zero going negatively until the reverse current recovers to a point which is less than 10% peak reverse current.

Reverse recovery time is a direct function of the forward current prior to the application of reverse voltage.

For any given rectifier, recovery time is very circuit dependent. In order to cover all circuit conditions, curves are given for typical recovered stored charge versus commutation di/dt for various levels of forward current and for junction temperatures of 25°C and 150°C.

To use these curses, it is necessary to know the forward current level just before commutation, the circuit commutation di/dt, and the operating junction temperature. The reverse recovery test current waveform for all Motorola fast recovery rectifiers is shown.



From stored charge curves versus di/dt, recovery time (t_{rr}) and peak reverse recovery current ($I_{RM(REC)}$) can be closely approximated using the following formulas:

$$t_{rr} = 1.41 \times \left[\frac{Q_R}{di/dt}\right]^{1/2}$$

$$I_{RM(REC)} = 1.41 \times [Q_R \times di/dt]^{1/2}$$

FIGURE 11 – FORWARD RECOVERY TIME

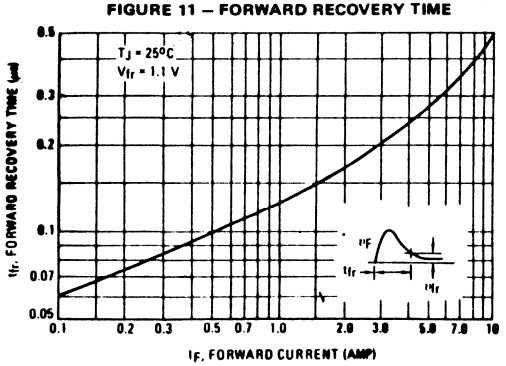
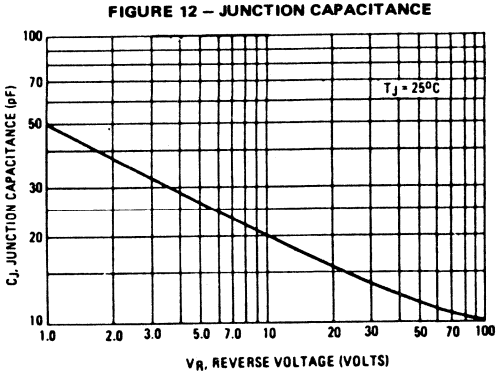


FIGURE 12 – JUNCTION CAPACITANCE



BY 396 SERIES

FAST RECOVERY POWER RECTIFIERS

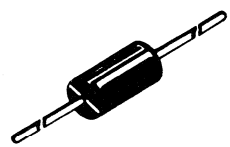
100–800 VOLTS
3,0 AMPERES

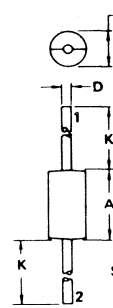
SUBMINIATURE SIZE, AXIAL LEAD MOUNTED FAST RECOVERY POWER RECTIFIERS

. . . designed for special applications such as dc power supplies, inverters, converters, ultrasonic systems, choppers, low RF interference and free wheeling diodes. A complete line of fast recovery rectifiers having typical recovery time of 100 nanoseconds providing high efficiency at frequencies to 250 kHz.

Designer's Data for "Worst Case" Conditions

The Designers Data sheets permit the design of most circuits entirely from the information presented. Limit curves – representing boundaries on device characteristics – are given to facilitate "worst case" design.





STYLE 1:
PIN 1. CATHODE
2. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.65	0.370	0.380
B	4.83	5.33	0.190	0.210
D	1.22	1.32	0.048	0.052
K	26.97	27.23	1.062	1.072

CASE 267-01

MAXIMUM RATINGS

Rating	Symbol	BY396	BY397	BY398	BY399	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	100	200	400	800	Volts
Non-Repetitive Peak Reverse Voltage	V_{RSM}	200	300	500	1000	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	70	140	280	560	Volts
Average Rectified Forward Current (Single phase resistive load, T_A = 90°C) (1)	I_O	3.0				Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions)	I_{FSM}	100 (one cycle)				Amp
Operating and Storage Junction Temperature Range (2)	T_J,T_{stg}	-65 to +175				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient (Recommended Printed Circuit Board Mouting, See Note 6, Page 8)	$R_{\theta JA}$	28	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Instantaneous Forward Voltage (I_F = 9.4 Amp, T_J = 175°C)	v_F	–	0.9	1.1	Volts
Forward Voltage (I_F = 3.0 Amp, T_J = 25°C)	V_F	–	1.04	1.25	Volts
Reverse Current (rated dc voltage) T_J = 25°C	I_R	–	2.0	10	μA
T_J = 100°C				300	

REVERSE RECOVERY CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Recovery Time (I_F = 1.0 Amp to V_R = 30 Vdc, Figure 25) (I_F = 10 mA, I_{RR} = 10 mA, 1 mA)	t_{rr}	– –	100 150	200 400	ns
Reverse Recovery Current (I_F = 1.0 Amp to V_R = 30 Vdc, Figure 25)	$I_{RM(REC)}$	–	–	2.0	Amp

(1) Must be derated for reverse power dissipation. See Note 2.
(2) Derate as shown in Figure 1

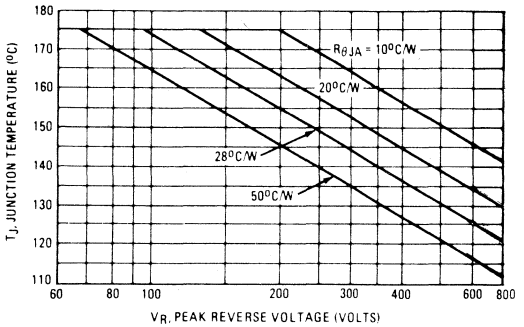
MECHANICAL CHARACTERISTICS

Case: Void Free, Transfer Molded
Finish: External Leads are Plated, Leads are readily Solderable
Polarity: Indicated by Cathode Band
Weight: 1.1 Grams (Approximately)
Maximum Lead Temperature for Soldering Purposes:
240°C, 1/8" from case for 10 s at 5.0 lb. tension

7

MAXIMUM CURRENT AND TEMPERATURE RATINGS

FIGURE 1 – MAXIMUM ALLOWABLE JUNCTION TEMPERATURE



NOTE 1
MAXIMUM JUNCTION TEMPERATURE DERATING

When operating this rectifier at junction temperatures over 120°C, reverse power dissipation and the possibility of thermal runaway must be considered. The data of Figure 1 is based upon worst case reverse power and should be used to derate $T_{J(max)}$ from its maximum value of 175°C. See Note 2 for additional information on derating for reverse power dissipation.

When current ratings are computed from $T_{J(max)}$ and reverse power dissipation is also included, ratings vary with reverse voltage as shown on Figures 2 thru 5.

RESISTIVE LOAD RATINGS

Printed Circuit Board Mounting – See Note 6, Page 8

FIGURE 2 – SINE WAVE INPUT

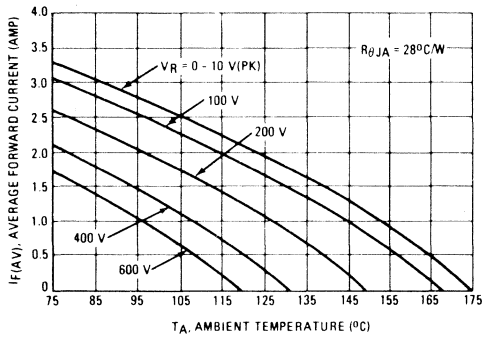


FIGURE 3 – SQUARE WAVE INPUT

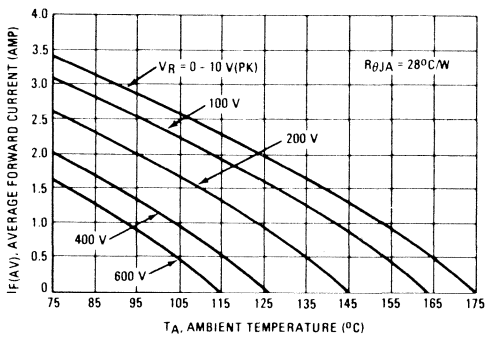


FIGURE 4 – SINE WAVE INPUT

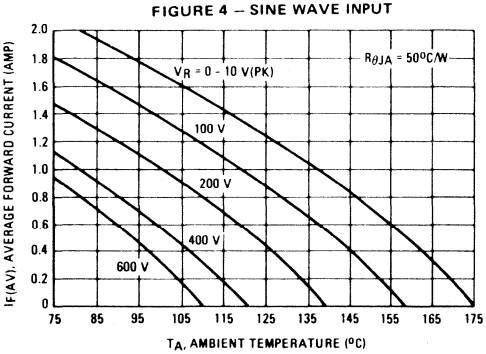
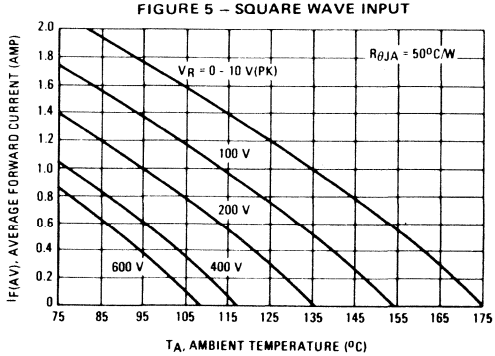


FIGURE 5 – SQUARE WAVE INPUT



MAXIMUM CURRENT RATINGS

Current derating data is based upon the thermal response data of Figure 29 and the forward power dissipation data of Figures 19 and 20. Since reverse power dissipation is not considered in Figures 6 thru 11, additional derating for reverse voltage and for junction to ambient thermal resistance must be applied. See Note 2.

SINE WAVE INPUTS

FIGURE 6 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

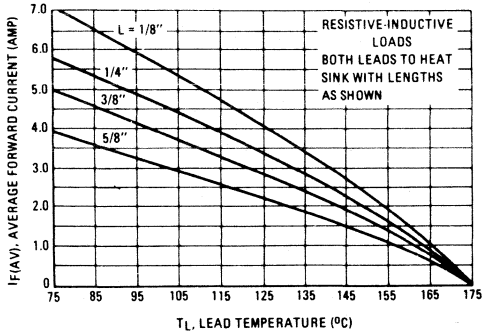


FIGURE 8 – 1/8" LEAD LENGTH, VARIOUS LOADS

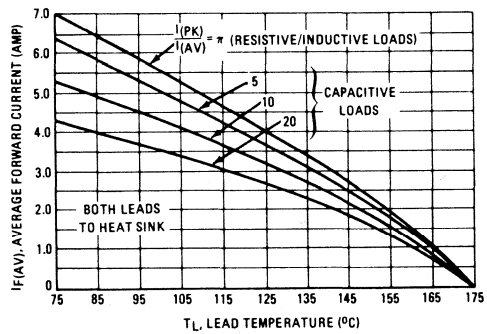
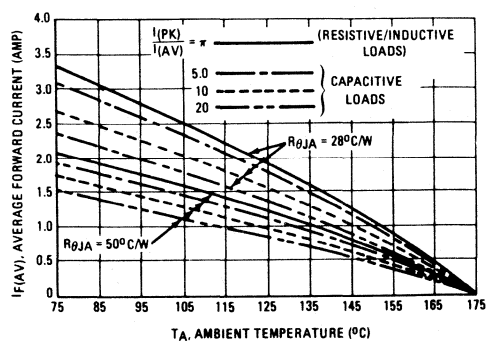


FIGURE 10 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS



SQUARE WAVE INPUTS

FIGURE 7 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

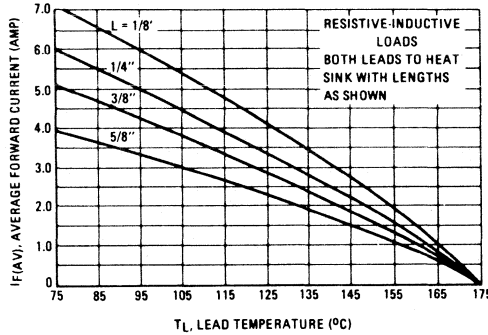


FIGURE 9 – 1/8" LEAD LENGTH, VARIOUS LOADS

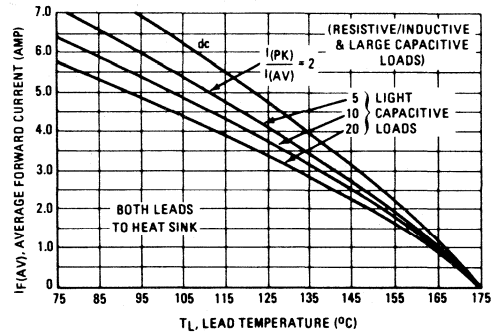
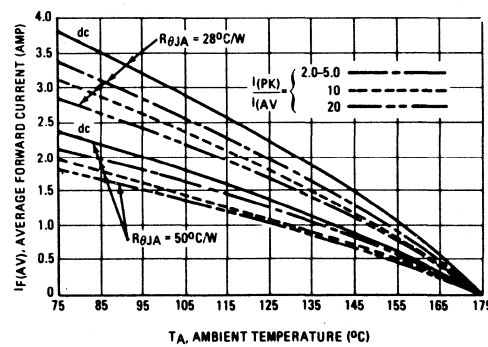


FIGURE 11 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS



7

REVERSE POWER DISSIPATION AND CURRENT

NOTE 2
DERATING FOR REVERSE POWER DISSIPATION

In this rectifier, power loss due to reverse current is generally not negligible. For reliable circuit design, the maximum junction temperature must be limited to either 175°C or the temperature which results in thermal runaway. Proper derating may be accomplished by use of equation 1 or equation 2.

Equation 1 $T_A = T_1 - (175 - T_{J(max)}) - P_R R_{\theta JA}$

Where: T_1 = Maximum Allowable Ambient Temperature neglecting reverse power dissipation (from Figures 10 or 11)

$T_{J(max)}$ = Maximum Allowable Junction Temperature to prevent thermal runaway or 175°C, which ever is lower. (See Figure 1).

P_R = Reverse Power Dissipation (From Figure 12 or 13, adjusted for $T_{J(max)}$ as shown below)

$R_{\theta JA}$ = Thermal Resistance, Junction to Ambient.

When thermal resistance, junction to ambient, is over 20°C/W, the effect of thermal response is negligible. Satisfactory derating may be found by using:

Equation 2 $T_A = T_{J(max)} - (P_R + P_F) R_{\theta JA}$

P_F = Forward Power Dissipation (See Figures 19 & 20)

Other terms defined above.

The reverse power given on Figures 12 and 13 is calculated for T_J = 150°C. When T_J is lower, P_R will decrease; its value can be found by multiplying P_R by the normalized reverse current from Figure 14 at the temperature of interest.

The reverse power data is calculated for half wave rectification circuits. For full wave rectification using either a bridge or a center-tapped transformer, the data for resistive loads is equivalent when V_P is the line to line voltage across the rectifiers. For capacitive loads, it is recommended that the dc case on Figure 13 be used, regardless of input waveform, for bridge circuits. For capacitively loaded full wave center-tapped circuits, the 20:1 data of Figure 12 should be used for sine wave inputs and the capacitive load data of Figure 13 should be used for square wave inputs regardless of $I_{(pk)}/I_{(av)}$. For these two cases, V_P is the voltage across one leg of the transformer.

Example 1 Find maximum ambient temperature for I_{AV} = 2 A, capacitive load of I_{PK}/I_{AV} = 20, Input Voltage = 60 V (rms), sine wave, $R_{\theta JA}$ = 28°C/W, half wave circuit.

Solution 1 (using Equation 1)

Step 1: Find V_P; $V_P = \sqrt{2}\, V_{in}$ = 85 V, $V_{R(pk)}$ = 170

Step 2: Find $T_{J(max)}$ from Figure 1. Read $T_{J(max)}$ = 157°C

Step 3: Find $P_{R(max)}$ from Figure 12. Read P_R = 360 mW @ 150°C

Step 4: Find I_R normalized from Figure 14. Read $I_{R(norm)}$ = 1.5

Step 5: Correct P_R to $T_{J(max)}$. $P_R = I_{R(norm)} \times P_R$ (Figure 12) P_R = 1.5 x 360 = 540 mW

Step 6: Find $T_A = T_1$ from Figure 10. Read T_1 = 94°C

Step 7: Compute T_A from $T_A = T_1 - (175 - T_{J(max)}) - P_R R_{\theta JA}$
$T_A = 94 - (175 - 157) - (0.54)(28)$
T_A = 61°C

Solution 2 (using Equation 2)

Steps 1 thru 5 are as Solution 1

Step 6: Find P_F from Figure 19. Read P_F = 3.0 W

Step 7: Compute T_A from $T_A = T_{J(max)} - (P_R + P_F) R_{\theta JA}$
$T_A = 157 - (0.54 + 3)28$
T_A = 58°C

The discrepancy occurs because thermal response is factored into solution 1, and advantage is taken of the cooling time after the power pulse and before reverse voltage achieves its maximum. 61°C is a satisfactory ambient temperature.

FIGURE 12 – REVERSE POWER DISSIPATION, SINE WAVE

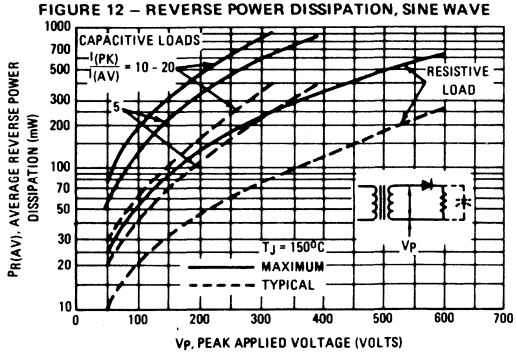


FIGURE 13 – REVERSE POWER DISSIPATION, SQUARE WAVE

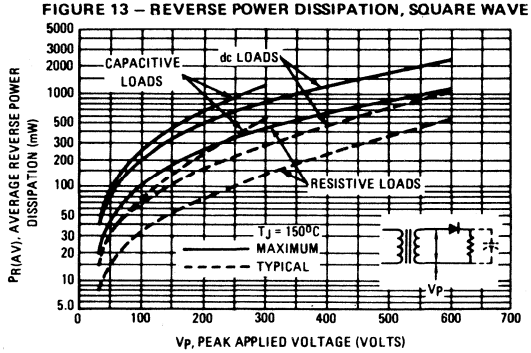


FIGURE 14 – NORMALIZED REVERSE CURRENT

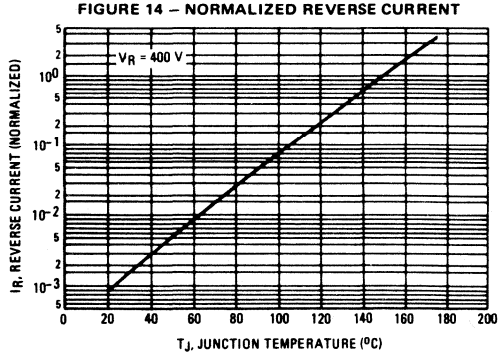
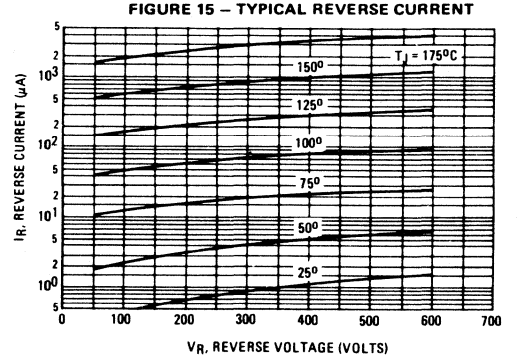


FIGURE 15 – TYPICAL REVERSE CURRENT



STATIC CHARACTERISTICS

FIGURE 16 – FORWARD VOLTAGE

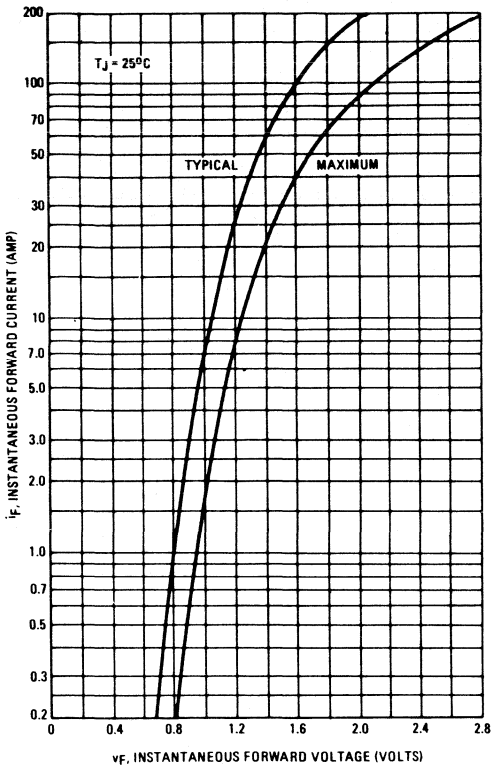


FIGURE 17 – MAXIMUM SURGE CAPABILITY

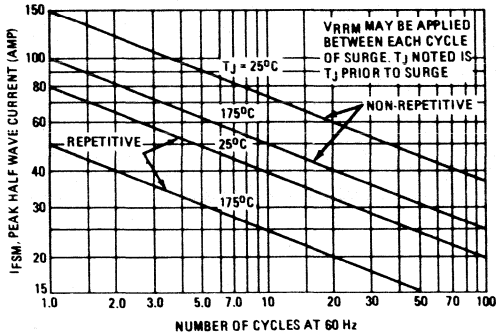
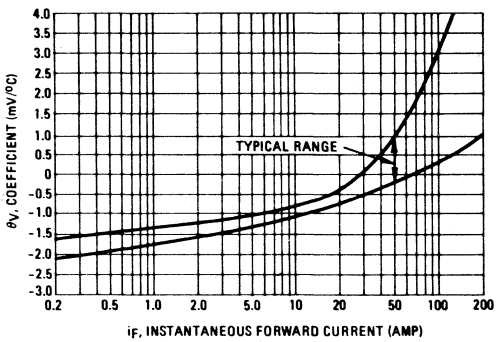
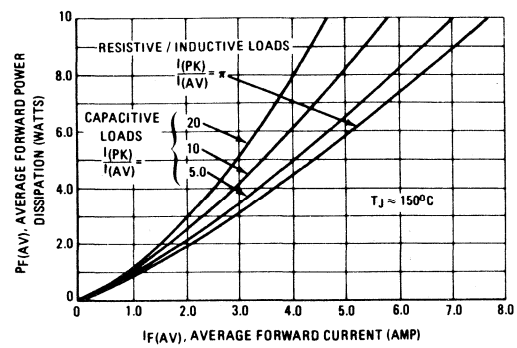


FIGURE 18 – FORWARD VOLTAGE TEMPERATURE COEFFICIENT



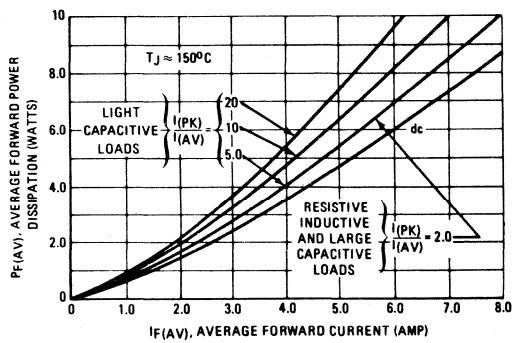
SINE WAVE INPUT

FIGURE 19 – FORWARD POWER DISSIPATION



SQUARE WAVE INPUT

FIGURE 20 – FORWARD POWER DISSIPATION



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TYPICAL RECOVERED STORED CHARAGE DATA

FIGURE 21 – T_J = 25°C (See Note 3)

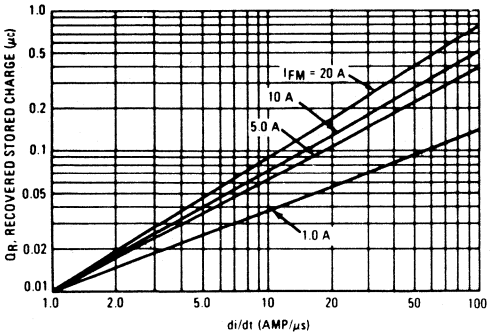


FIGURE 22 – T_J = 75°C

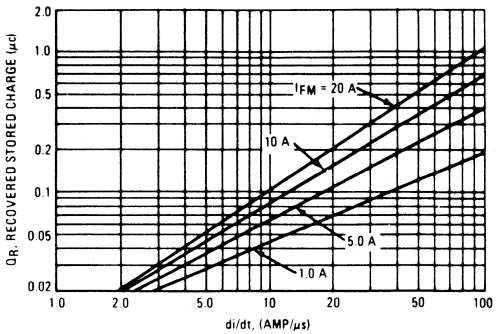


FIGURE 23 – T_J = 100°C

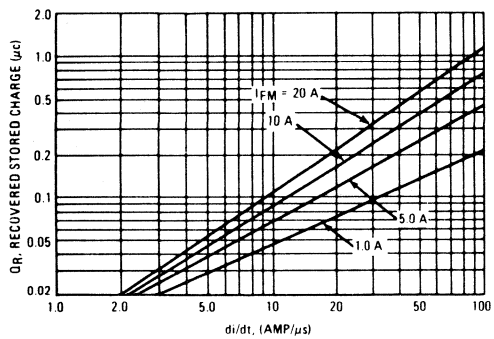
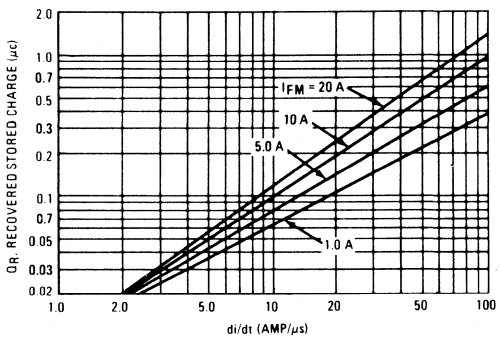


FIGURE 24 – T_J = 150°C



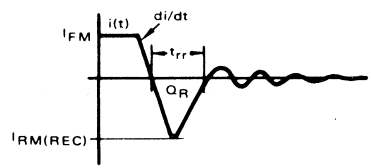
NOTE 3

Reverse recovery time is the period which elapses from the time that the current, thru a previously forward biased rectifier diode, passes thru zero going negatively until the reverse current recovers to a point which is less than 10% peak reverse current.

Reverse recovery time is a direct function of the forward current prior to the application of reverse voltage.

For any given rectifier, recovery time is very circuit dependent. Typical and maximum recovery time of all Motorola fast recovery power rectifiers are rated under a fixed set of conditions using I_F = 1.0 A, V_R = 30 V. In order to cover all circuit conditions, curves are given for typical recovered stored charge versus commutation di/dt for various levels of forward current and for junction temperatures of 25°C, 75°C, 100°C, and 150°C.

To use these curves, it is necessary to know the forward current level just before commutation, the circuit commutation di/dt, and the operating junction temperature. The reverse recovery test current waveform for all Motorola fast recovery rectifiers is shown.



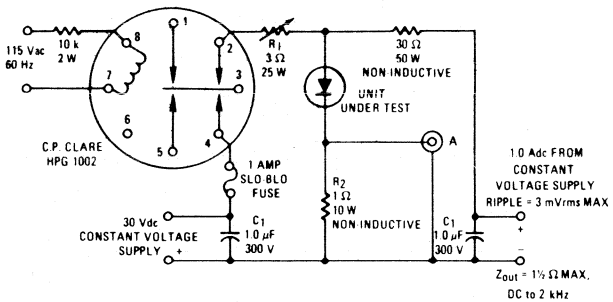
From stored charge curves versus di/dt, recovery time (t_{rr}) and peak reverse recovery current ($I_{RM(REC)}$) can be closely approximated using the following formulas:

$$t_{rr} = 1.41 \times \left[\frac{Q_R}{di/dt}\right]^{1/2}$$

$$I_{RM(REC)} = 1.41 \times \left[Q_R \times di/dt\right]^{1/2}$$

DYNAMIC CHARACTERISTICS

FIGURE 25 – REVERSE RECOVERY CIRCUIT



MINIMIZE ALL LEAD LENGTHS

A – TEKTRONIX 545A, K PLUG IN PRE-AMP, P6000 PROBE OR EQUIVALENT

R_1 – ADJUSTED FOR 1.4 Ω BETWEEN POINT 2 OF RELAY AND RECTIFIER INDUCTANCE ≈ 38 μH

R_2 – TEN 1 W, 10 Ω, 1% CARBON CORE IN PARALLEL

$T_A = 25^{+10}_{-0}$°C FOR RECTIFIER

FIGURE 26 – FORWARD RECOVERY TIME

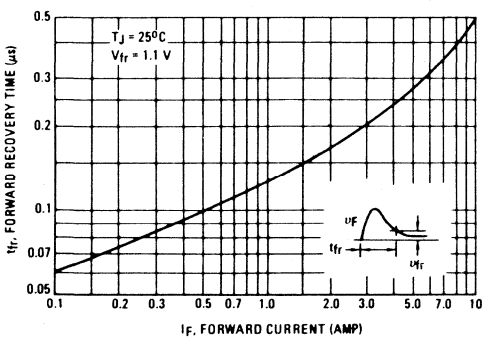


FIGURE 27 – JUNCTION CAPACITANCE

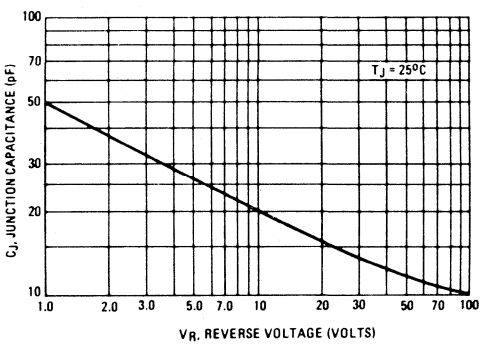


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FIGURE 28 – THERMAL RESPONSE

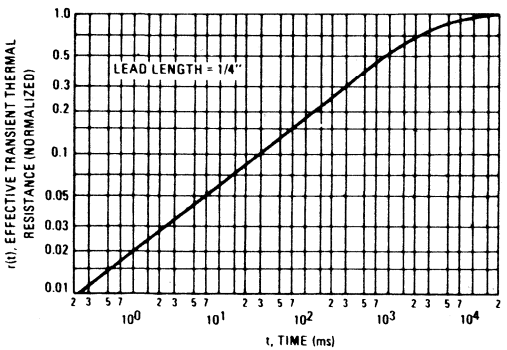
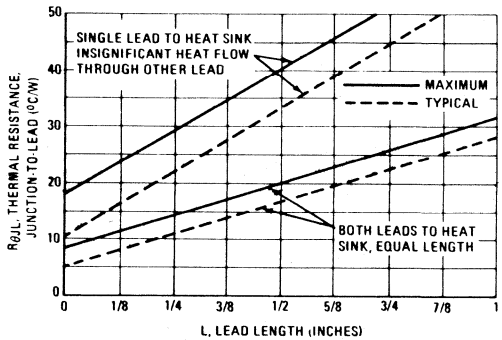


FIGURE 29 – STEADY-STATE THERMAL RESISTANCE



NOTE 4

To determine maximum junction temperature of the diode in a given situation, the following procedure is recommended:

The temperature of the lead should be measured using a thermocouple placed on the lead as close as possible to the tie point. The thermal mass connected to the tie point is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady state conditions are achieved. Using the measured value of T_L, the junction temperature may be determined by:

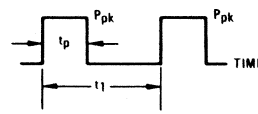
$$T_J = T_L + \Delta T_{JL}$$

where ΔT_{JL} is the increase in junction temperature above the lead temperature. It may be determined by:

$$\Delta T_{JL} = P_{pk} \cdot R_{\theta JL} [D + (1 - D) \cdot r(t_1 + t_p) + r(t_p) - r(t_1)]$$

where r(t) = normalized value of transient thermal resistance at time t from Figure 28, i.e.:

$r(t_1 + t_p)$ = normalized value of transient thermal resistance at time $t_1 + t_p$.



DUTY CYCLE = t_p/t_1

PEAK POWER, P_{pk}, is peak of an equivalent square power pulse.

NOTE 5

Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heat sink. Terms in the model signify:

T_A = Ambient Temperature
T_L = Lead Temperature
T_C = Case Temperature
T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_D = Total Power Dissipation = $P_F + P_R$
P_F = Forward Power Dissipation
P_R = Reverse Power Dissipation

(Subscripts A and K refer to anode and cathode sides respectively.) Values for thermal resistance components are:

$R_{\theta L}$ = 46°C/W/IN. Typically and 48°C/W/IN Maximum.
$R_{\theta J}$ = 10°C/W Typically and 16°C/W Maximum.

The maximum lead temperature may be found as follows:

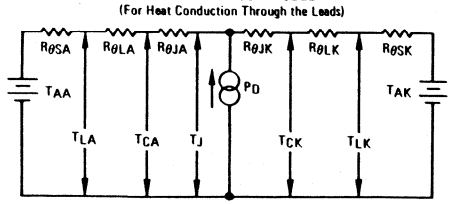
$$T_L = T_{J(max)} - \Delta T_{JL}$$

where

ΔT_{JL} can be approximated as follows:

$\Delta T_{JL} \approx R_{\theta JL} \cdot P_D$; P_D is the sum of forward and reverse power dissipation shown in Figures 2 and 4 for sine wave operation and Figures 3 and 5 for square wave operation.

THERMAL CIRCUIT MODEL
(For Heat Conduction Through the Leads)



NOTE 6

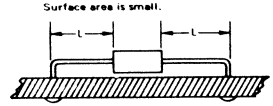
Data shown for thermal resistance junction-to-ambient ($R_{\theta JA}$) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

TYPICAL VALUES FOR $R_{\theta JA}$ IN STILL AIR

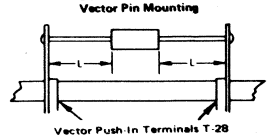
MOUNTING METHOD	LEAD LENGTH, L (IN)				$R_{\theta JA}$
	1/8	1/4	1/2	3/4	
1	50	51	53	55	°C/W
2	58	59	61	63	°C/W
3	28				°C/W

MOUNTING METHOD 1

P.C. Board Where Available Copper Surface area is small.

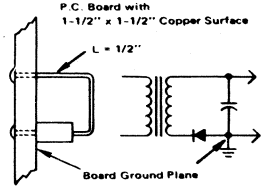


MOUNTING METHOD 2
Vector Pin Mounting



MOUNTING METHOD 3

P.C. Board with 1-1/2" x 1-1/2" Copper Surface



BY 406/407

SUBMINIATURE SIZE, AXIAL LEAD MOUNTED FAST RECOVERY POWER RECTIFIERS

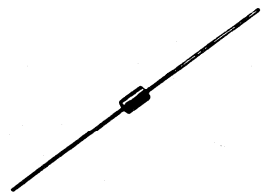
. . . designed for special applications such as dc power supplies, inverters, converters, ultrasonic systems, choppers, low RF interference and free wheeling diodes. A complete line of fast recovery rectifiers having typical recovery time of 200 nanoseconds providing high efficiency at frequencies to 250 Hz.

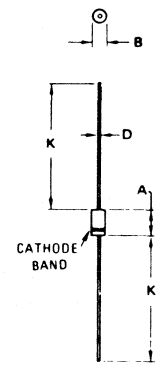
DESIGNER'S DATA FOR „WORST CASE" CONDITIONS

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit curves – representing device characteristic boundaries – are given to facilitate „worst case" design.

FAST RECOVERY POWER RECTIFIERS

350/600 VOLTS
0.8 AMPERE





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94	–	1.100	–

CASE 59-04

MAXIMUM RATINGS

Ratings	Symbol	BY 406	BY 407	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage	V_{RWM} V_{RRM}	350	600	Volts
DC Blocking Voltage	V_R	300	500	Volts
Average Rectified Forward Current (Single phase, resistive load, T_A = 75° C)	$I_{F(AV)}$	0,8		Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions) (T_A = 75° C)	I_{FSM}	20		Amps
Operating Junction Temp. Range	T_J	–65 to +150		°C
Storage Temperature Range	T_{stg}	–65 to +175		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max.	Unit
Thermal Resistance, Junction to Ambient (Typical Printed Circuit Board Mounting)	$R_{\theta JA}$	65	°C/W

ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Forward Voltage (I_F = 2,0 Amp. T_A = 25 Grad C)	V_F	–	1,1	1,55	Volts
Reverse Current (rated dc voltage) T_A = 25° C T_A = 125° C	I_R	– –	1,0 –	2,0 125	µA

REVERSE RECOVERY CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Reverse Recovery Time (I_F = 10 mA to V_R = 50 V	t_{rr}	–	150	300	ns

MECHANICAL CHARACTERISTICS

CASE: Void Free, Transfer Molded

FINISH: External leads are tin plated, leads are readily solderable

POLARITY: Cathode indicated by Polarity band

WEIGHT: 0.4 Grams (Approximately)

7

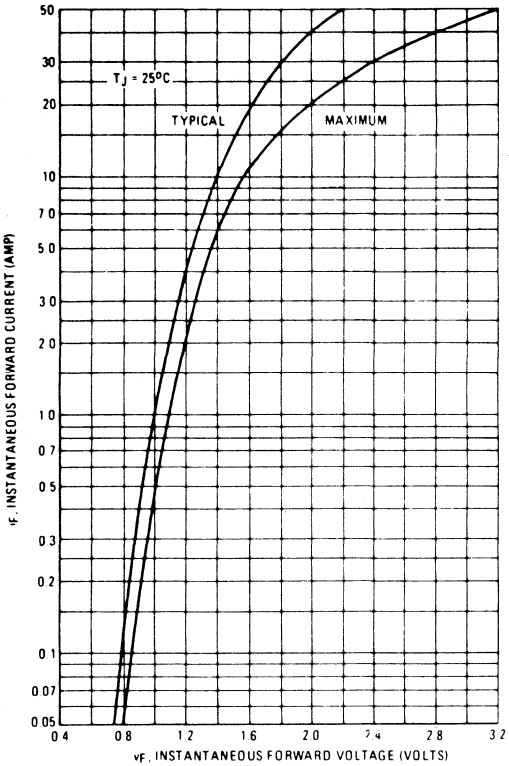


FIGURE 1 – FORWARD VOLTAGE

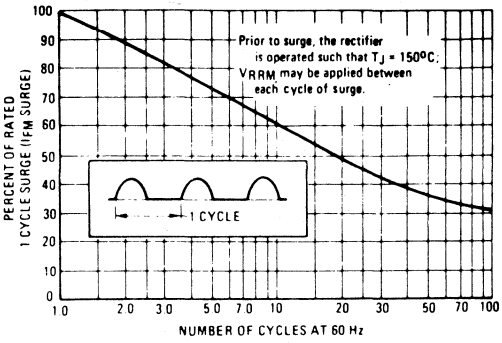


FIGURE 2 – MAXIMUM SURGE CAPABILITY

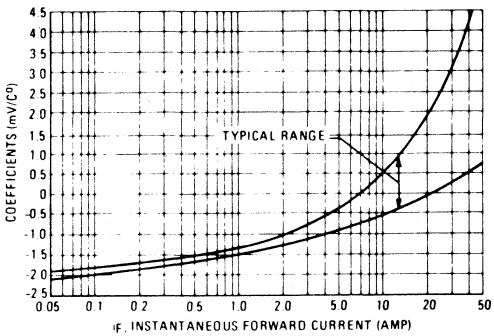


FIGURE 3 – TEMPERATURE COEFFICIENT

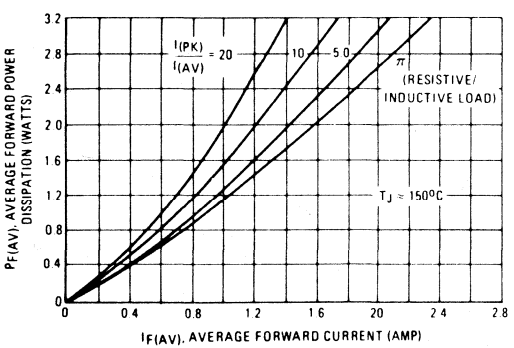


FIGURE 4 – FORWARD POWER DISSIPATION

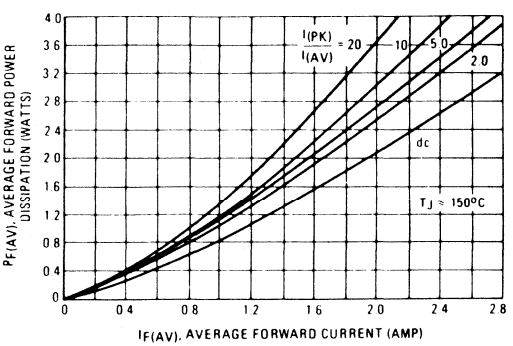


FIGURE 5 – FORWARD POWER DISSIPATION

MAXIMUM CURRENT RATINGS
(SEE NOTES 1 and 2)

SINE WAVE INPUT

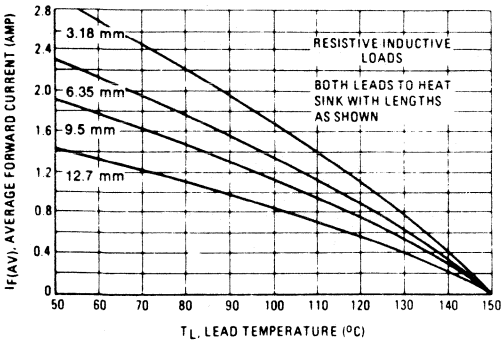


FIGURE 6 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

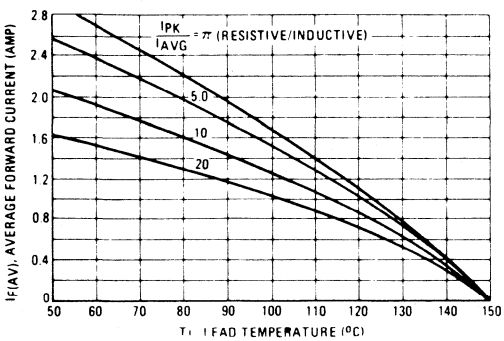


FIGURE 8 — 3.18 mm LEAD LENGTH, VARIOUS LOADS

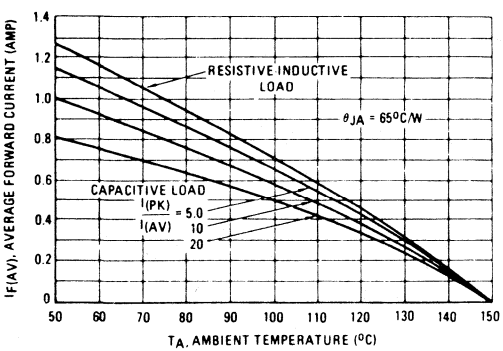


FIGURE 10 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS

SQUARE WAVE INPUT

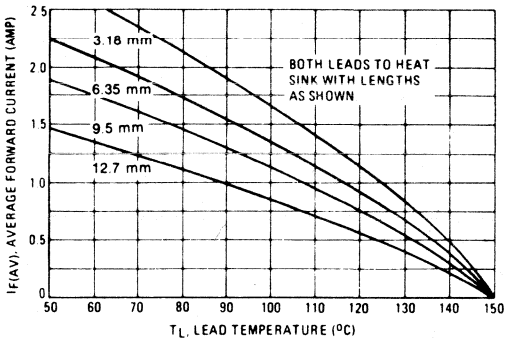


FIGURE 7 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

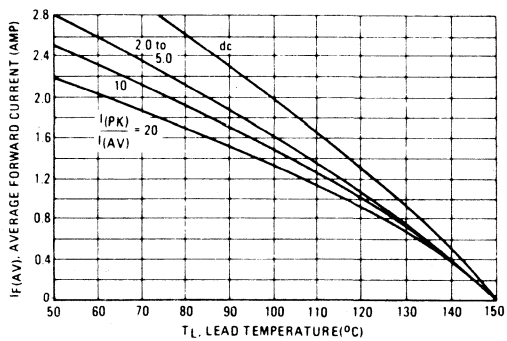


FIGURE 9 — 3.18 mm LEAD LENGTH, VARIOUS LOADS

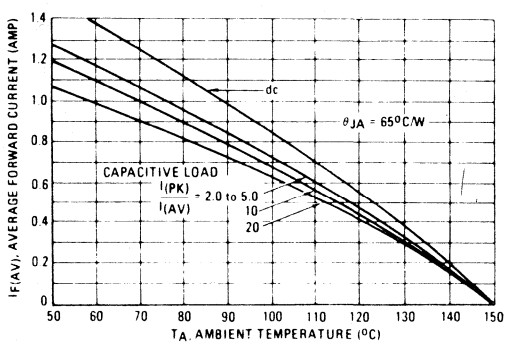


FIGURE 11 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS

7

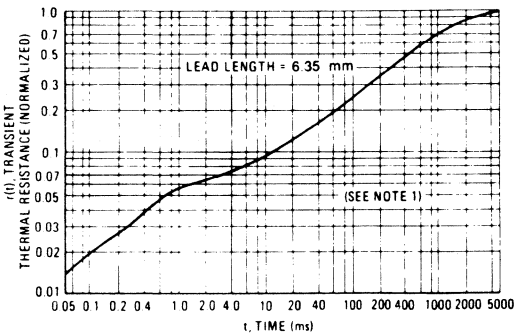


FIGURE 12 – THERMAL RESPONSE

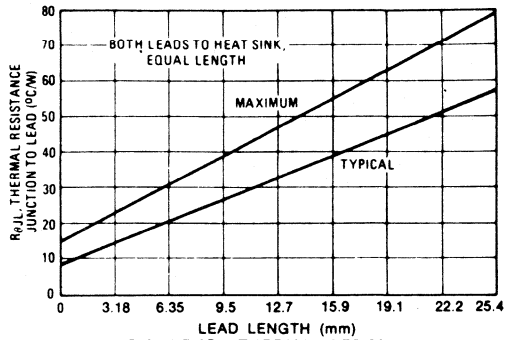
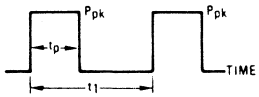


FIGURE 13 – THERMAL RESISTANCE

NOTE 1



DUTY CYCLE, $D = t_p/t_1$
PEAK POWER, P_{pk}, is peak of an equivalent square power pulse.

To determine maximum junction temperature of the diode in a given situation, the following procedure is recommended:

The temperature of the case should be measured using a thermocouple placed on the case as close as possible to the tie point. The thermal mass connected to the tie point is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady-state conditions are achieved. Using the measured value of T_C, the junction temperature may be determined by:

$$T_J = T_C + \triangle T_{JC}$$

where $\triangle T_{JC}$ is the increase in junction temperature above the case temperature. It may be determined by:

$$\triangle T_{JC} = P_{pk} \cdot R_{\theta JC}\left[D + (1 - D) \cdot r(t_1 + t_p) + r(t_p) - r(t_1)\right]$$

where

$r(t)$ = normalized value of transient thermal resistance at time, t, from Figure 12, i.e.:

$r(t_1 + t_p)$ = normalized value of transient thermal resistance at time $t_1 + t_p$.

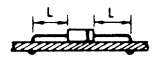
NOTE 2

Data shown for thermal resistance junction-to-ambient (θ_{JA}) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

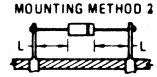
TYPICAL VALUES FOR θ_{JA} IN STILL AIR

MOUNTING METHOD	LEAD LENGTH, L(mm) 3.81	6.35	12.7	19.1	$R_{\theta JA}$
1	65	72	82	92	°C/W
2	74	81	91	101	°C/W
3	40				°C/W

MOUNTING METHOD 1

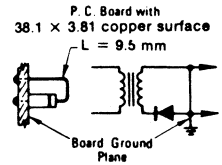


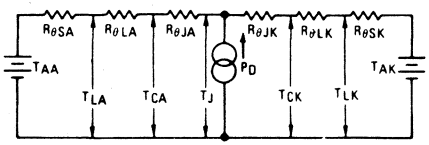
MOUNTING METHOD 2



Vector pin mounting

MOUNTING METHOD 3





Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heat sink. Terms in the model signify:

T_A = Ambient Temperature
T_L = Lead Temperature
T_C = Case Temperature
T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_D = Power Dissipation

(Subscripts A and K refer to anode and cathode sides respectively.)

Values for thermal resistance components are:

$R_{\theta L}$ = 112°C/W/IN. Typically and 128°C/W/IN Maximum

$R_{\theta J}$ = 18°C/W Typically and 30°C/W Maximum

The maximum lead temperature may be calculated as follows:

$T_L = 150° - \triangle T_{JL}$

$\triangle T_{JL}$ can be calculated as shown in NOTE 1 or it may be approximated as follows:

$\triangle T_{JL} \approx R_{\theta JL} \cdot P_F$; P_F may be formulated for sine-wave operation from Figure 3 or from Figure 4 for square-wave operation.

FIGURE 14 – THERMAL CIRCUIT MODEL

TYPICAL DYNAMIC CHARACTERISTICS

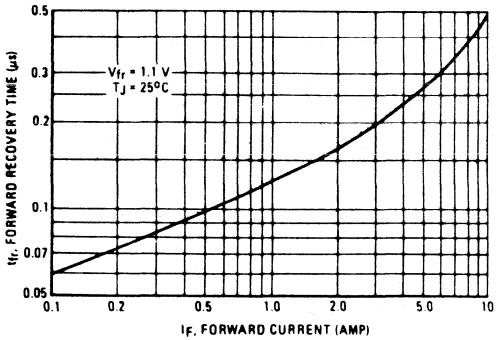


FIGURE 15 – FORWARD RECOVERY TIME

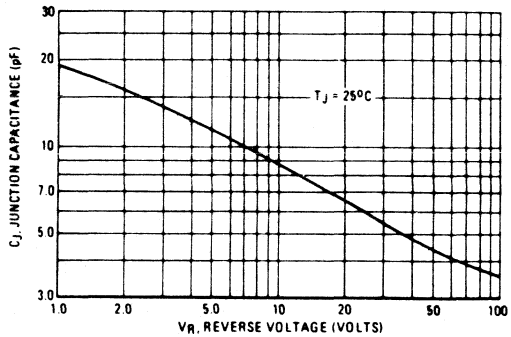


FIGURE 16 – JUNCTION CAPACITANCE

TYPICAL RECOVERED STORED CHARGE DATA
(SEE NOTE 3)

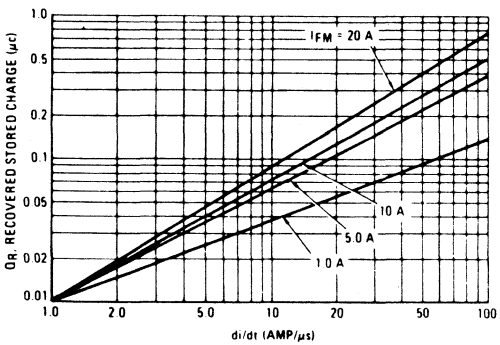


FIGURE 17 – T_J = 25°C

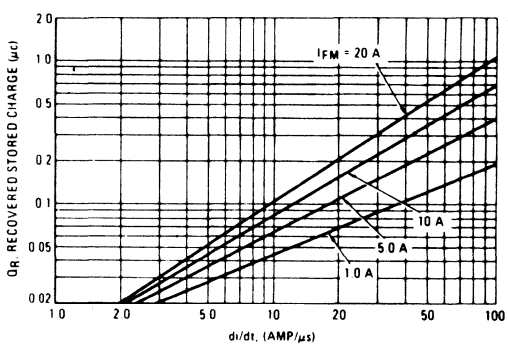


FIGURE 18 – T_J = 75°C

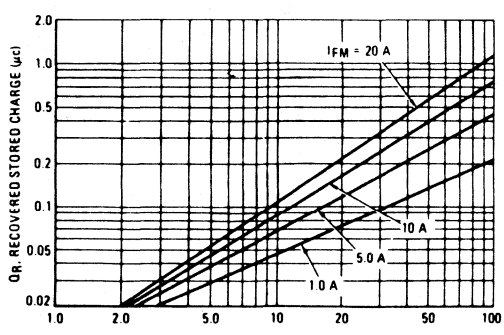


FIGURE 19 – T_J = 100°C

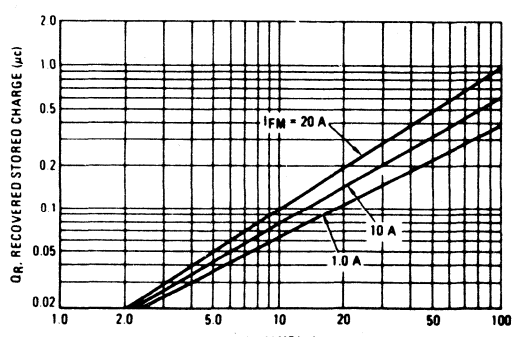


FIGURE 20 – T_J = 150°C

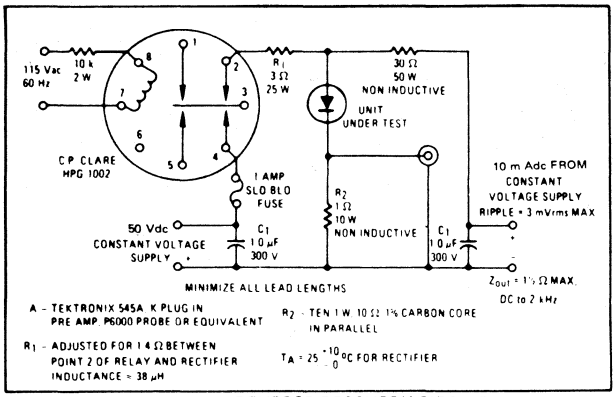


FIGURE 21 – REVERSE RECOVERY CIRCUIT

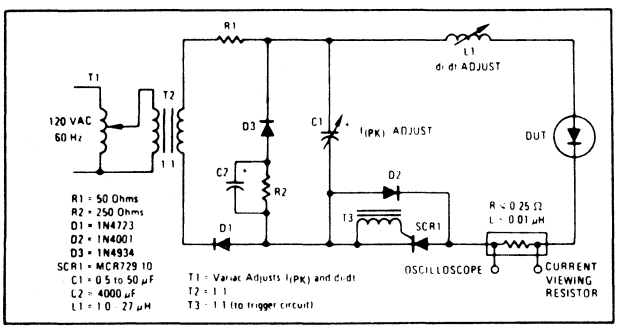


FIGURE 22 – JEDEC REVERSE RECOVERY CIRCUIT

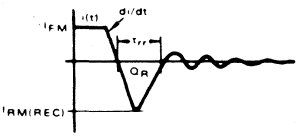
NOTE 3

Reverse recovery time is the period which elapses from the time that the current, thru a previously forward biased rectifier diode, passes thru zero going negatively until the reverse current recovers to a point which is less than 10% peak reverse current.

Reverse recovery time is a direct function of the forward current prior to the application of reverse voltage.

For any given rectifier, recovery time is very circuit dependent. Typical and maximum recovery time of all Motorola fast recovery power rectifiers are rated under a fixed set of conditions using IF = 10 mA VR = 50 VR. In order to cover all circuit conditions, curves are given for typical recovered stored charge versus commutation di/dt for various levels of forward current and for junction temperatures of 25°C, 75°C, 100°C, and 150°C.

To use these curves, it is necessary to know the forward current level just before commutation, the circuit commutation di/dt, and the operating junction temperature. The reverse recovery test current waveform for all Motorola fast recovery rectifiers is shown.



From stored charge curves versus di/dt, recovery time (t_{rr}) and peak reverse recovery current ($I_{RM(REC)}$) can be closely approximated using the following formulas:

$$t_{rr} = 1.41 \times \left[\frac{Q_R}{di/dt}\right]^{1/2}$$

$$I_{RM(REC)} = 1.41 \times \left[Q_R \times di/dt\right]^{1/2}$$

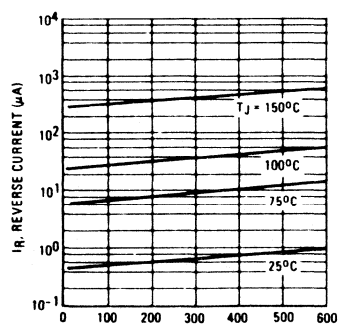


FIGURE 23 – TYPICAL REVERSE LEAKAGE

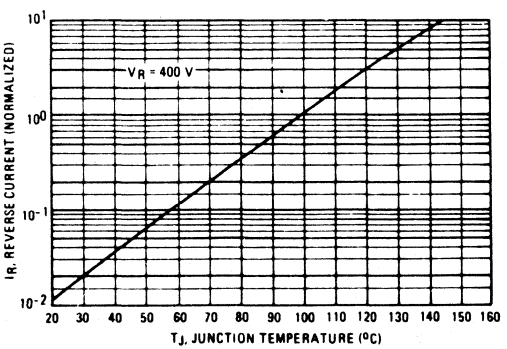


FIGURE 24 – TYPICAL REVERSE LEAKAGE

BY 500 SERIES

FAST RECOVERY POWER RECTIFIERS

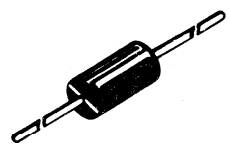
100–600 VOLTS
5 AMPERES

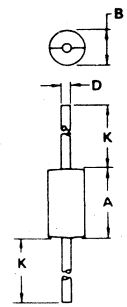
SUBMINIATURE SIZE, AXIAL LEAD MOUNTED FAST RECOVERY POWER RECTIFIERS

. . . designed for special applications such as dc power supplies, inverters, converters, ultrasonic systems, choppers, low RF interference and free wheeling diodes. A complete line of fast recovery rectifiers having typical recovery time of 100 nanoseconds providing high efficiency at frequencies to 250 kHz.

Designer's Data for "Worst Case" Conditions

The Designers Data sheets permit the design of most circuits entirely from the information presented. Limit curves – representing boundaries on device characteristics – are given to facilitate "worst case" design.





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.65	0.370	0.380
B	4.83	5.33	0.190	0.210
D	1.22	1.32	0.048	0.052
K	26.97	27.23	1.062	1.072

CASE 267-01

MAXIMUM RATINGS

Rating	Symbol	BY 500–100	BY 500–200	BY 500–400	BY 500–600	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	100	200	400	600	Volts
Non-Repetitive Peak Reverse Voltage	V_{RSM}	150	250	450	650	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	70	140	280	420	Volts
Average Rectified Forward Current (Single phase resistive load, T_A = 25° C) (1)	I_O	5.0				Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions)	I_{FSM}	200 (one cycle)				Amp
Operating and Storage Junction Temperature Range (2)	T_J, T_{stg}	-65 to +175				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient (Recommended Printed Circuit Board Mouting, See Note 6, Page 8)	$R_{\theta JA}$	28	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Forward Voltage (I_F = 3.0 Amp, T_J = 25°C)	V_F	–	1.04	1.25	Volts
Reverse Current (rated dc voltage) T_J = 25°C	I_R	–	2.0	10	μA
T_J = 100°C				300	

REVERSE RECOVERY CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Recovery Time (I_F = 1.0 Amp to V_R = 30 Vdc, Figure 25) (I_F = 15 Amp, di/dt = 10 A/μs, Figure 26)	t_{rr}	– –	100 150	200 300	ns
Reverse Recovery Current (I_F = 1.0 Amp to V_R = 30 Vdc, Figure 25)	$I_{RM(REC)}$	–	–	2.0	Amp

(1) Must be derated for reverse power dissipation. See Note 2, Page 3.
(2) Derate as shown in Figure 1

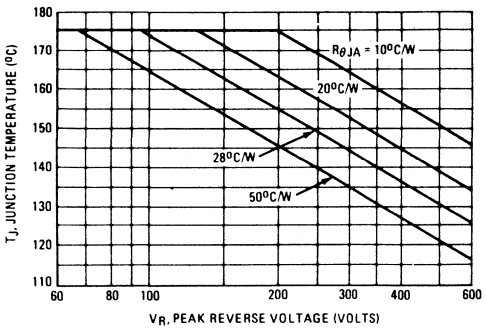
MECHANICAL CHARACTERISTICS

Case: Void Free, Transfer Molded
Finish: External Leads are Plated, Leads are readily Solderable
Polarity: Indicated by Cathode Band
Weight: 1.1 Grams (Approximately)
Maximum Lead Temperature for Soldering Purposes:
240°C, 1/8" from case for 10 s at 5.0 lb. tension

7

MAXIMUM CURRENT AND TEMPERATURE RATINGS

FIGURE 1 – MAXIMUM ALLOWABLE JUNCTION TEMPERATURE



NOTE 1
MAXIMUM JUNCTION TEMPERATURE DERATING

When operating this rectifier at junction temperatures over 120°C, reverse power dissipation and the possibility of thermal runaway must be considered. The data of Figure 1 is based upon worst case reverse power and should be used to derate $T_{J(max)}$ from its maximum value of 175°C. See Note 2 for additional information on derating for reverse power dissipation.

When current ratings are computed from $T_{J(max)}$ and reverse power dissipation is also included, ratings vary with reverse voltage as shown on Figures 2 thru 5.

RESISTIVE LOAD RATINGS

Printed Circuit Board Mounting – See Note 6, Page 8

FIGURE 2 – SINE WAVE INPUT

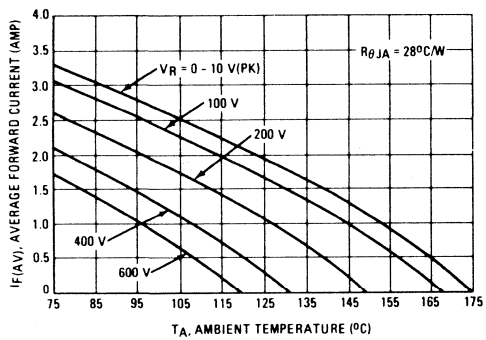


FIGURE 3 – SQUARE WAVE INPUT

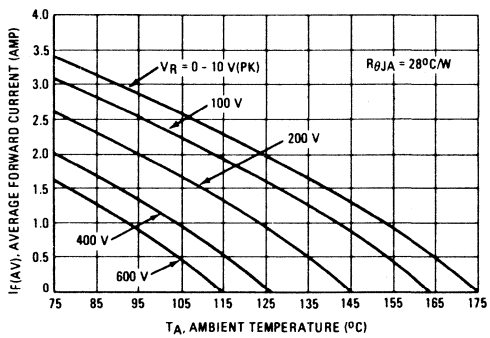


FIGURE 4 – SINE WAVE INPUT

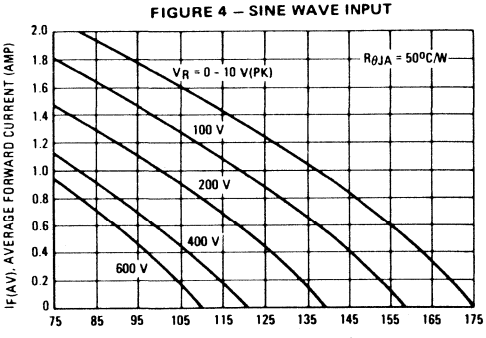
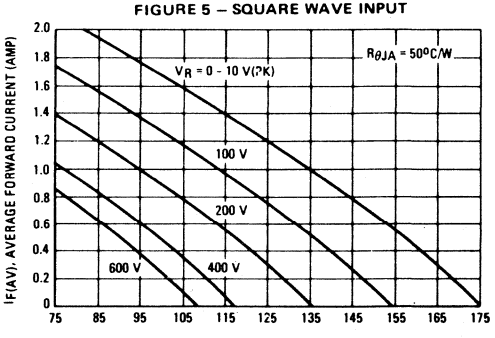


FIGURE 5 – SQUARE WAVE INPUT



MAXIMUM CURRENT RATINGS

Current derating data is based upon the thermal response data of Figure 29 and the forward power dissipation data of Figures 19 and 20. Since reverse power dissipation is not considered in Figures 6 thru 11, additional derating for reverse voltage and for junction to ambient thermal resistance must be applied. See Note 2.

SINE WAVE INPUTS

FIGURE 6 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

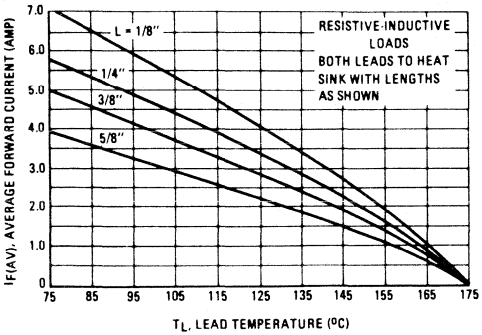


FIGURE 8 – 1/8" LEAD LENGTH, VARIOUS LOADS

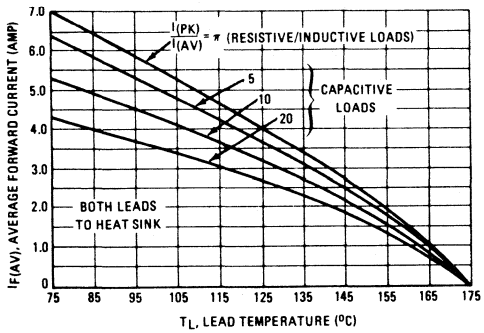
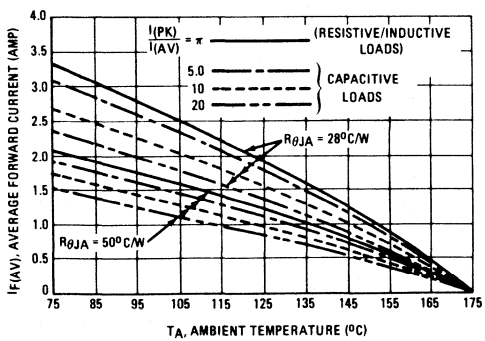


FIGURE 10 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS



SQUARE WAVE INPUTS

FIGURE 7 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

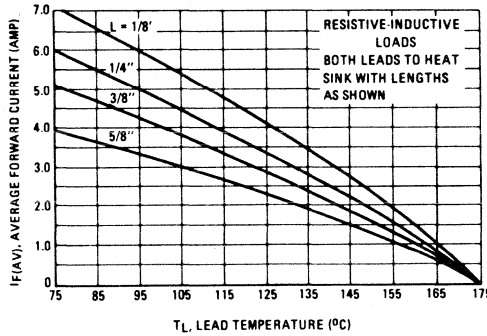


FIGURE 9 – 1/8" LEAD LENGTH, VARIOUS LOADS

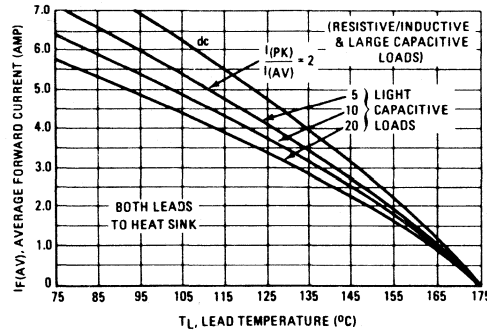
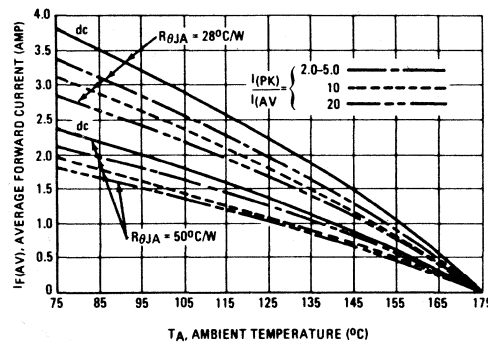


FIGURE 11 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS



7

REVERSE POWER DISSIPATION AND CURRENT

NOTE 2
DERATING FOR REVERSE POWER DISSIPATION

In this rectifier, power loss due to reverse current is generally not negligible. For reliable circuit design, the maximum junction temperature must be limited to either 175°C or the temperature which results in thermal runaway. Proper derating may be accomplished by use of equation 1 or equation 2.

Equation 1 $T_A = T_1 - (175 - T_{J(max)}) - P_R R_{\theta JA}$

Where: T_1 = Maximum Allowable Ambient Temperature neglecting reverse power dissipation (from Figures 10 or 11)

$T_{J(max)}$ = Maximum Allowable Junction Temperature to prevent thermal runaway or 175°C, which ever is lower. (See Figure 1).

P_R = Reverse Power Dissipation (From Figure 12 or 13, adjusted for $T_{J(max)}$ as shown below)

$R_{\theta JA}$ = Thermal Resistance, Junction to Ambient.

When thermal resistance, junction to ambient, is over 20°C/W, the effect of thermal response is negligible. Satisfactory derating may be found by using:

Equation 2 $T_A = T_{J(max)} - (P_R + P_F) R_{\theta JA}$

P_F = Forward Power Dissipation (See Figures 19 & 20)

Other terms defined above.

The reverse power given on Figures 12 and 13 is calculated for $T_J = 150°C$. When T_J is lower, P_R will decrease; its value can be found by multiplying P_R by the normalized reverse current from Figure 14 at the temperature of interest.

The reverse power data is calculated for half wave rectification circuits. For full wave rectification using either a bridge or a center-tapped transformer, the data for resistive loads is equivalent when Vp is the line to line voltage across the rectifiers. For capacitive loads, it is recommended that the dc case on Figure 13 be used, regardless of input waveform, for bridge circuits. For capacitively loaded full wave center-tapped circuits, the 20:1 data of Figure 12 should be used for sine wave inputs and the capacitive load data of Figure 13 should be used for square wave inputs regardless of $I_{(pk)}/I_{(av)}$. For these two cases, Vp is the voltage across one leg of the transformer.

Example 1 Find maximum ambient temperature for I_{AV} = 2 A, capacitive load of I_{PK}/I_{AV} = 20, Input Voltage = 60 V (rms), sine wave, $R_{\theta JA}$ = 28°C/W, half wave circuit.

Solution 1 (using Equation 1)

Step 1: Find V_P; $V_P = \sqrt{2}\, V_{in} = 85$ V, $V_{R(pk)} = 170$

Step 2: Find $T_{J(max)}$ from Figure 1. Read $T_{J(max)} = 157°C$

Step 3: Find $P_{R(max)}$ from Figure 12. Read P_R = 360 mW @ 150°C

Step 4: Find I_R normalized from Figure 14. Read $I_{R(norm)} = 1.5$

Step 5: Correct P_R to $T_{J(max)}$. $P_R = I_{R(norm)} \times P_R$ (Figure 12) $P_R = 1.5 \times 360 = 540$ mW

Step 6: Find $T_A = T_1$ from Figure 10. Read $T_1 = 94°C$

Step 7: Compute T_A from $T_A = T_1 - (175 - T_{J(max)} - P_R R_{\theta JA}$
$T_A = 94 - (175 - 157) - (0.54)(28)$
$T_A = 61°C$

Solution 2 (using Equation 2)

Steps 1 thru 5 are as Solution 1

Step 6: Find P_F from Figure 19. Read P_F = 3.0 W

Step 7: Compute T_A from $T_A = T_{J(max)} - (P_R + P_F) R_{\theta JA}$
$T_A = 157 - (0.54 + 3)28$
$T_A = 58°C$

The discrepancy occurs because thermal response is factored into solution 1, and advantage is taken of the cooling time after the power pulse and before reverse voltage achieves its maximum. 61°C is a satisfactory ambient temperature.

FIGURE 12 – REVERSE POWER DISSIPATION, SINE WAVE

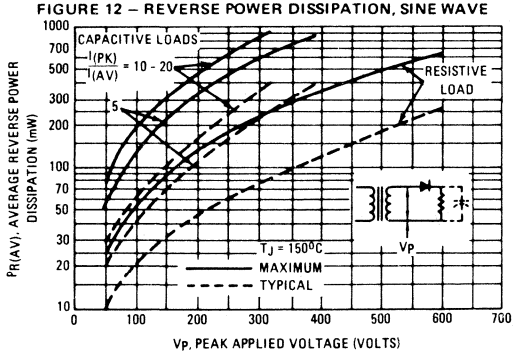


FIGURE 13 – REVERSE POWER DISSIPATION, SQUARE WAVE

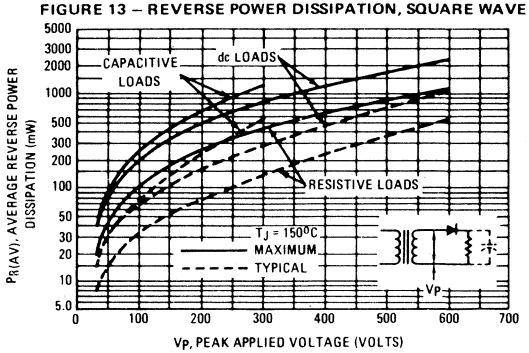


FIGURE 14 – NORMALIZED REVERSE CURRENT

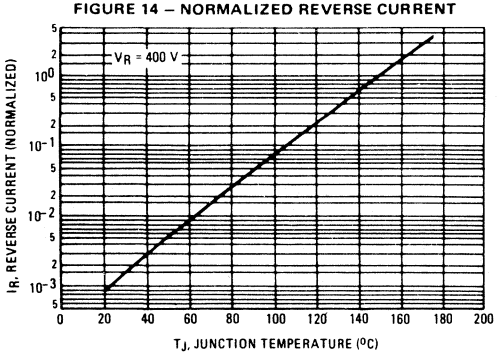
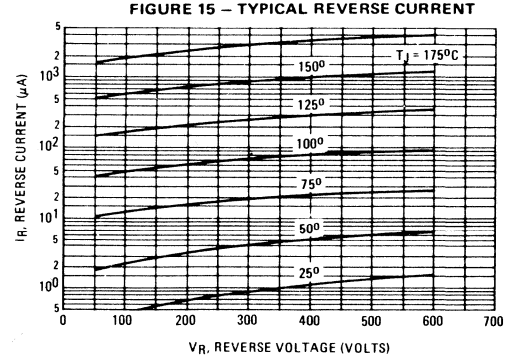


FIGURE 15 – TYPICAL REVERSE CURRENT



STATIC CHARACTERISTICS

FIGURE 16 – FORWARD VOLTAGE

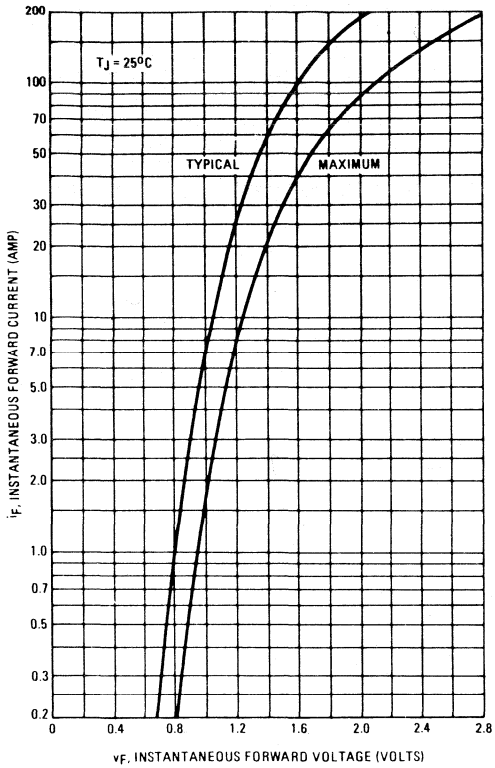


FIGURE 17–MAXIMUM NONREPETITIVE SURGE CURRENT

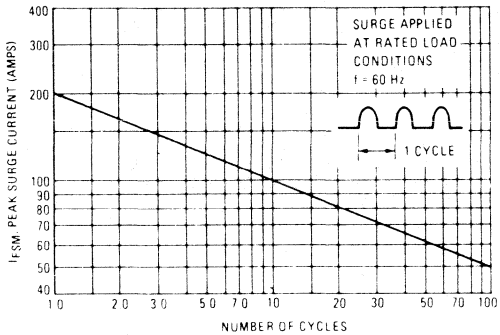
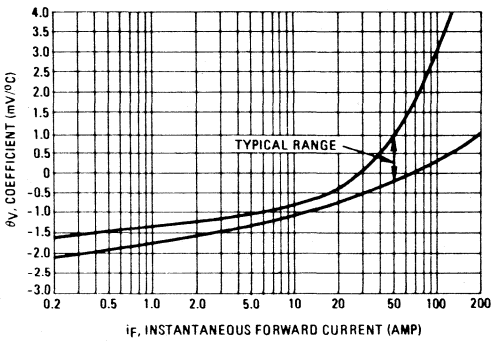
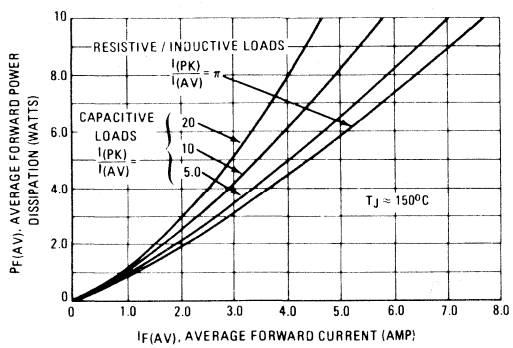


FIGURE 18 – FORWARD VOLTAGE TEMPERATURE COEFFICIENT



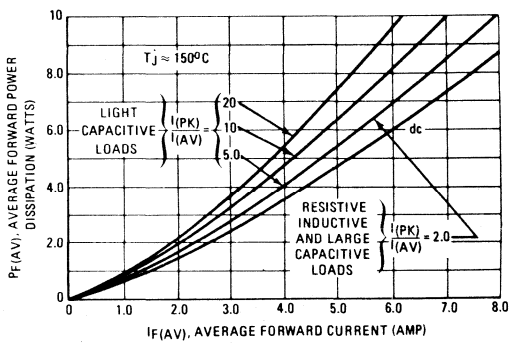
SINE WAVE INPUT

FIGURE 19 – FORWARD POWER DISSIPATION



SQUARE WAVE INPUT

FIGURE 20 – FORWARD POWER DISSIPATION



7

TYPICAL RECOVERED STORED CHARAGE DATA

(See Note 3)

FIGURE 21 – T_J = 25°C

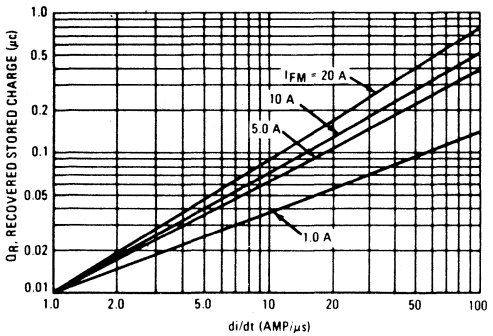


FIGURE 22 – T_J = 75°C

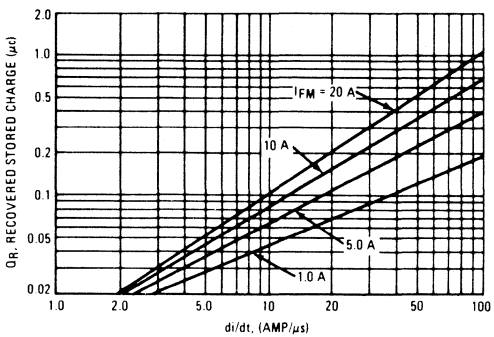


FIGURE 23 – T_J = 100°C

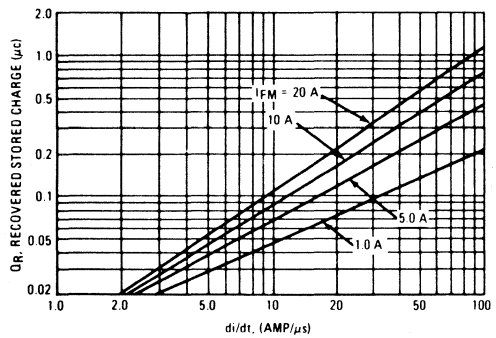
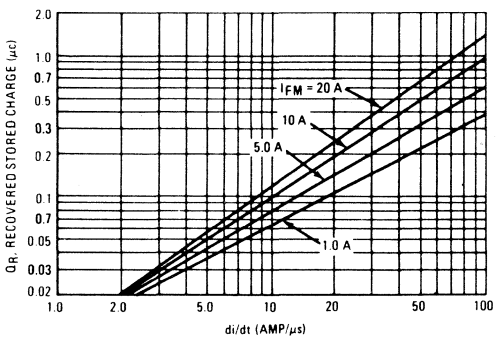


FIGURE 24 – T_J = 150°C



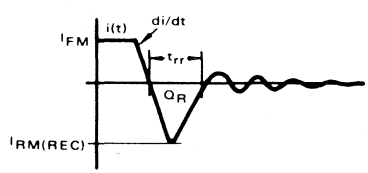
NOTE 3

Reverse recovery time is the period which elapses from the time that the current, thru a previously forward biased rectifier diode, passes thru zero going negatively until the reverse current recovers to a point which is less than 10% peak reverse current.

Reverse recovery time is a direct function of the forward current prior to the application of reverse voltage.

For any given rectifier, recovery time is very circuit dependent. Typical and maximum recovery time of all Motorola fast recovery power rectifiers are rated under a fixed set of conditions using I_F = 1.0 A, V_R = 30 V. In order to cover all circuit conditions, curves are given for typical recovered stored charge versus commutation di/dt for various levels of forward current and for junction temperatures of 25°C, 75°C, 100°C, and 150°C.

To use these curves, it is necessary to know the forward current level just before commutation, the circuit commutation di/dt, and the operating junction temperature. The reverse recovery test current waveform for all Motorola fast recovery rectifiers is shown.



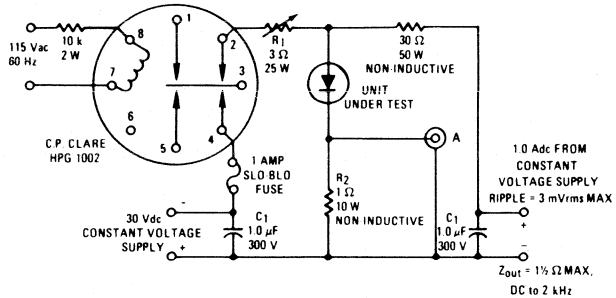
From stored charge curves versus di/dt, recovery time (t_{rr}) and peak reverse recovery current ($I_{RM(REC)}$) can be closely approximated using the following formulas:

$$t_{rr} = 1.41 \times \left[\frac{Q_R}{di/dt}\right]^{1/2}$$

$$I_{RM(REC)} = 1.41 \times \left[Q_R \times di/dt\right]^{1/2}$$

DYNAMIC CHARACTERISTICS

FIGURE 25 – REVERSE RECOVERY CIRCUIT



MINIMIZE ALL LEAD LENGTHS

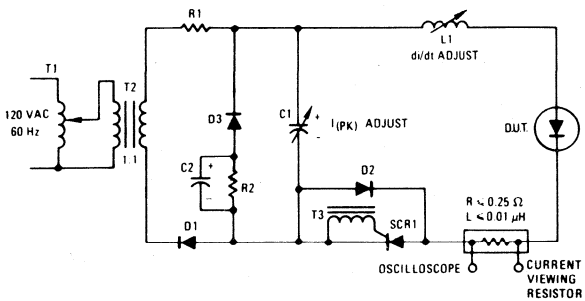
A – TEKTRONIX 545A, K PLUG IN PRE-AMP, P6000 PROBE OR EQUIVALENT

R_1 – ADJUSTED FOR 1.4 Ω BETWEEN POINT 2 OF RELAY AND RECTIFIER INDUCTANCE ≈ 38 μH

R_2 – TEN-1 W, 10 Ω, 1% CARBON CORE IN PARALLEL

$T_A = 25^{+10}_{-0}$ °C FOR RECTIFIER

FIGURE 26 – JEDEC REVERSE RECOVERY CIRCUIT



R1 = 50 Ohms
R2 = 250 Ohms
D1 = 1N4723
D2 = 1N4001
D3 = 1N4934
SCR1 = MCR729-10
C1 = 0.5 to 50 μF
C2 ≈ 4000 μF
L1 = 1.0 - 27 μH
T1 = Variac Adjusts $I_{(PK)}$ and di/dt
T2 = 1:1
T3 = 1:1 (to trigger circuit)

FIGURE 27 – FORWARD RECOVERY TIME

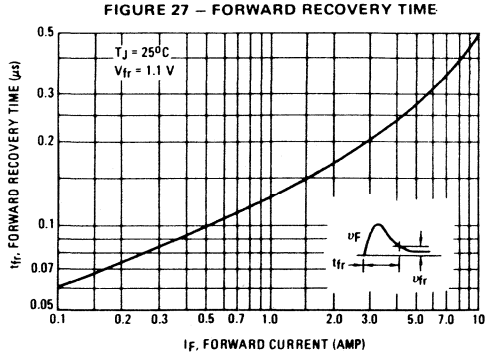


FIGURE 28 – JUNCTION CAPACITANCE

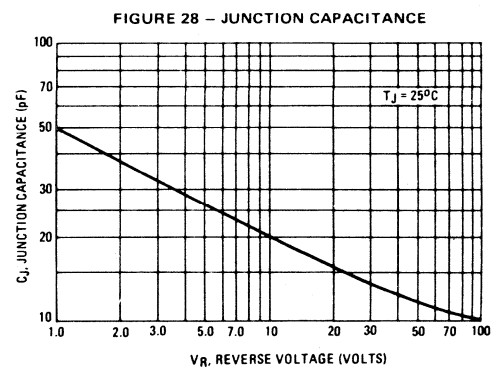


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FIGURE 29 – THERMAL RESPONSE

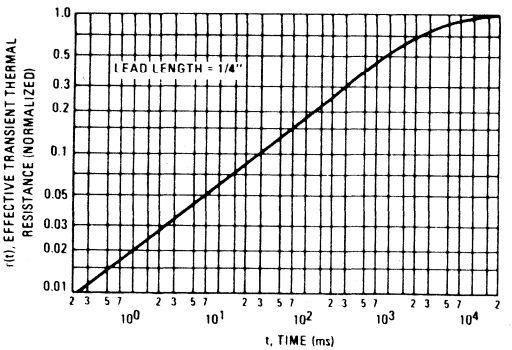
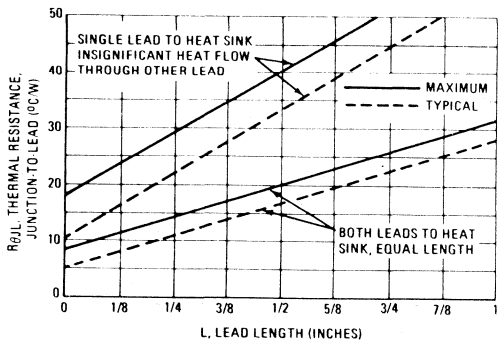


FIGURE 30 – STEADY-STATE THERMAL RESISTANCE



NOTE 4

To determine maximum junction temperature of the diode in a given situation, the following procedure is recommended.

The temperature of the lead should be measured using a thermocouple placed on the lead as close as possible to the tie point. The thermal mass connected to the tie point is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady state conditions are achieved. Using the measured value of T_L, the junction temperature may be determined by:

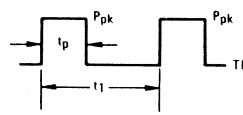
$$T_J = T_L + \Delta T_{JL}$$

where ΔT_{JL} is the increase in junction temperature above the lead temperature. It may be determined by:

$$\Delta T_{JL} = P_{pk} \cdot R_{\theta JL} [D + (1 - D) \cdot r(t_1 + t_p) + r(t_p) - r(t_1)]$$

where r(t) = normalized value of transient thermal resistance at time t from Figure 29, i.e.

$r(t_1 + t_p)$ = normalized value of transient thermal resistance at time $t_1 + t_p$.



DUTY CYCLE = t_p/t_1
PEAK POWER, P_{pk}, is peak of an equivalent square power pulse.

NOTE 5

Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heat sink. Terms in the model signify:

T_A = Ambient Temperature
T_L = Lead Temperature
T_C = Case Temperature
T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_D = Total Power Dissipation = $P_F + P_R$
P_F = Forward Power Dissipation
P_R = Reverse Power Dissipation

(Subscripts A and K refer to anode and cathode sides respectively.) Values for thermal resistance components are:

$R_{\theta L}$ = 46°C/W/IN. Typically and 48°C/W/IN Maximum.
$R_{\theta J}$ = 10°C/W Typically and 16°C/W Maximum.

The maximum lead temperature may be found as follows:

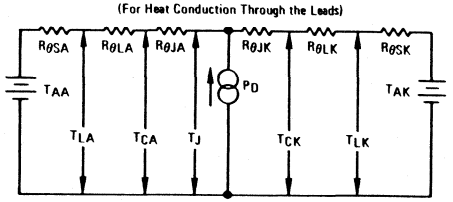
$$T_L = T_{J(max)} - \Delta T_{JL}$$

where

ΔT_{JL} can be approximated as follows:

$\Delta T_{JL} \approx R_{\theta JL} \cdot P_D$. P_D is the sum of forward and reverse power dissipation shown in Figures 2 and 4 for sine wave operation and Figures 3 and 5 for square wave operation.

THERMAL CIRCUIT MODEL
(For Heat Conduction Through the Leads)



NOTE 6

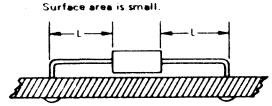
Data shown for thermal resistance junction-to-ambient ($R_{\theta JA}$) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

TYPICAL VALUES FOR $R_{\theta JA}$ IN STILL AIR

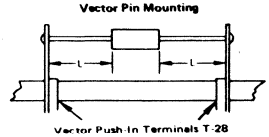
MOUNTING METHOD	LEAD LENGTH, L (IN)				$R_{\theta JA}$
	1/8	1/4	1/2	3/4	
1	50	51	53	55	°C/W
2	58	59	61	63	°C/W
3	28				°C/W

MOUNTING METHOD 1

P.C. Board Where Available Copper Surface area is small.

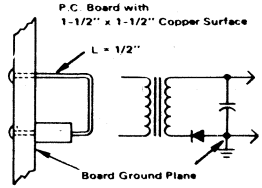


MOUNTING METHOD 2
Vector Pin Mounting



MOUNTING METHOD 3

P.C. Board with 1-1/2" x 1-1/2" Copper Surface



BY 601 thru BY 608 SERIES

"SURMETIC" RECTIFIERS

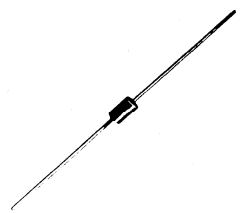
. . . subminiature size, axial lead mounted rectifiers for general-purpose main rectifier applications in TV/HiFi sets and domestic appliances.

Designers Data for "Worst Case" Conditions

The Designers Data Sheets permit the design of most circuits entirely from the information presented. Limit curves – representing boundaries on device characteristics – are given to facilitate "worst case" design.

LEAD MOUNTED SILICON RECTIFIERS

50–1250 VOLTS
DIFFUSED JUNCTION

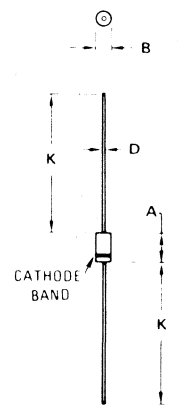


MAXIMUM RATINGS

Rating	Symbol	BY601	BY602	BY603	BY604	BY605	BY606	BY607	BY608	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	400	600	800	1000	1250	Volts
Non-Repetitive Peak Reverse Voltage (halfwave, single phase, 50 Hz)	V_{RSM}	60	120	240	480	720	1000	1200	1500	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	35	70	140	280	420	560	700	850	Volts
Average Rectified Forward Current (single phase, resistive load, 50 Hz, see Figure 8, T_A = 75 °C)	I_O	1.5								Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions, see Figure 2)	I_{FSM}	50 (for 1 cycle)								Amp
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +175								°C

ELECTRICAL CHARACTERISTICS

Characteristic and Conditions	Symbol	Typ	Max	Unit
Maximum Instantaneous Forward Voltage Drop (I_F = 1.5 Amp, T_J = 25 °C) Figure 1	V_F	1.0	1.15	Volts
Maximum Reverse Current (rated dc voltage) T_J = 25 °C T_J = 100 °C	I_R	0.05 1.0	10 50	μA



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94		1.100	

CASE 59-04
Does Not Conform to DO-41 Outline.

MECHANICAL CHARACTERISTICS

CASE: Void free, Transfer Molded.
MAXIMUM LEAD TEMPERATURE FOR SOLDERING PURPOSES: 350 °C, 1.27 cm from case for 10 seconds at 2.27 kg tension.
FINISH: All external surfaces are corrosion-resistant, leads are readily solderable.
POLARITY: Cathode indicated by color band.
WEIGHT: 0.40 Grams (approximately).

7

FIGURE 1 – FORWARD VOLTAGE

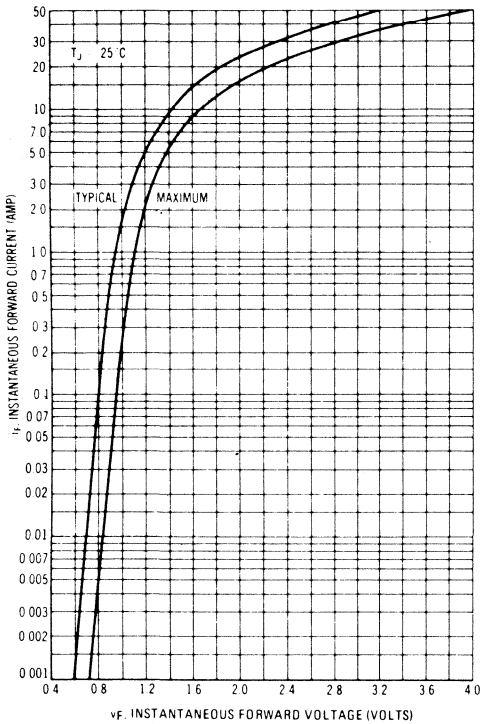


FIGURE 2 – NON REPETITIVE SURGE CAPABILITY

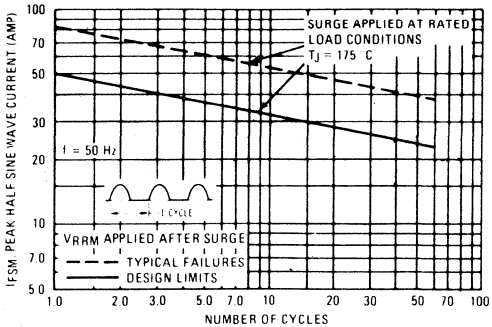


FIGURE 3 – FORWARD VOLTAGE TEMPERATURE COEFFICIENT

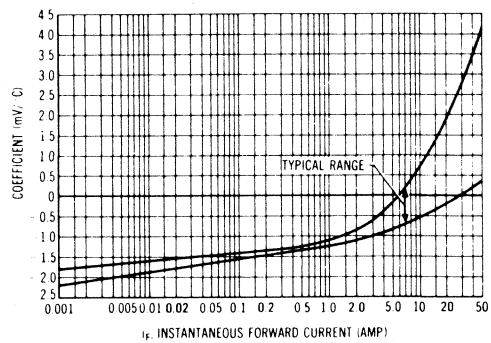
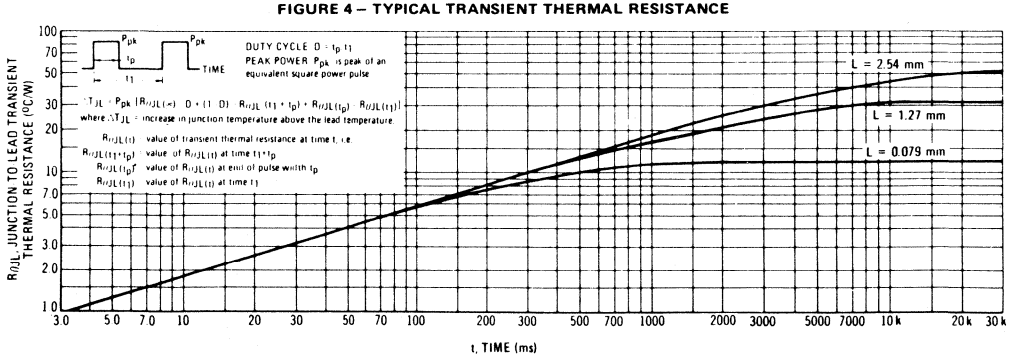


FIGURE 4 – TYPICAL TRANSIENT THERMAL RESISTANCE



The temperature of the lead should be measured using a thermocouple placed on the lead as close as possible to the tie point. The thermal mass connected to the tie point is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady-state conditions are achieved. Using the measured value of T_L, the junction temperature may be determined by:

$$T_J = T_L + \Delta T_{JL}.$$

CURRENT DERATING DATA

FIGURE 5 – FORWARD POWER DISSIPATION

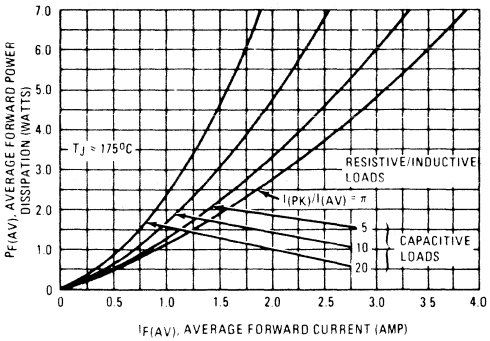


FIGURE 6 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

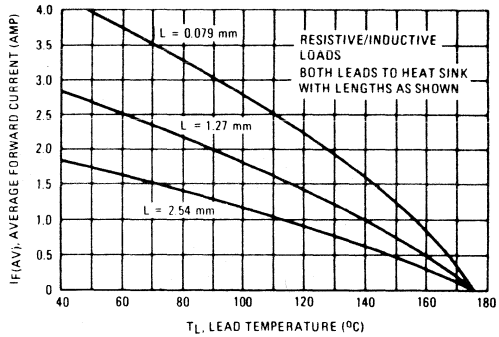


FIGURE 7 – 1.27 mm LEAD LENGTH, VARIOUS LOADS

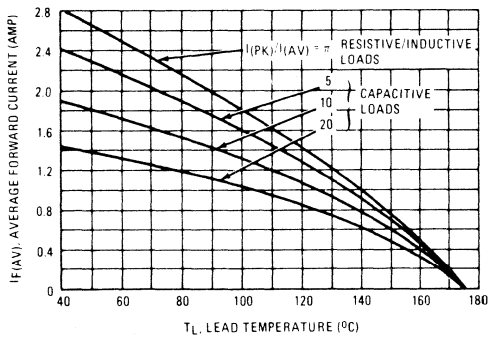


FIGURE 8 – PRINTED CIRCUIT BOARD MOUNTING VARIOUS LOADS

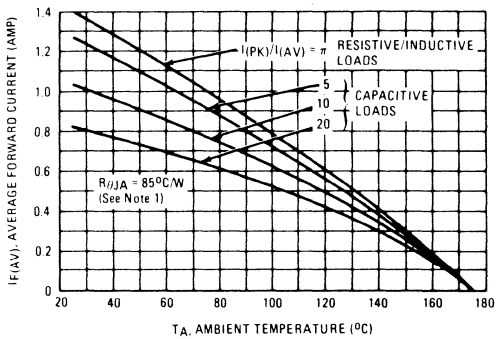
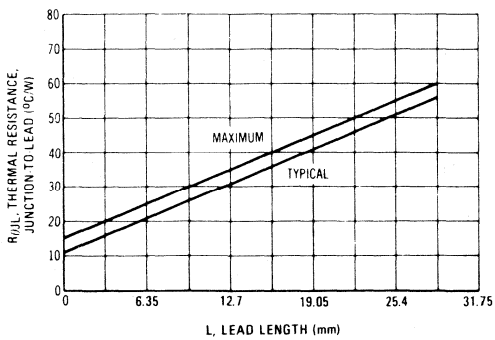


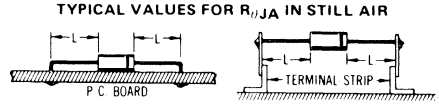
FIGURE 9 – STEADY-STATE THERMAL RESISTANCE



NOTE 1

Data shown for thermal resistance junction-to-ambient ($R_{\theta JA}$) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured

TYPICAL VALUES FOR $R_{\theta JA}$ IN STILL AIR



MOUNTING METHOD 1 — MOUNTING METHOD 2

MOUNTING METHOD	LEAD LENGTH (cm) 0.079	1.27	2.54	$R_{\theta JA}$
1	—	75	85	C/W
2	55	72	85	C/W

7

TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 10 – FORWARD RECOVERY TIME

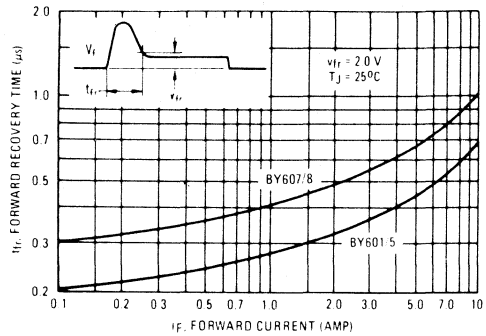


FIGURE 11 – REVERSE RECOVERY TIME

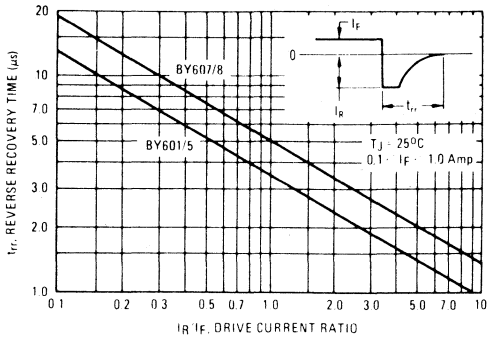


FIGURE 12 – JUNCTION CAPACITANCE

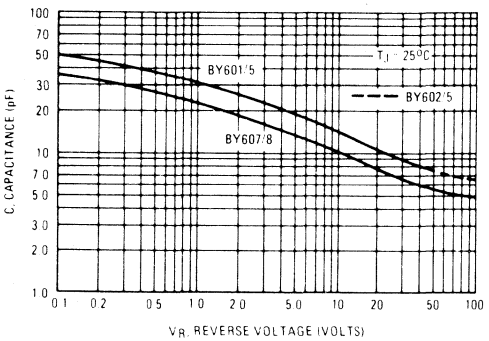


FIGURE 13 – RECTIFICATION WAVEFORM EFFICIENT FOR SINE WAVE

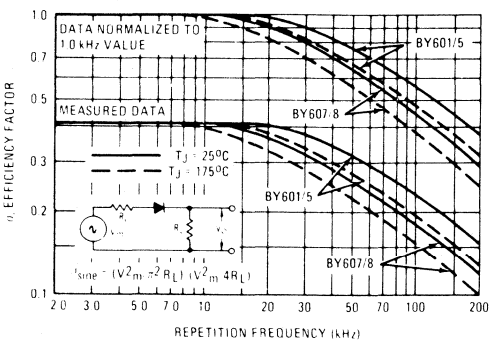
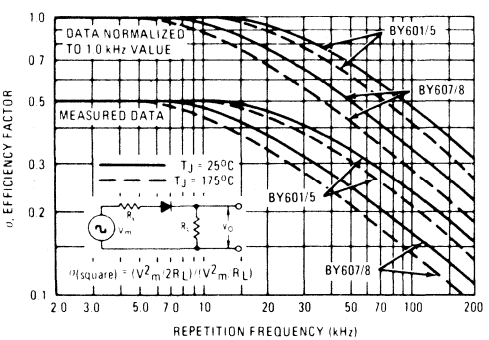


FIGURE 14 – RECTIFICATION WAVEFORM EFFICIENCY FOR SQUARE WAVE



RECTIFIER EFFICIENCY NOTE

The rectification efficiency factor σ shown in Figures 13 and 14 was calculated using the formula:

$$\sigma = \frac{P_{dc}}{P_{rms}} = \frac{\frac{V^2_{O(dc)}}{R_L}}{\frac{V^2_{O(rms)}}{R_L}} \bullet 100\% = \frac{V^2_{O(dc)}}{V^2_{O(ac)} + V^2_{O(dc)}} \bullet 100\% \quad (1)$$

For a sine wave input $V_m \sin(\omega t)$ to the diode, assumed lossless, the maximum theoretical efficiency factor becomes 40%; for a square wave input of amplitude V_m, the efficiency factor becomes 50%. (A full wave circuit has twice these efficiencies).

As the frequency of the input signal is increased, the reverse recovery time of the diode (Figure 11) becomes significant, resulting in an increasing ac voltage component across R_L which is opposite in polarity to the forward current thereby reducing the value of the efficiency factor σ, as shown in Figures 13 and 14.

It should be emphasized that Figures 13 and 14 show waveform efficiency only, they do not account for diode losses. Data was obtained by measuring the ac component of V_O with a true rms voltmeter and the dc component with a dc voltmeter. The data was used in Equation 1 to obtain points for the Figures.

BYT 25—50 thru BYT 25—1000 SERIES

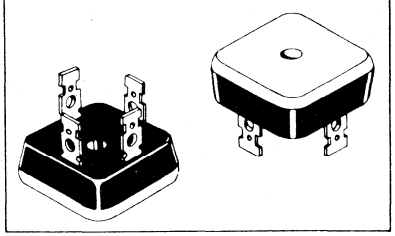
RECTIFIER ASSEMBLY

. . . utilizing individual void-free molded rectifiers, interconnected and mounted on an electrically isolated aluminum heat sink by a high thermal-conductive epoxy resin.

- 400 Ampere Surge Capability
- Electrically Isolated Base
- 1800 Volt Heat Sink Isolation
- Maximum space saving

MINIATURE SINGLE PHASE FULL-WAVE BRIDGE

25 AMPERES
50—1000 VOLTS



MAXIMUM RATINGS

Rating (Per Diode)	Symbol	BYT25							Unit
		50	100	200	400	600	800	1000	
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	400	600	800	1000	Volts
DC Output Voltage Resistive Load Capacitive Load	Vdc	30 50	62 100	124 200	250 400	380 600	500 800	630 1000	Volts
Sine Wave RMS Input Voltage	V_R(RMS)	35	70	140	280	420	560	700	Volts
Average Rectified Forward Current (Single phase bridge, resistive load, 50 Hz, T_C = 55 °C	I_O	25							Amp
Non-Repetitive Peak Surge Current applied (Surge at rated load conditions)	I_{FSM}	400							Amp
Operating and Storage Junction	T_J, T_{stg}	−60 to +175							°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Thermal Resistance, Junction to Case Each Die Total Bridge	$R_{\theta JC}$	 8.0 2.0	 10 2.8	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Instantaneous Forward Voltage (Per Diode) (i_F = 40 A)	V_F	–	0.95	1.05	Volts
Reverse Current (Per Diode) (Rated V_R)	I_R	–	–	0.10	mA

MECHANICAL CHARACTERISTICS

CASE: Plastic case with an electrically isolated aluminum base.

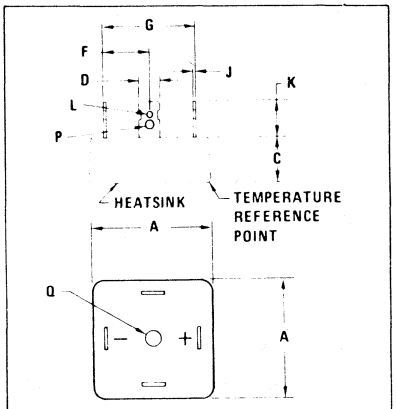
POLARITY: Terminal designation embossed on case:
+DC output
−DC output
AC not marked

MOUNTING POSITION: Bolt down. Highest heat transfer efficiency accomplished through the surface opposite the terminals. Use silicone heat sink compound on mounting surface for maximum heat transfer.

WEIGHT: 25 grams (approx.)

TERMINALS: Suitable for fast-on connections. Readily solderable, corrosion resistant. Soldering recommended for applications greater than 15 amperes.

MOUNTING TORQUE: 20 in. lb. max.



NOTE:
1. DIM "Q" SHALL BE MEASURED ON HEATSINK SIDE OF PKG.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.65	26.16	1.010	1.030
C	12.44	13.97	0.490	0.550
D	6.10	6.60	0.240	0.260
F	10.01	10.49	0.394	0.413
G	19.99	21.01	0.787	0.827
J	0.71	0.86	0.028	0.034
K	10.41	11.43	0.410	0.450
L	1.52	2.06	0.060	0.081
P	2.79	2.92	0.110	0.115
Q	4.42	4.67	0.174	0.184

CASE 309A-03

7

FIGURE 1 – FORWARD VOLTAGE

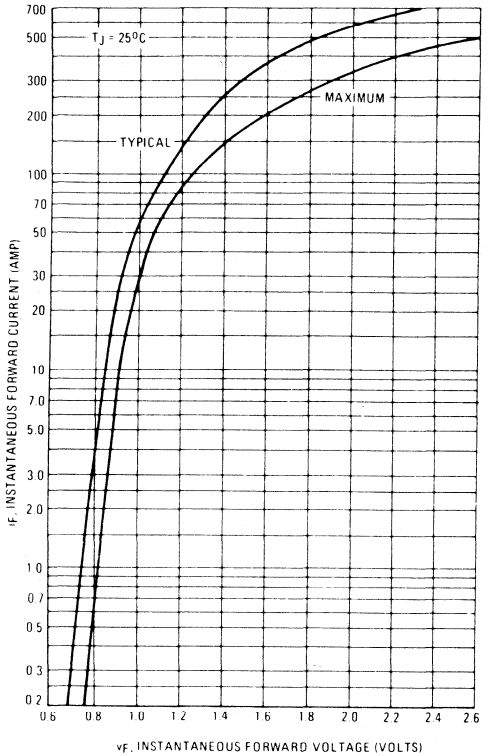


FIGURE 2 – NON REPETITIVE SURGE CURRENT

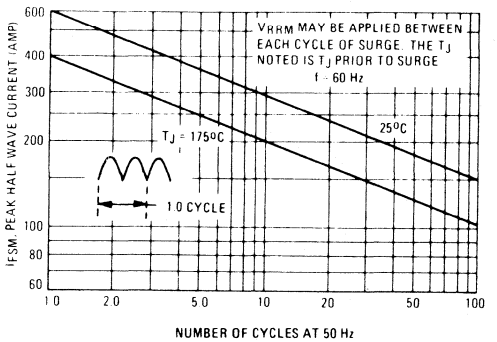


FIGURE 3 – FORWARD VOLTAGE TEMPERATURE COEFFICIENT

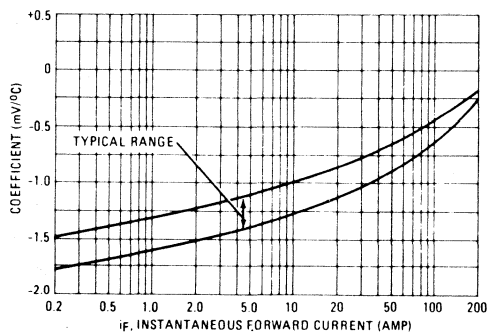


FIGURE 4 – CURRENT DERATING

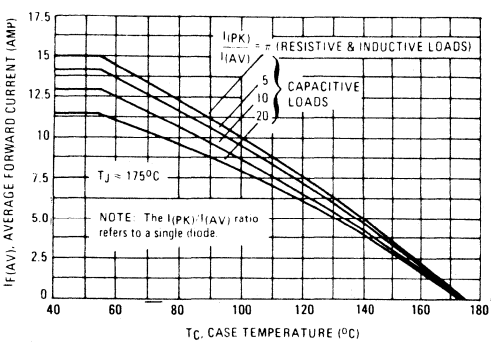


FIGURE 5 – FORWARD POWER DISSIPATION

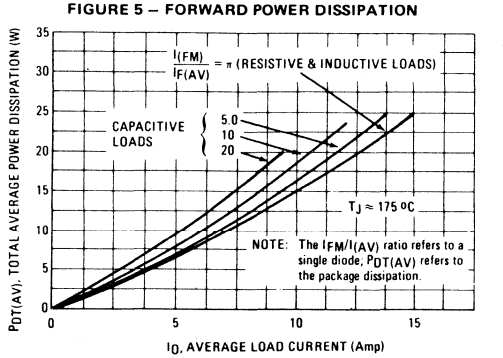
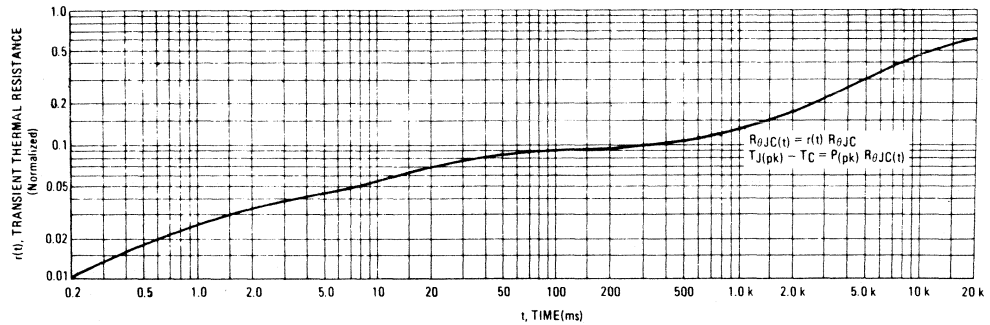
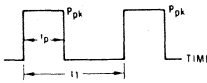


FIGURE 6 – TYPICAL THERMAL RESPONSE



NOTE 1



DUTY CYCLE D = t_p / t_1
PEAK POWER P_{pk} is peak of an equivalent square power pulse

To determine maximum junction temperature of the diode in a given situation, the following procedure is recommended.

The temperature of the case should be measured using a thermocouple placed on the case at the temperature reference point (see the outline drawing on page 1). The thermal mass connected to the case is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady state conditions are achieved. Using the measured value of T_C, the junction temperature may be determined by:

$$T_J = T_C + \Delta T_{JC}$$

where ΔT_{JC} is the increase in junction temperature above the case temperature. It may be determined by:

$$\Delta T_{JC} = P_{pk} \bullet R_{\theta JC} [D + (1 - D) \bullet r(t_1 + t_p) + r(t_p) - r(t_1)]$$

where

r(t) = normalized value of transient thermal resistance at time, t, from Figure 8, i.e.,

$r(t_1 + t_p)$ = normalized value of transient thermal resistance at time $t_1 + t_p$.

FIGURE 7 – CAPACITANCE

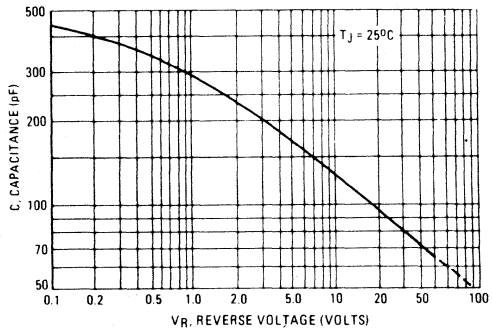


FIGURE 8 – FORWARD RECOVERY TIME

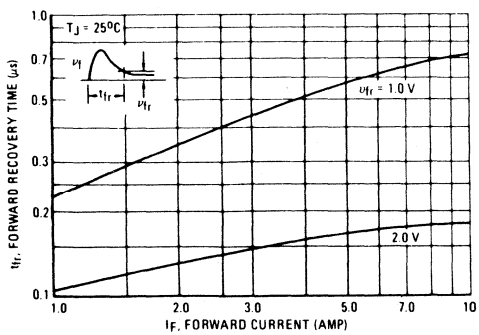
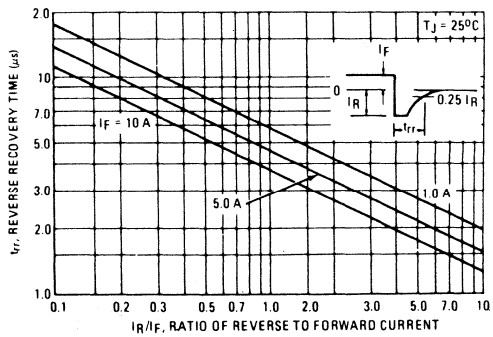


FIGURE 9 – REVERSE RECOVERY TIME



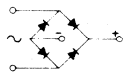
7

BYW 20 SERIES

RECTIFIER ASSEMBLY

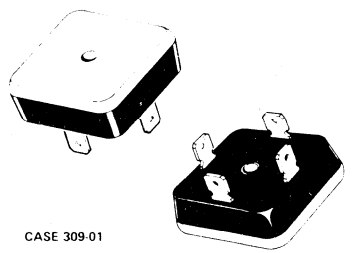
. . . utilizing individual void-free molded MR2500 Series rectifiers, interconnected and mounted on an electrically isolated aluminium heat sink by a high thermal-conductive epoxy resin.

- 400 Ampere Surge Capability
- Electrically Isolated Base (Isolation Breakdown Voltage 2.5 KV).
- Cost Effective in Lower Current Applications
- Maximum Power Dissipation 25 Watts



SINGLE-PHASE FULL-WAVE BRIDGE

15 AMPERES
50-1000 VOLTS



CASE 309-01

MAXIMUM RATINGS

Rating (Per Diode)	Symbol	BYW 20	BYW 21	BYW 22	BYW 24	BYW 26	BYW 28	BYW 79	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	400	600	800	1000	Volts
DC Output Voltage Resistive Load Capacitive Load	Vdc	 30 50	 62 100	 124 200	 250 400	 380 600	 500 800	 630 1000	Volts
Sine Wave RMS Input Voltage	$V_{R(RMS)}$	35	70	140	280	420	560	700	Volts
Average Rectified Forward Current (Single phase bridge, resistive load, 50 Hz, T_C = 55 °C	I_O	15							Amp
Non Repetitive Peak Surge Current applied (Surge at rated load conditions)	I_{FSM}	400							Amp
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +175							°C

THERMAL CHARACTERISTICS (Total Bridge)

Characteristic	Symbol	Typ	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.1	2.75	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Instantaneous Forward Voltage (Per Diode) (I_F = 24 A)	V_F	--	1.0	1.10	Volts
Reverse Current (Per Diode) (Rated V_R)	I_R	--	--	0.10	mA

MECHANICAL CHARACTERISTICS

CASE: Plastic case with electrically isolated aluminum base.

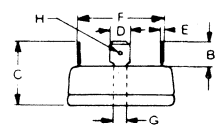
POLARITY: Terminal designation embossed on case:
+ DC output,
- DC output,
AC not marked.

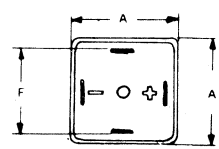
MOUNTING POSITION: Bolt down. Highest heat transfer efficiency accomplished through the surface opposite the terminals. Use silicon grease on mounting surface for maximum heat transfer.

WEIGHT: 40 grams (approx.)

TERMINALS: Suitable for fast-on connections. Readily solderable, corrosion resistant. Soldering recommended for applications greater than 15 Amperes.

MOUNTING TORQUE: 0.23 Kg-m. Max.





Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	1.368	1.387	34.75	35.25
B	.344	.364	8.75	9.25
C	.836	.875	21.25	22.25
D	.244	.251	6.20	6.40
E	.030	.032	0.77	0.83
F	1.102	1.125	28.00	28.60
G	.165	.177	4.20	4.50
H	.064	.068	1.65	1.75

NOTES
1. Hole is counter sunk for # 6 socket head screw.
2. Dim. "B", "C", "D", "E" and "H" are typical.

FIGURE 1 – FORWARD VOLTAGE

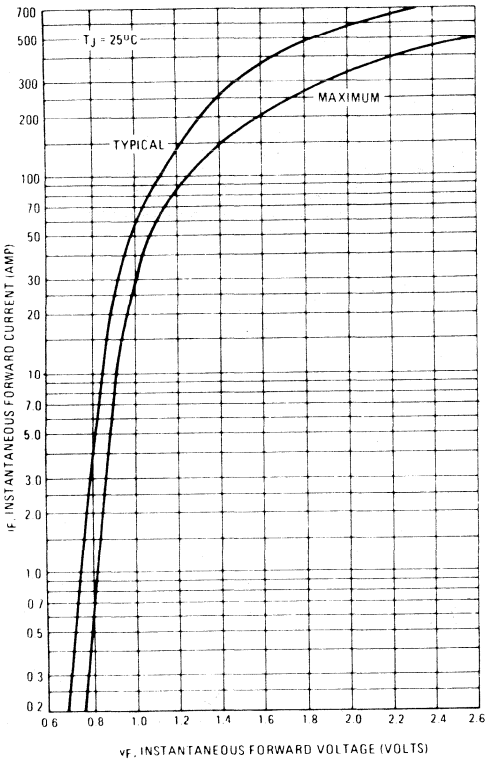


FIGURE 2 – NON REPETITIVE SURGE CURRENT

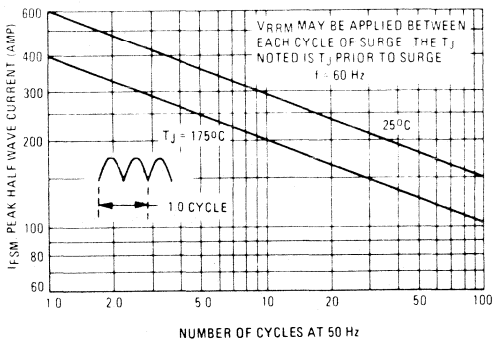


FIGURE 3 – FORWARD VOLTAGE TEMPERATURE COEFFICIENT

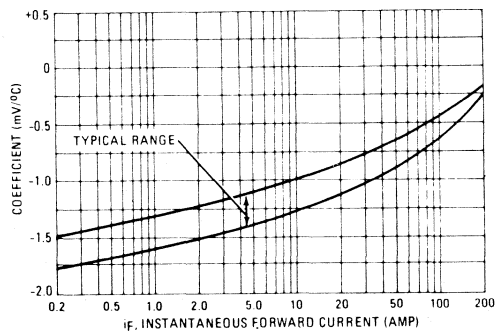


FIGURE 4 – CURRENT DERATING

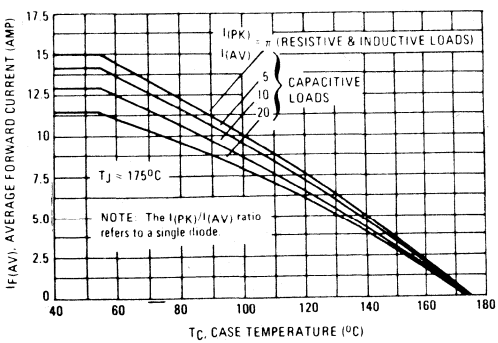


FIGURE 5 – FORWARD POWER DISSIPATION

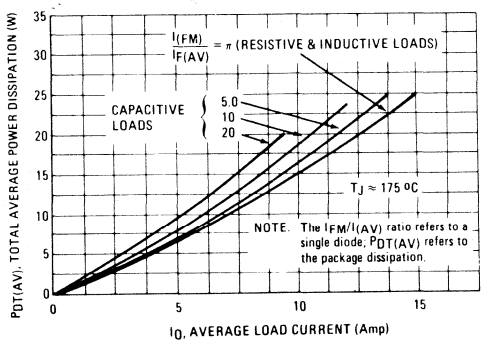


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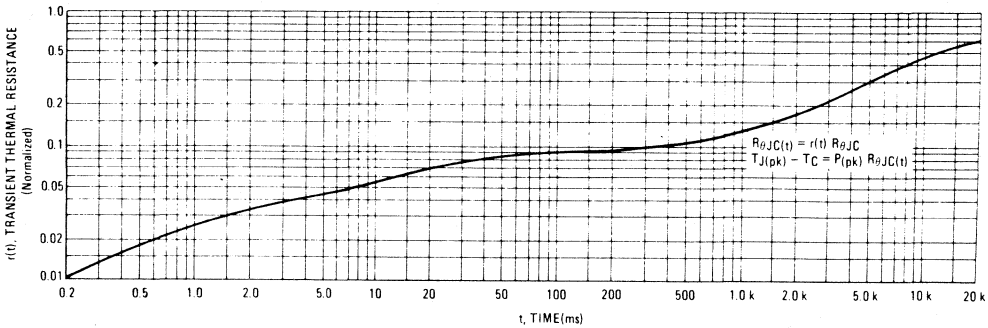
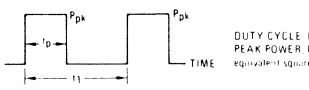
FIGURE 6 – TYPICAL THERMAL RESPONSE



NOTE 1



To determine maximum junction temperature of the diode in a given situation, the following procedure is recommended.

The temperature of the case should be measured using a thermocouple placed on the case at the temperature reference point (see the outline drawing on page 1). The thermal mass connected to the case is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady state conditions are achieved. Using the measured value of T_C, the junction temperature may be determined by:

$$T_J = T_C + \Delta T_{JC}$$

where ΔT_{JC} is the increase in junction temperature above the case temperature. It may be determined by:

$$\Delta T_{JC} = P_{pk} \bullet R_{\theta JC} [D + (1 - D) \bullet r(t_1 + t_p) + r(t_p) - r(t_1)]$$

where

r(t) = normalized value of transient thermal resistance at time, t, from Figure 8, i.e.,

$r(t_1 + t_p)$ = normalized value of transient thermal resistance at time $t_1 + t_p$.

FIGURE 7 – CAPACITANCE

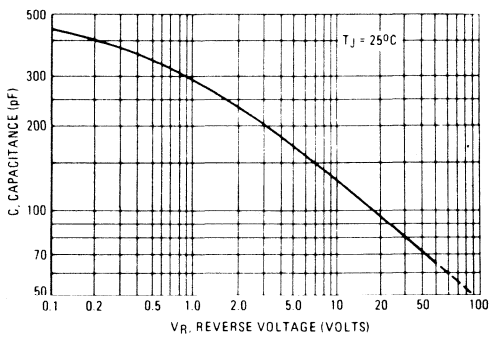


FIGURE 8 – FORWARD RECOVERY TIME

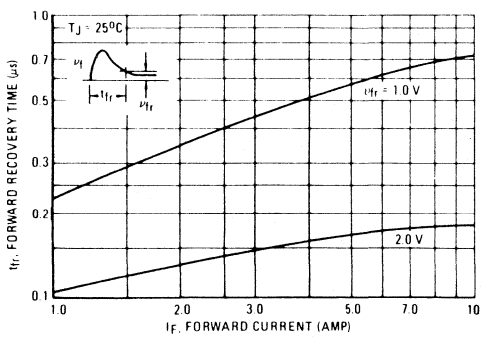
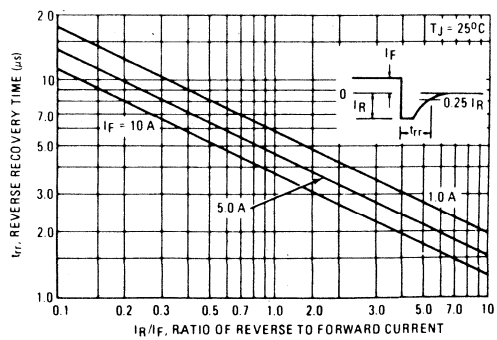


FIGURE 9 – REVERSE RECOVERY TIME



BYX 10

Designers Data Sheet

"SURMETIC" RECTIFIERS

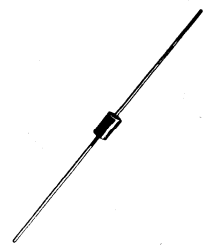
. . . subminiature size, axial lead-mounted rectifier for general-purpose, low-power applications.

Designers Data for "Worst Case" Conditions

The Designers Data Sheets permit the design of most circuits entirely from the information presented. Limits curves—representing boundaries on device characteristics—are given to facilitate "worst-case" design.

LEAD-MOUNTED SILICON RECTIFIER

1600 VOLTS
0,5 AMPERE



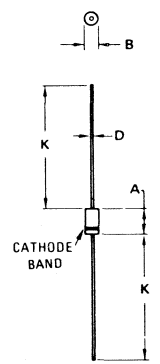
MAXIMUM RATINGS

Rating	Symbol	BYX 10	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	800*	Volts
Nonrepetitive Peak Reverse Voltage (Halfwave, Single Phase, 60 Hz)	V_{RSM}	1600*	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	560*	Volts
Average Rectified Forward Current (Single Phase, Resistive Load, 60 Hz, T_L = 70°C, 1/2" From Body)	I_O	0.5* 1.0* (MOTOROLA SPECIFIED)	Amp
Nonrepetitive Peak Surge Current (Surge Applied at Rated Load Conditions, See Figure 2)	I_{FSM}	30 (for 1 cycle)	Amp
Storage Temperature Range	T_{stg}	-65 to +175	°C
Operating Temperature Range	T_L	-65 to +170	°C
DC Blocking Voltage Temperature	T_L	150	°C

ELECTRICAL CHARACTERISTICS

Characteristic and Conditions	Symbol	Typ	Max	Unit
Maximum Instantaneous Forward Voltage Drop (i_F = 2.0 Amp Peak, T_L = 170° C, 1/2 Inch Leads)	v_F	–	1.1	Volts
Maximum Reverse Current (Rated dc Voltage) T = 25° C	I_R		1.0	μA
T_J = 125° C			50	μA

* Indicates Pro-electron Registered Data



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94	–	1.100	–

CASE 59-04
Dimensions Within JEDEC DO-15 Outline.

MECHANICAL CHARACTERISTICS

CASE: Void free, transfer molded

MAXIMUM LEAD TEMPERATURE FOR SOLDERING PURPOSES: 240°C, 1/8" from case for 10 seconds at 5 lbs. tension

FINISH: All external surfaces are corrosion-resistant, leads are readily solderable

POLARITY: Cathode indicated by color band

WEIGHT: 0.40 grams (approximately)

7

FIGURE 1 – FORWARD VOLTAGE

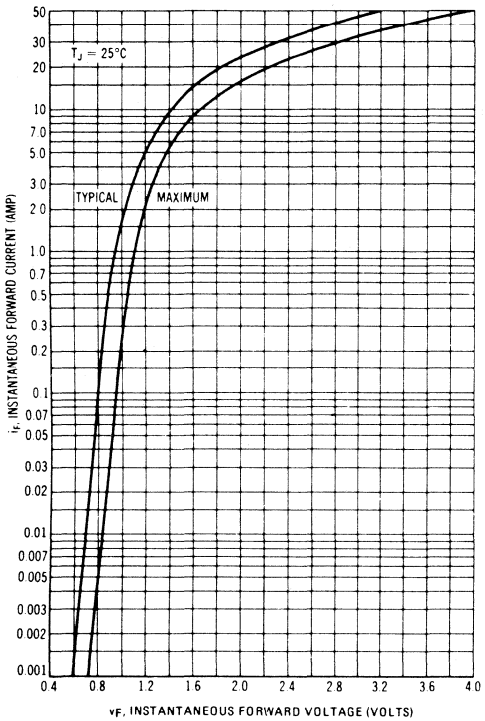


FIGURE 2 – MAXIMUM NONREPETITIVE SURGE CURRENT

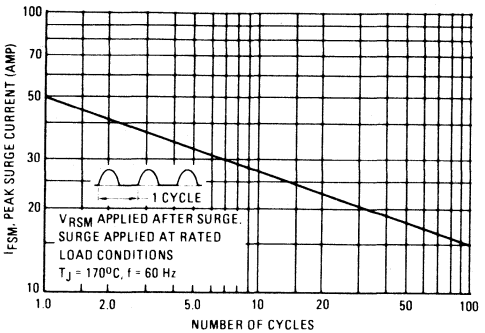


FIGURE 3 – FORWARD VOLTAGE TEMPERATURE COEFFICIENT

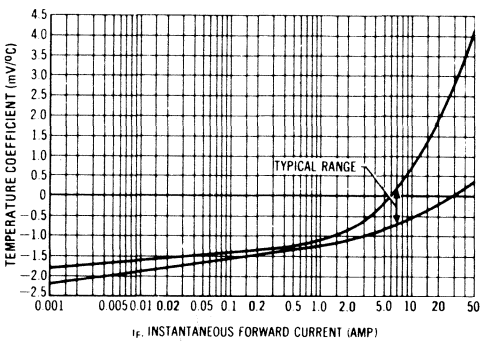
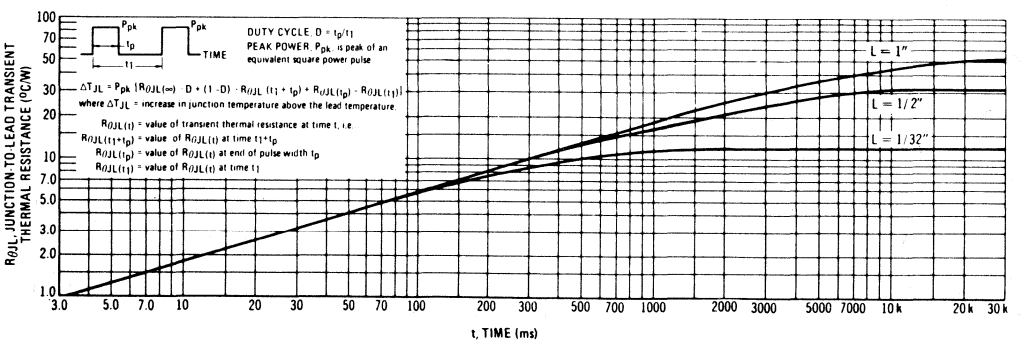


FIGURE 4 – TYPIÇAL TRANSIENT THERMAL RESISTANCE



The temperature of the lead should be measured using a thermocouple placed on the lead as close as possible to the tie point. The thermal mass connected to the tie point is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady-state conditions are achieved. Using the measured value of T_L, the junction temperature may be determined by:

$$T_J = T_L + \Delta T_{JL}.$$

FIGURE 5 – FORWARD POWER DISSIPATION

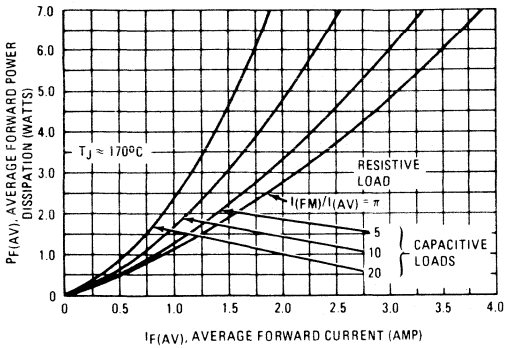


FIGURE 6 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

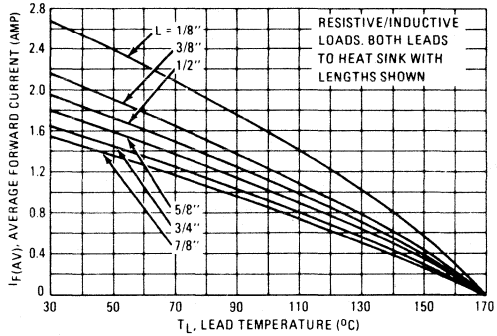


FIGURE 7 – 1/2" LEAD LENGTH, VARIOUS LOADS

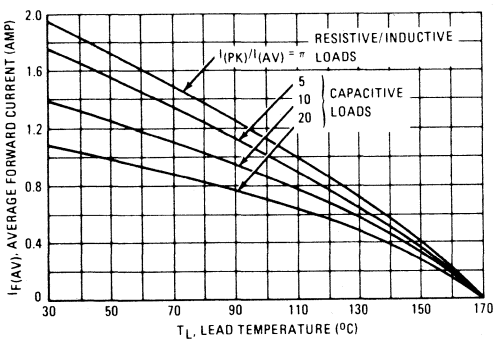


FIGURE 8 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS

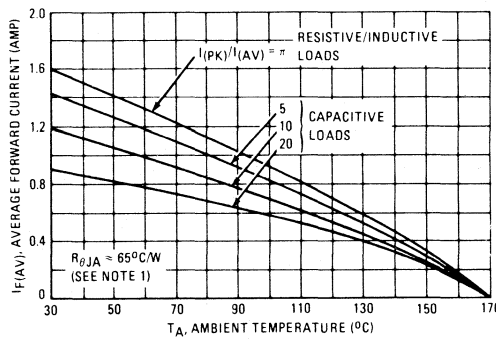
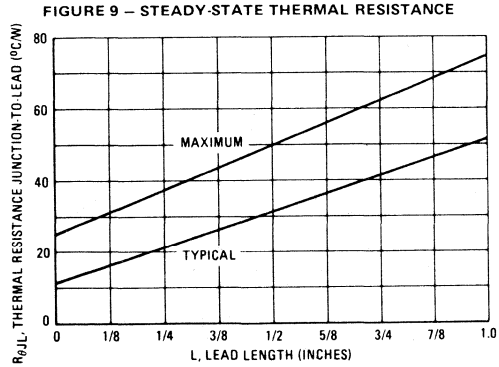


FIGURE 9 – STEADY-STATE THERMAL RESISTANCE



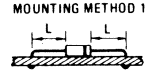
NOTE 1

Data shown for thermal resistance junction-to-ambient (θ_{JA}) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

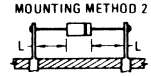
TYPICAL VALUES FOR θ_{JA} IN STILL AIR

MOUNTING METHOD	LEAD LENGTH, L (IN) 1/8	1/4	1/2	3/4	$R_{\theta JA}$
1	65	72	82	92	$^oC/W$
2	74	81	91	101	$^oC/W$
3	40				$^oC/W$

MOUNTING METHOD 1



MOUNTING METHOD 2



Vector pin mounting

MOUNTING METHOD 3

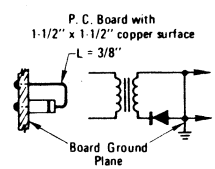


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FIGURE 10 – FORWARD RECOVERY TIME

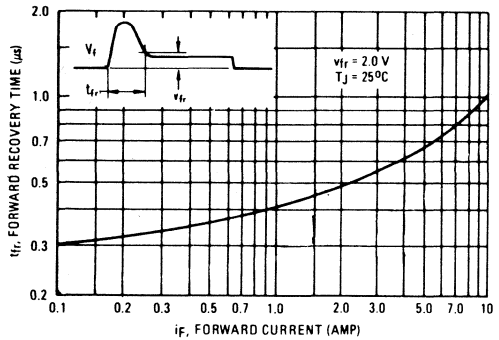


FIGURE 11 – REVERSE RECOVERY TIME

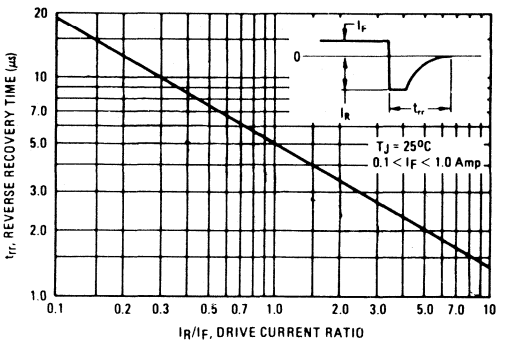


FIGURE 12 – JUNCTION CAPACITANCE

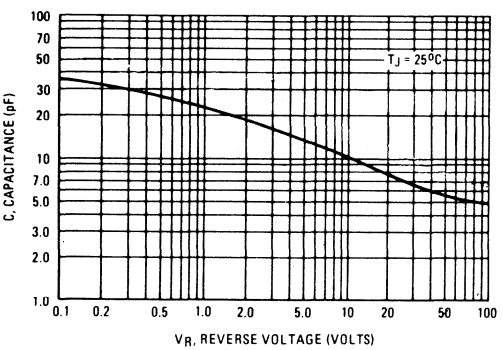


FIGURE 13 – RECTIFICATION WAVEFORM EFFICIENCY FOR SINE WAVE

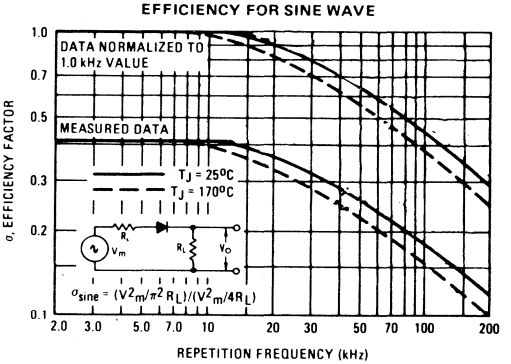
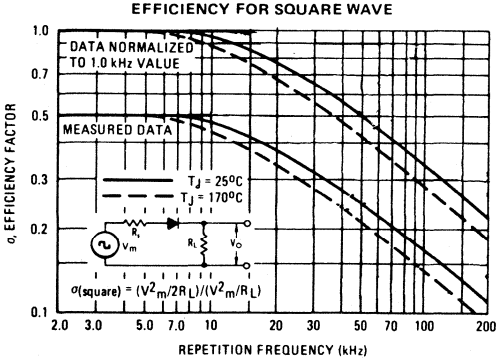


FIGURE 14 – RECTIFICATION WAVEFORM EFFICIENCY FOR SQUARE WAVE



RECTIFIER EFFICIENCY NOTE

The rectification efficiency factor σ shown in Figures 13 and 14 was calculated using the formula:

$$\sigma = \frac{P_{dc}}{P_{rms}} = \frac{\frac{V^2_{O(dc)}}{R_L}}{\frac{V^2_{O(rms)}}{R_L}} \bullet 100\% = \frac{V^2_{O(dc)}}{V^2_{O(ac)} + V^2_{O(dc)}} \bullet 100\% \quad (1)$$

For a sine wave input $V_m \sin(\omega t)$ to the diode, assumed lossless, the maximum theoretical efficiency factor becomes 40%; for a square wave input of amplitude V_m, the efficiency factor becomes 50%. (A full wave circuit has twice these efficiencies).

As the frequency of the input signal is increased, the reverse recovery time of the diode (Figure 11) becomes significant, resulting in an increasing ac voltage component across R_L which is opposite in polarity to the forward current thereby reducing the value of the efficiency factor σ, as shown in Figures 13 and 14.

It should be emphasized that Figures 13 and 14 show waveform efficiency only; they do not account for diode losses. Data was obtained by measuring the ac component of V_O with a true rms voltmeter and the dc component with a dc voltmeter. The data was used in Equation 1 to obtain points for the Figures.

BYX 55 SERIES

SUBMINIATURE SIZE, AXIAL LEAD MOUNTED FAST RECOVERY POWER RECTIFIERS

. . . designed for special applications such as dc power supplies, inverters, converters, ultrasonic systems, choppers, low RF interference and free wheeling diodes. A complete line of fast recovery rectifiers having typical recovery time of 300 nanoseconds providing high efficiency at frequencies to 250 KHz.

FAST SOFT RECOVERY POWER RECTIFIERS

350 & 600 VOLTS
1.2 AMPERE

DESIGNER'S DATA FOR "WORST CASE" CONDITIONS

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit curves – representing device characteristic boundaries – are given to facilitate "worst case" design.

MAXIMUM RATINGS

Ratings	Symbol	BYX 55–350	BYX 55–600	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	350	600	Volts
Non Repetitive Peak Reverse Voltage	V_{RSM}	350	600	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	240	420	Volts
Average Rectified Forward Current (Single phase, resistive load, T_A = 75 °C)	I_O	1.2		Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions) (T_A = 75 °C)	I_{FSM}	40		Amps
Operating Junction Temperature Range	T_J	–65 to +150		°C
Storage Temperature Range	T_{stg}	–65 to +175		°C

THERMAL CHARACTERISTICS

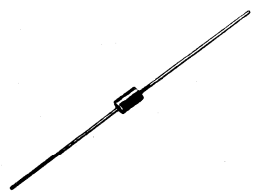
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient (Typical Printed Circuit Board Mounting)	$R_{\theta JA}$	65	°C/W

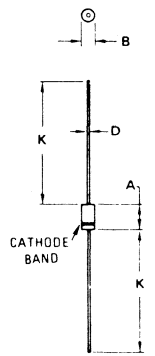
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Forward Voltage (I_F = 4.0 AMP, T_A = 25°C)	V_F	–	1.0	1.25	Volts
Reverse Current (rated dc voltage) T_A = 25°C T_A = 100°C	I_R	– –	1.0 50	10 100	μA

REVERSE RECOVERY CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Recovery Time (I_F = 1.0 Amp to V_R = 50 Vdc) (Figure 21)	t_{rr}	–		350	ns
Reverse Recovery Current (I_F = 1.0 Amp to V_R = 30 Vdc) (Figure 21)	$I_{RM(REC)}$	–	–	3.0	Amp





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94	–	1.100	–

CASE 59 04

MECHANICAL CHARACTERISTICS

CASE: Void Free, Transfer Molded

FINISH: External leads are tin plated, leads are readily solderable

POLARITY: Cathode indicated by Polarity band

WEIGHT: 0.4 Grams (Approximately)

7

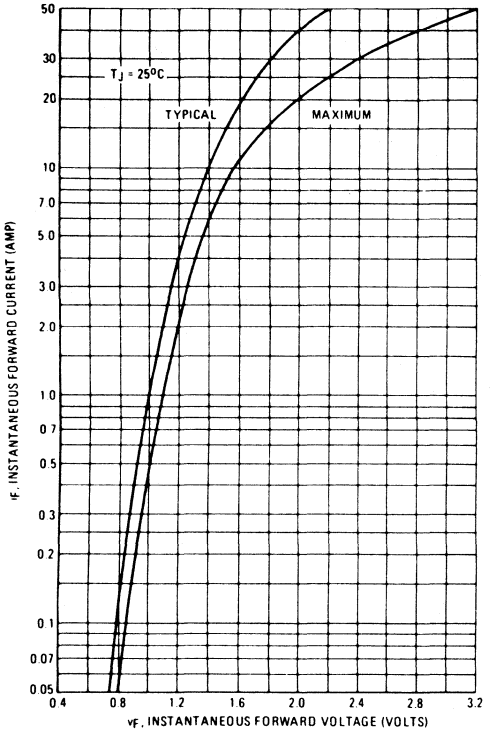


FIGURE 1 – FORWARD VOLTAGE

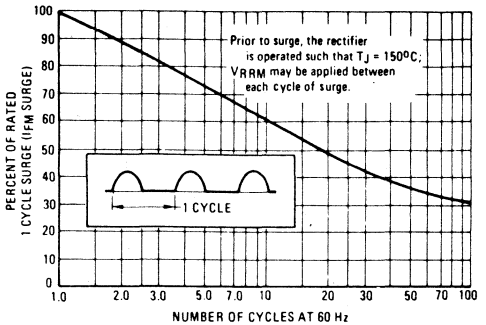


FIGURE 2 – MAXIMUM SURGE CAPABILITY

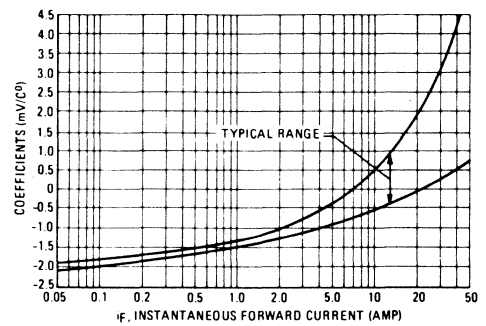


FIGURE 3 – TEMPERATURE COEFFICIENT

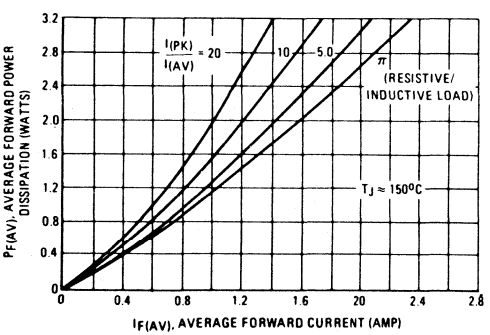


FIGURE 4 – FORWARD POWER DISSIPATION

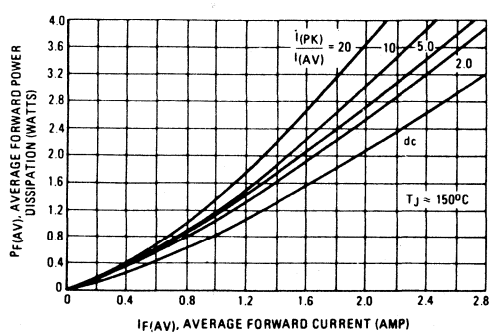


FIGURE 5 – FORWARD POWER DISSIPATION

MAXIMUM CURRENT RATINGS
(SEE NOTES 1 and 2)

SINE WAVE INPUT

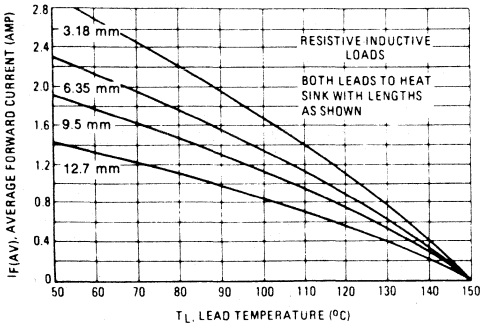


FIGURE 6 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

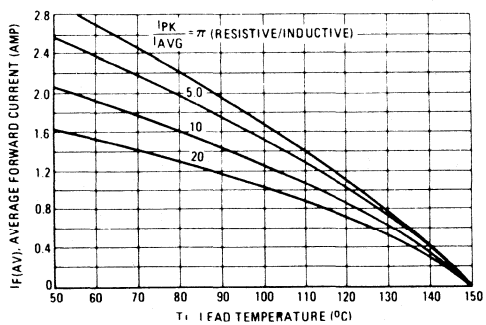


FIGURE 8 — 3.18 mm LEAD LENGTH, VARIOUS LOADS

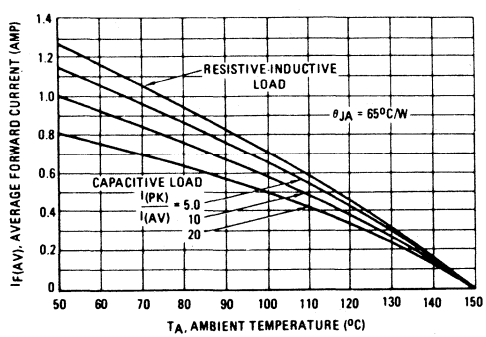


FIGURE 10 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS

SQUARE WAVE INPUT

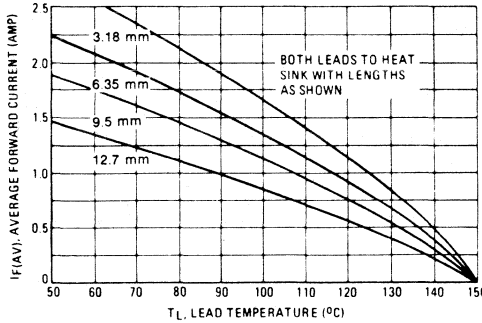


FIGURE 7 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

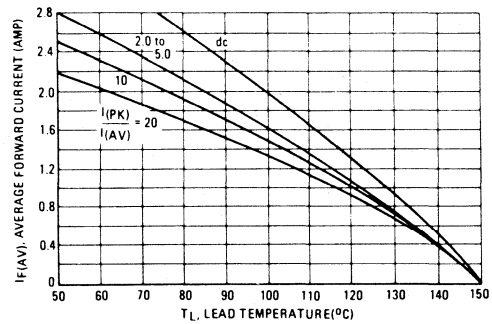


FIGURE 9 — 3.18 mm LEAD LENGTH, VARIOUS LOADS

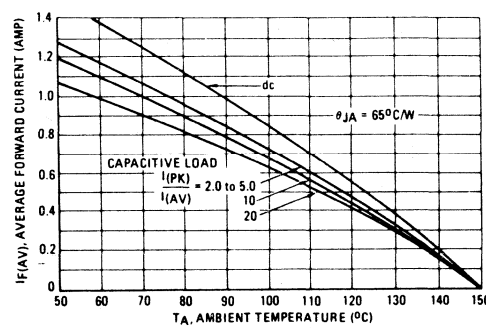


FIGURE 11 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS

7

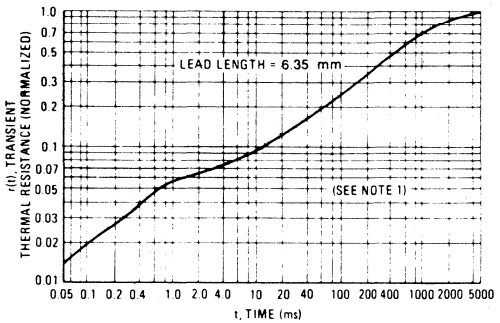


FIGURE 12 – THERMAL RESPONSE

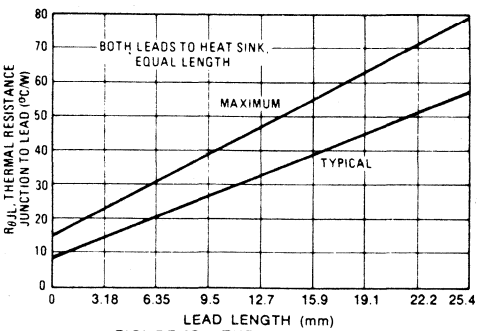
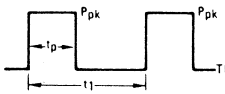


FIGURE 13 – THERMAL RESISTANCE

NOTE 1



DUTY CYCLE, $D = t_p/t_1$
PEAK POWER, P_{pk}, is peak of an equivalent square power pulse.

To determine maximum junction temperature of the diode in a given situation, the following procedure is recommended.

The temperature of the case should be measured using a thermocouple placed on the case as close as possible to the tie point. The thermal mass connected to the tie point is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady-state conditions are achieved. Using the measured value of T_C, the junction temperature may be determined by:

$$T_J = T_C + \Delta T_{JC}$$

where ΔT_{JC} is the increase in junction temperature above the case temperature. It may be determined by:

$$\Delta T_{JC} = P_{pk} \cdot R_{\theta JC}\left[D + (1 - D) \cdot r(t_1 + t_p) + r(t_p) - r(t_1)\right]$$

where

$r(t)$ = normalized value of transient thermal resistance at time, t, from Figure 12, i.e.:

$r(t_1 + t_p)$ = normalized value of transient thermal resistance at time $t_1 + t_p$.

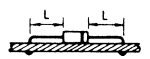
NOTE 2

Data shown for thermal resistance junction-to-ambient (θ_{JA}) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

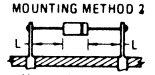
TYPICAL VALUES FOR θ_{JA} IN STILL AIR

MOUNTING METHOD	LEAD LENGTH, L(mm) 3.81	6.35	12.7	19.1	$R_{\theta JA}$
1	65	72	82	92	°C/W
2	74	81	91	101	°C/W
3	40				°C/W

MOUNTING METHOD 1

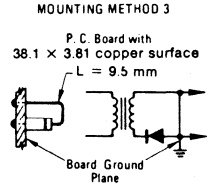


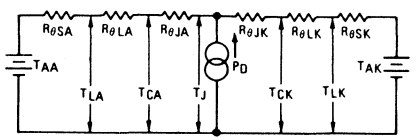
MOUNTING METHOD 2



Vector pin mounting

MOUNTING METHOD 3





Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heat sink. Terms in the model signify:

T_A = Ambient Temperature
T_L = Lead Temperature
T_C = Case Temperature
T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_D = Power Dissipation

(Subscripts A and K refer to anode and cathode sides respectively.)

Values for thermal resistance components are:

$R_{\theta L}$ = 112°C/W/IN. Typically and 128°C/W/IN Maximum

$R_{\theta J}$ = 18°C/W Typically and 30°C/W Maximum

The maximum lead temperature may be calculated as follows:

$$T_L = 150^{\circ} - \Delta T_{JL}$$

ΔT_{JL} can be calculated as shown in NOTE 1 or it may be approximated as follows:

$\Delta T_{JL} \approx R_{\theta JL} \cdot P_F$; P_F may be formulated for sine-wave operation from Figure 3 or from Figure 4 for square-wave operation.

FIGURE 14 – THERMAL CIRCUIT MODEL

TYPICAL DYNAMIC CHARACTERISTICS

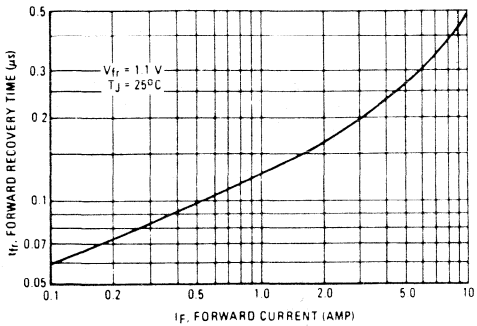


FIGURE 15 – FORWARD RECOVERY TIME

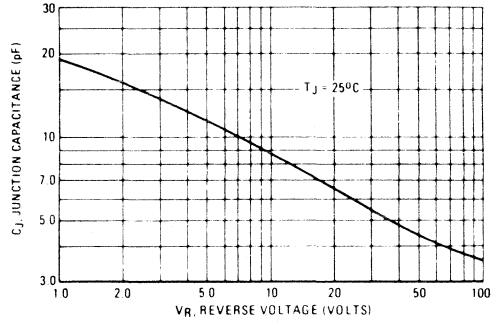


FIGURE 16 – JUNCTION CAPACITANCE

TYPICAL RECOVERED STORED CHARGE DATA
(SEE NOTE 3)

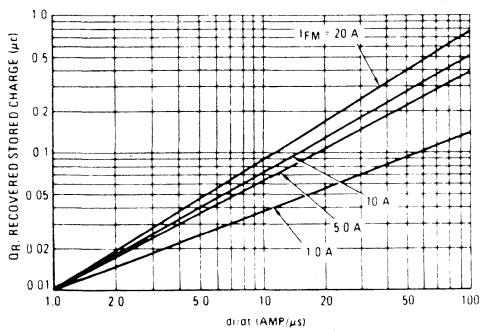


FIGURE 17 – T_J = 25°C

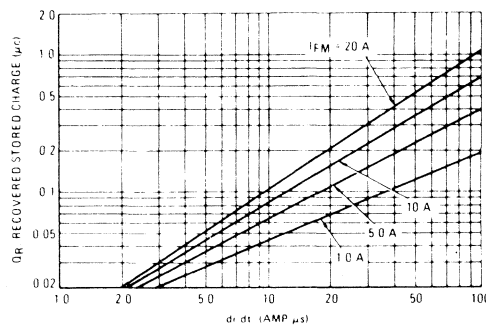


FIGURE 18 – T_J = 75°C

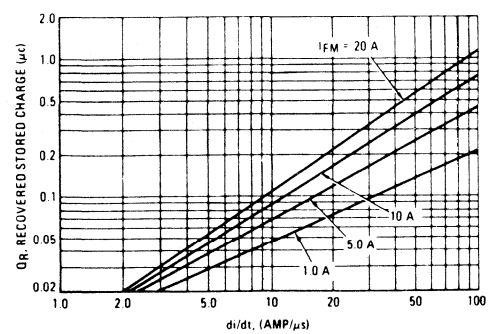


FIGURE 19 – T_J = 100°C

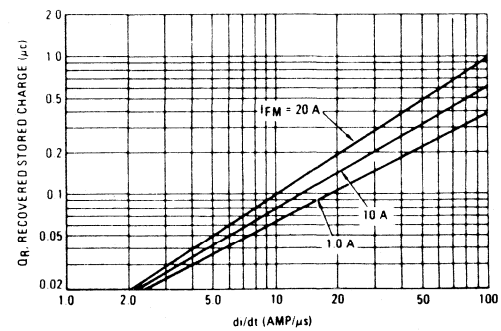


FIGURE 20 – T_J = 150°C

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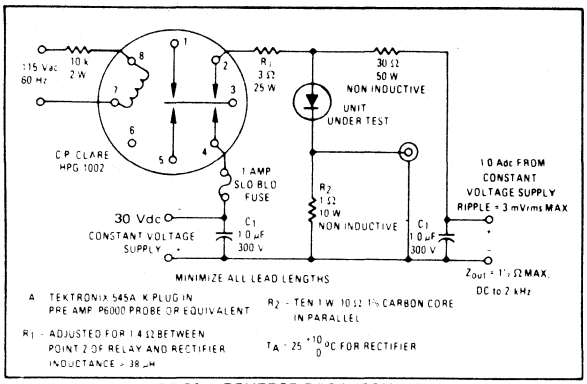


FIGURE 21 – REVERSE RECOVERY CIRCUIT

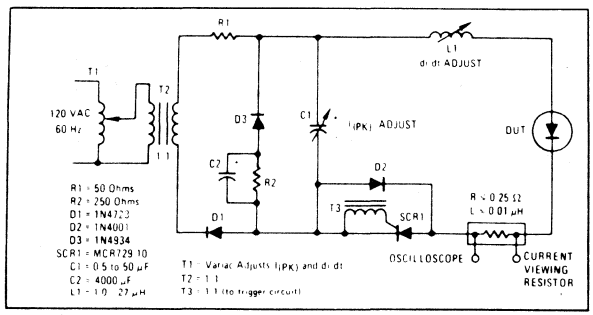


FIGURE 22 – JEDEC REVERSE RECOVERY CIRCUIT

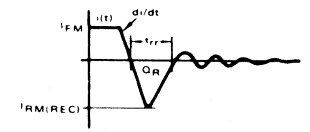
NOTE 3

Reverse recovery time is the period which elapses from the time that the current, thru a previously forward biased rectifier diode, passes thru zero going negatively until the reverse current recovers to a point which is less than 10% peak reverse current.

Reverse recovery time is a direct function of the forward current prior to the application of reverse voltage.

For any given rectifier, recovery time is very circuit dependent. Typical and maximum recovery time of all Motorola fast recovery power rectifiers are rated under a fixed set of conditions using I_F = 1.0 A, V_R = 50 V. In order to cover all circuit conditions, curves are given for typical recovered stored charge versus commutation di/dt for various levels of forward current and for junction temperatures of 25°C, 75°C, 100°C, and 150°C.

To use these curves, it is necessary to know the forward current level just before commutation, the circuit commutation di/dt, and the operating junction temperature. The reverse recovery test current waveform for all Motorola fast recovery rectifiers is shown.



From stored charge curves versus di/dt, recovery time (t_{rr}) and peak reverse recovery current ($I_{RM(REC)}$) can be closely approximated using the following formulas

$$t_{rr} = 1.41 \times \left[\frac{Q_R}{di/dt}\right]^{1/2}$$

$$I_{RM(REC)} = 1.41 \times \left[Q_R \times di/dt\right]^{1/2}$$

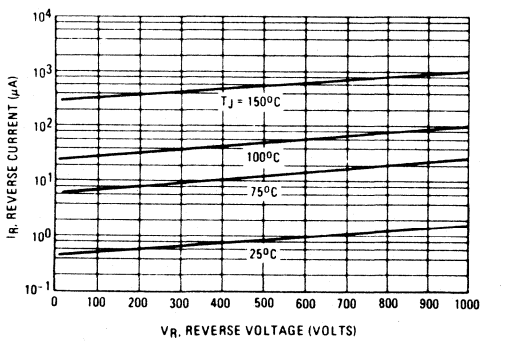


FIGURE 23 – TYPICAL REVERSE LEAKAGE

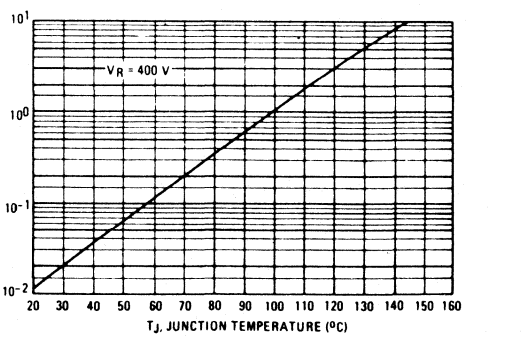


FIGURE 24 – TYPICAL REVERSE LEAKAGE

BZX79C2V4 thru BZX79C200

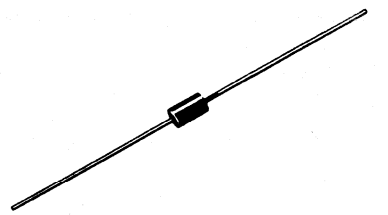
500 MILLIWATT HERMETICALLY SEALED GLASS SILICON ZENER DIODES

. . . A completely new line of 500 mW Zener Diodes offering the following advantages:

- Complete Voltage Range — 2.4 to 200 Volts
- DO-35 Package — Smaller than Conventional DO-7 Package
- Double Slug Type Construction
- Metallurgically Bonded Construction
- Pro-Electron Registration
- Oxide Passivated Die

GLASS ZENER DIODES

500 MILLIWATT
2.4 – 200 VOLTS



***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
DC Power Dissipation @ $T_L \leq 50^oC$, Lead Length = 10 mm	P_D	500	mW
Derate above 50^oC		3.33	$mW/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +200	^oC

MECHANICAL CHARACTERISTICS

CASE: Double slug type, hermetically sealed glass

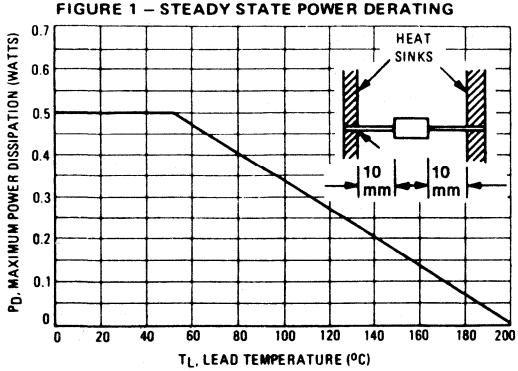
MAXIMUM LEAD TEMPERATURE FOR SOLDERING PURPOSES: 230^oC, 2 mm from case for 10 seconds

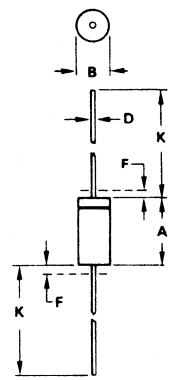
FINISH: All external surfaces are corrosion resistant with readily solderable leads.

POLARITY: Cathode indicated by color band. When operated in zener mode, cathode will be positive with respect to anode.

MOUNTING POSITION: Any

FIGURE 1 – STEADY STATE POWER DERATING





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	3.05	5.08	0.120	0.200
B	1.52	2.29	0.060	0.090
D	0.46	0.56	0.018	0.022
F	–	1.27	–	0.050
K	12.70	–	0.500	–

All JEDEC dimensions and notes apply.

CASE 299-01
DO-35

NOTE:
1. POLARITY DENOTED BY CATHODE BAND.
2. LEAD DIAMETER IS NOT CONTROLLED WITHIN DIMENSION "F".

7

***ELECTRICAL CHARACTERISTICS** (T_L = 30°C unless otherwise noted.) (V_F = 1.5 Volts Max @ I_F = 100 mAdc for all types.)

Device Type (Note 2)	Zener Voltage (Note 1) Min.	Max.	I_{ZT} = (mA)	Impedance (Ohm) @ I_{ZT} f = 1000 Hz Max. (Note 3)	Leakage Current (μ A) Max.	@ V_R = (Volt)	Temp. Coefficient (Typical) (mV/°C) Min.	Max.	Capacitance (Typical) (pF) V_R = 0, f = 1 MHz
BZX79C2V4	2.2	2.6	5	100	100	1.0	— 3.5	0	255
BZX79C2V7	2.5	2.9	5	100	75	1.0	— 3.5	0	230
BZX79C3V0	2.8	3.2	5	95	50	1.0	— 3.5	0	215
BZX79C3V3	3.1	3.5	5	95	25	1.0	— 3.5	0	200
BZX79C3V6	3.4	3.8	5	90	15	1.0	— 3.5	0	185
BZX79C3V9	3.7	4.1	5	90	10	1.0	— 3.5	+ 0.3	175
BZX79C4V3	4.0	4.6	5	90	5	1.0	— 3.5	+ 1.0	160
BZX79C4V7	4.4	5.0	5	80	3	2.0	— 3.5	+ 0.2	130
BZX79C5V1	4.8	5.4	5	60	2	2.0	— 2.7	+ 1.2	110
BZX79C5V6	5.2	6.0	5	40	1	2.0	— 2.0	+ 2.5	95
BZX79C6V2	5.8	6.6	5	10	3	4.0	0.4	3.7	90
BZX79C6V8	6.4	7.2	5	15	2	4.0	1.2	4.5	85
BZX79C7V5	7.0	7.9	5	15	1	5.0	2.5	5.3	80
BZX79C8V2	7.7	8.7	5	15	.7	5.0	3.2	6.2	75
BZX79C9V1	8.5	9.6	5	15	.5	6.0	3.8	7.0	70
BZX79C10	9.4	10.6	5	20	.2	7.0	4.5	8.0	70
BZX79C11	10.4	11.6	5	20	.1	8.0	5.4	9.0	65
BZX79C12	11.4	12.7	5	25	.1	8.0	6.0	10.0	65
BZX79C13	12.4	14.1	5	30	.1	8.0	7.0	11.0	60
BZX79C15	13.8	15.6	5	30	.05	10.5	9.2	13.0	55
BZX79C16	15.3	17.1	5	40	.05	11.2	10.4	14.0	52
BZX79C18	16.8	19.1	5	45	.05	12.6	12.9	16.0	47
BZX79C20	18.8	21.2	5	55	.05	14.0	14.4	18.0	36
BZX79C22	20.8	23.3	5	55	.05	15.4	16.4	20.0	34
BZX79C24	22.8	25.6	5	70	.05	16.8	18.4	22.0	33
BZX79C27	25.1	28.9	2	80	.05	18.9		23.5	30
BZX79C30	28.0	32.0	2	80	.05	21.0		26.0	27
BZX79C33	31.0	35.0	2	80	.05	23.1		29.0	25
BZX79C36	34.0	38.0	2	90	.05	25.2		31.0	23
BZX79C39	37.0	41.0	2	130	.05	27.3		34.0	21
BZX79C43	40.0	46.0	2	150	.05	30.1		37.0	21
BZX79C47	44.0	50.0	2	170	.05	32.9		40.0	19
BZX79C51	48.0	54.0	2	180	.05	35.7		44.0	19
BZX79C56	52.0	60.0	2	200	.05	39.2		47.0	18
BZX79C62	58.0	66.0	2	215	.05	43.4		51.0	17
BZX79C68	64.0	72.0	2	240	.05	47.6		56.0	17
BZX79C75	70.0	79.0	2	255	.05	52.5		60.0	16.5
BZX79C82	77.0	87.0	2	280	.1	62.0	46	95	29
BZX79C91	85.0	96.0	2	300	.1	69.0	51	107	28
BZX79C100	94.0	106.0	1	500	.1	76.0	57	119	27
BZX79C110	104.0	116.0	1	650	.1	84.0	63	131	26
BZX79C120	114.0	127.0	1	800	.1	91.0	69	144	24
BZX79C130	124.0	141.0	1	950	.1	99.0	75	158	23
BZX79C150	138.0	156.0	1	1250	.1	114.0	87	185	21
BZX79C160	153.0	171.0	1	1400	.1	122.0	93	200	20
BZX79C180	168.0	191.0	1	1700	.1	137.0	105	228	18
BZX79C200	188.0	212.0	1	2000	.1	152.0	120	255	17

NOTE 1: Zener voltage is measured under pulse conditions such that Tj is no more than 2° C above T.A.

NOTE 2 — TOLERANCE AND VOLTAGE DESIGNATION
Tolerance designation — The type numbers listed indicate a tolerance of ± 5%. Device tolerances of ± 2% are indicated by a "B".

NOTE 3:
Z_{ZT} is measured by dividing the ac voltage drop across the device by the ac current applied. The specified limits are for I_Z(ac) = 0.1 I_Z(dc) with the ac frequency = 1.0 kHz.

TYPICAL CHARACTERISTICS

TEMPERATURE COEFFICIENTS (-55°C to +150°C temperature range)

FIGURE 2A – ZENER VOLTAGE 2.4 to 12 VOLTS

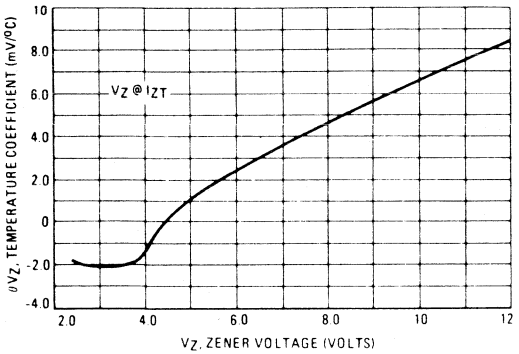


FIGURE 2B – ZENER VOLTAGE 12 to 200 VOLTS

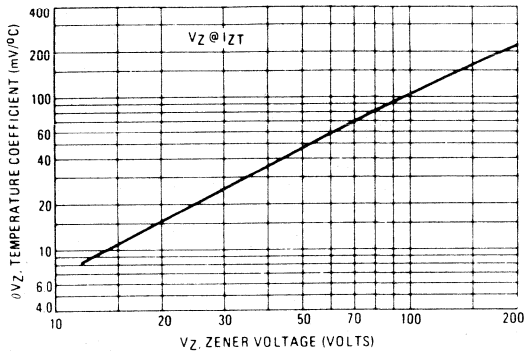


FIGURE 3 – EFFECT OF ZENER CURRENT ON ZENER IMPEDANCE

FIGURE 3A

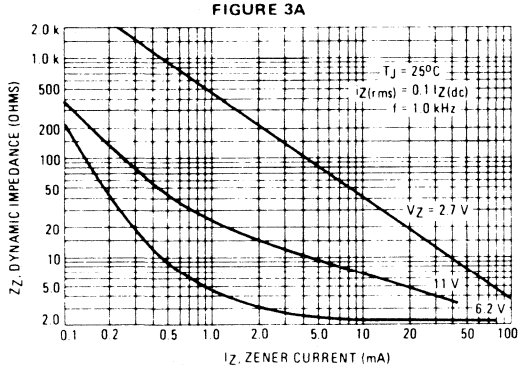


FIGURE 3B

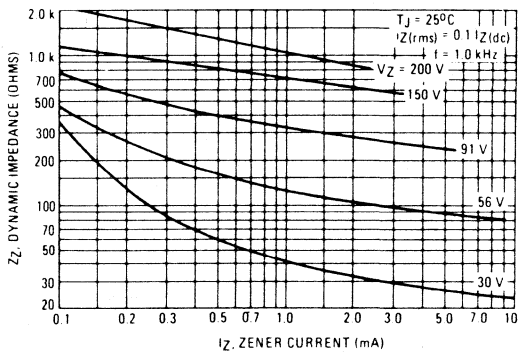
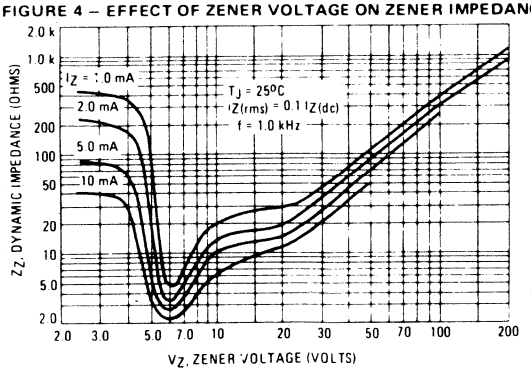


FIGURE 4 – EFFECT OF ZENER VOLTAGE ON ZENER IMPEDANCE



7

BZX83C2V7 thru BZX83C33
M-ZPD2.7 thru M-ZPD33

500 MILLIWATT HERMETICALLY SEALED GLASS SILICON ZENER DIODES

- Voltage Range 2.7 to 33 Volts according to the International E24 series (5%).
- DO-35 Package
- Double Slug Type Construction
- Metallurgically Bonded Construction
- Oxide Passivated Die

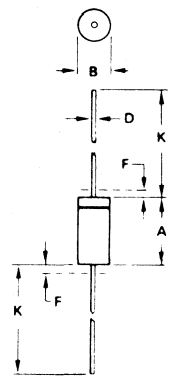
500 mW ZENER DIODES

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Power Dissipation @ $T_L \leq 25°C$ Lead Length = 4 mm Derate above 25°C	P_D	500 3.33	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +175	°C

MECHANICAL CHARACTERISTICS

MARKING: Polarity Band. Letter C (5% tolerance), Nominal voltage
CASE: Double slug type, hermetically sealed glass
MAXIMUM LEAD TEMPERATURE FOR SOLDERING PURPOSES: 230°C, 4 mm. from case for 10 seconds
FINISH: All external surfaces are corrosion resistant with readily solderable leads.
POLARITY: Cathode indicated by color band. When operated in zener mode, cathode will be positive with respect to anode.
MOUNTING POSITION: Any



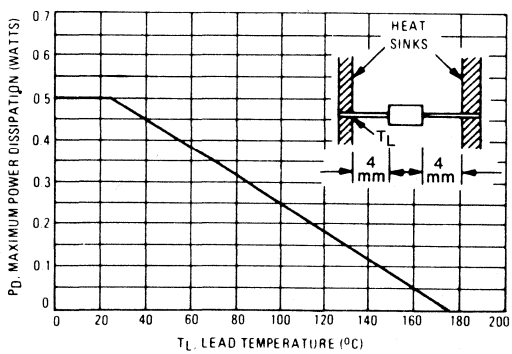
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	3.05	5.08	0.120	0.200
B	1.52	2.29	0.060	0.090
D	0.46	0.56	0.018	0.022
F		1.27	–	0.050
K	12.70		0.500	–

All JEDEC dimensions and notes apply.

CASE 299-01
DO-35

NOTE
1. POLARITY DENOTED BY CATHODE BAND
2. LEAD DIAMETER IS NOT CONTROLLED WITHIN DIMENSION "F"

FIGURE 1 – STEADY STATE POWER DERATING



ELECTRICAL CHARACTERISTICS (at T_L = 25 °C)

Motorola ZPD and BZX83C series. Forward Voltage V_F = 1V max at I_F = 50 mA.

Zener Voltage (Note 1) at I_{ZT} = 5 mA			Impedance (Ω) Max. (Note 2)		Typ. Temp. Coeff. at I_{ZT}	V_R min.	
Nominal	Min.	Max.	at I_{ZT}	at I_Z = 1 mA	%/o per °C	V	at I_R =
2.7	2.5	2.9	85	600	−0.09 . . . −0.04	1	100 μA
3.0	2.8	3.2	90	600	−0.09 . . . −0.03	1	60 μA
3.3	3.1	3.5	90	600	−0.08 . . . −0.03	1	30 μA
3.6	3.4	3.8	90	600	−0.08 . . . −0.03	1	20 μA
3.9	3.7	4.1	85	600	−0.07 . . . −0.03	1	10 μA
4.3	4.0	4.6	80	600	−0.06 . . . −0.01	1	5 μA
4.7	4.4	5.0	78	600	−0.05 . . . +0.02	1	2 μA
5.1	4.8	5.4	60	550	−0.03 . . . +0.04	0.8	100 nA
5.6	5.2	6.0	40	450	−0.02 . . . +0.06	1	100 nA
6.2	5.8	6.6	10	200	−0.01 . . . +0.07	2	100 nA
6.8	6.4	7.2	8	150	+0.02 . . . +0.07	3	100 nA
7.5	7.0	7.9	7	50	+0.03 . . . +0.07	5	100 nA
8.2	7.7	8.7	7	50	+0.04 . . . +0.07	6	100 nA
9.1	8.5	9.6	10	50	+0.05 . . . +0.08	7	100 nA
10	9.4	10.6	15	70	+0.05 . . . +0.08	7.5	100 nA
11	10.4	11.6	20	70	+0.05 . . . +0.09	8.5	100 nA
12	11.4	12.7	20	90	+0.06 . . . +0.09	9	100 nA
13	12.4	14.1	25	110	+0.07 . . . +0.09	10	100 nA
15	13.8	15.6	30	110	+0.07 . . . +0.09	11	100 nA
16	15.3	17.1	40	170	+0.08 . . . +0.095	12	100 nA
18	16.8	19.1	50	170	+0.08 . . . +0.10	14	100 nA
20	16.8	21.2	55	220	+0.08 . . . +0.10	15	100 nA
22	20.8	23.3	55	220	+0.08 . . . +0.10	17	100 nA
24	22.8	25.6	80	220	+0.08 . . . +0.10	18	100 nA
27	25.1	28.9	80	250	+0.08 . . . +0.10	20	100 nA
30	28.0	32.0	80	250	+0.08 . . . +0.10	22	100 nA
33	31.0	35.0	80	250	+0.08 . . . +0.10	24	100 nA

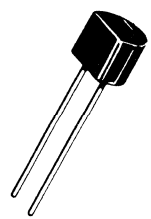
Note 1: Pulse test.
Note 2: f = 1 KHz, I_Z (ac) = 0.1 I_Z (dc).

SILICON HOT-CARRIER DIODE (SCHOTTKY BARRIER DIODE)

. . . designed primarily for UHF mixer applications but suitable also for use in detector and ultra-fast switching circuits. Supplied in an inexpensive plastic package for low-cost, high-volume consumer requirements.

- The Rugged Schottky Barrier Construction Provides Stable Characteristics by Eliminating the "Cat-Whisker" Contact
- Low Noise Figure – 7.0 dB Max @ 1.0 GHz
- Very Low Capacitance – Less Than 1.0 pF @ Zero Volts
- High Forward Conductance – 0.48 Volts (Typ) @ I_F = 10 mA

SILICON HOT-CARRIER UHF MIXER DIODE



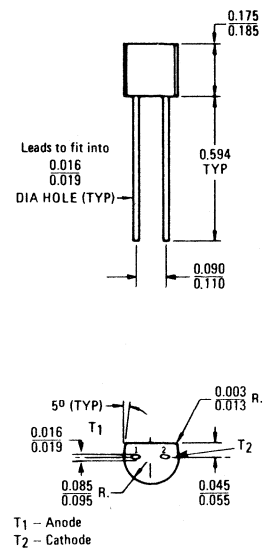
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	4.0	Volts
Forward Power Dissipation @ T_A = 25°C Derate above 25°C	P_F	280 2.8	mW mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μA)	$V_{(BR)R}$	4.0	5.0	–	Volts
Diode Capacitance (V_R = 0, f = 1.0 MHz, Note 1)	C_T	–	0.88	1.0	pF
Forward Voltage (I_F = 10 mA)	V_F*	–	0.48	0.60	Volts
Noise Figure (f = 1.0 GHz, Note 2)	NF	–	6.0	7.0	dB
Reverse Leakage (V_R = 3.0 V)	I_R	–	0.02	0.25	μA
Series Inductance (Note 3) (f = 250 MHz, Lead Length ≈ 1/16")	L_S	–	6.0	–	nH
Case Capacitance (Note 1) (f = 1.0 MHz, Lead Length ≈ 1/16")	C_C	–	0.18	–	pF

*Matched sets available. Contact Motorola Sales Office with specific requirements.



CASE 182-1

TYPICAL CHARACTERISTICS
(T_A = 25°C unless noted)

FIGURE 1 – REVERSE LEAKAGE

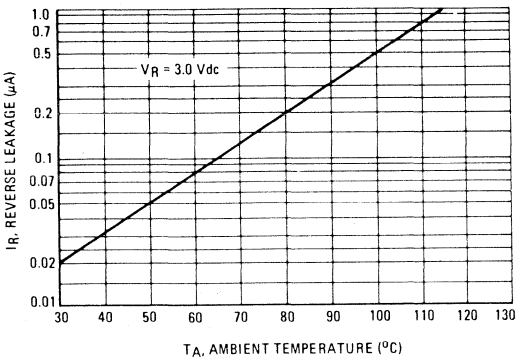


FIGURE 2 – FORWARD VOLTAGE

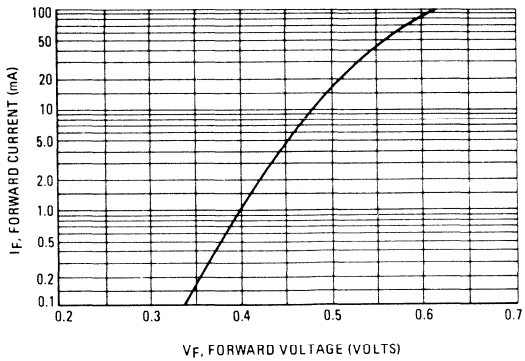


FIGURE 3 – CAPACITANCE

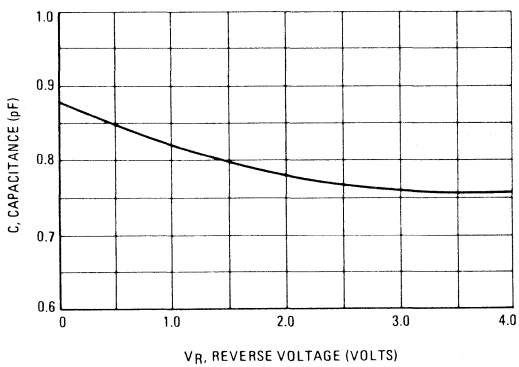


FIGURE 4 – NOISE FIGURE

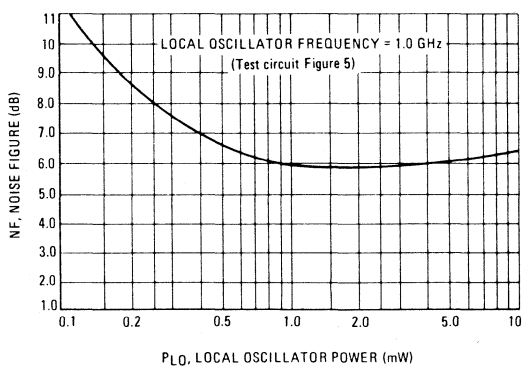
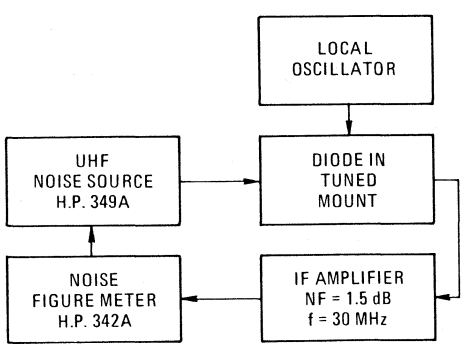


FIGURE 5 – NOISE FIGURE TEST CIRCUIT



NOTES ON TESTING AND SPECIFICATIONS

Note 1 – C_C and C_T are measured using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

Note 2 – Noise figure measured with diode under test in tuned diode mount using UHF noise source and local oscillator (LO) frequency of 1.0 GHz. The LO power is adjusted for 1.0 mW. IF amplifier NF = 1.5 dB, f = 30 MHz, see Figure 5.

Note 3 – L_S is measured on a package having a short instead of a die, using an impedance bridge (Boonton Radio Model 250A RX Meter).

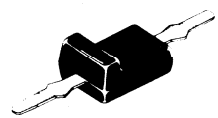
7

SILICON HOT-CARRIER DIODE (SCHOTTKY BARRIER DIODE)

. . . designed primarily for UHF mixer applications but suitable also for use in detector and ultra-fast switching circuits. Supplied in the low-inductance Mini-L package for low-cost, high-volume consumer requirements.

- The Rugged Schottky Barrier Construction Provides Stable Characteristics by Eliminating the "Cat-Whisker" Contact
- Low Noise Figure – 7.0 dB Max @ 1.0 GHz
- Very Low Capacitance – Less Than 1.0 pF @ Zero Volts
- High Forward Conductance – 0.48 volts (Typ) @ I_F = 10 mA
- Mini-L Ridge Clearly Identifies Cathode Lead for Easy Handling and Mounting

SILICON HOT-CARRIER UHF MIXER DIODE



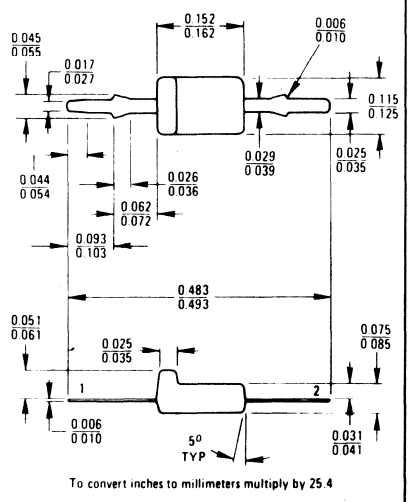
MAXIMUM RATINGS (T_J = 125°C unless otherwise noted)

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	4.0	Volts
Forward Power Dissipation @ T_A = 25°C Derate above 25°C	P_F	400 4.0	mW mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μA)	$V_{(BR)R}$	4.0	5.0	–	Volts
Diode Capacitance (V_R = 0, f = 1.0 MHz, Note 1)	C_T	–	0.8	1.0	pF
Forward Voltage (I_F = 10 mA)	V_F(1)	–	0.48	0.60	Volts
Noise Figure (f = 1.0 GHz, Note 2)	NF	–	6.0	7.0	dB
Reverse Leakage (V_R = 3.0 V)	I_R	–	0.02	0.25	μA
Series Inductance (Note 3) (f = 250 MHz, Measured at Lead Stop ≈ 1/8")	L_S	–	3.0	–	nH
Case Capacitance (Note 1) (f = 1.0 MHz)	C_C	–	0.1	–	pF

(1) Matched sets available. Contact Motorola Sales Office with specific requirements.



To convert inches to millimeters multiply by 25.4

Pin 1. Cathode
2. Anode

CASE 226

TYPICAL CHARACTERISTICS
(T_A = 25°C unless noted)

FIGURE 1 – REVERSE LEAKAGE

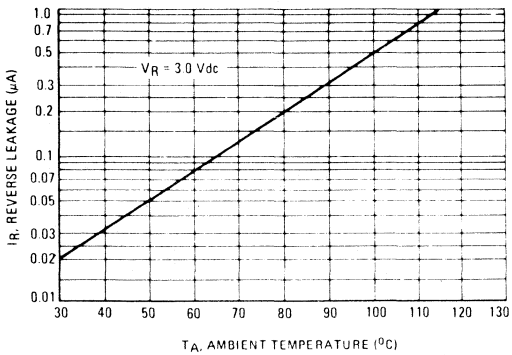


FIGURE 2 – FORWARD VOLTAGE

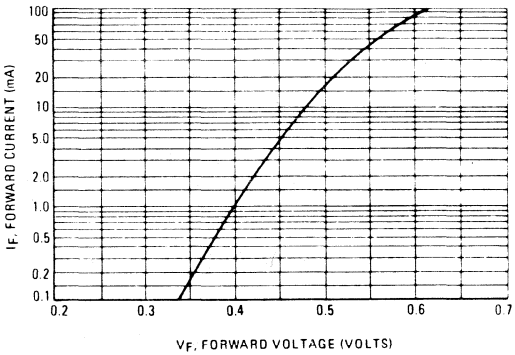


FIGURE 3 – DIODE CAPACITANCE

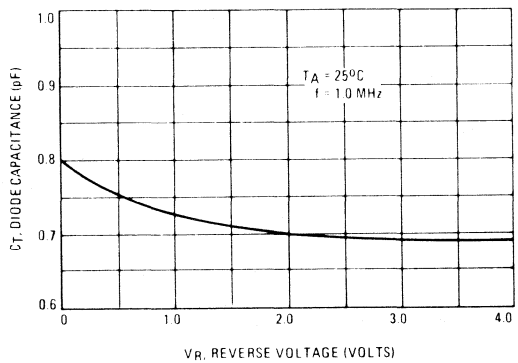


FIGURE 4 – NOISE FIGURE

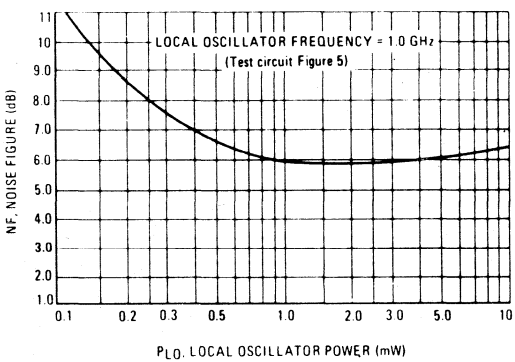
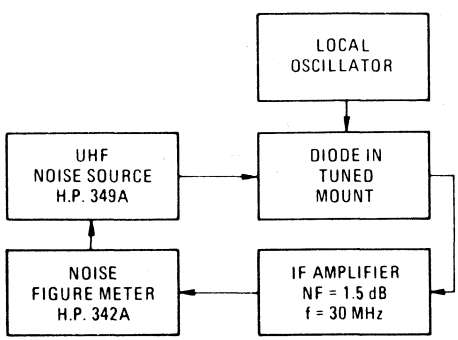


FIGURE 5 – NOISE FIGURE TEST CIRCUIT



NOTES ON TESTING AND SPECIFICATIONS

Note 1 C_C and C_T are measured using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

Note 2 Noise figure measured with diode under test in tuned diode mount using UHF noise source and local oscillator (LO) frequency of 1.0 GHz. The LO power is adjusted for 1.0 mW. IF amplifier NF = 1.5 dB, f = 30 MHz, see Figure 5.

Note 3 – L_S is measured on a package having a short instead of a die, using an impedance bridge (Boonton Radio Model 250A RX Meter).

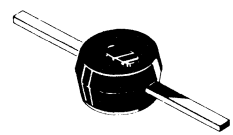
7

SILICON HOT-CARRIER MICRO-I▲ DIODE (SCHOTTKY BARRIER DIODE)

. . . designed primarily for UHF mixer applications but suitable also for use in detector and ultra-fast switching circuits.

- The Rugged Schottky Barrier Construction Provides Stable Characteristics by Eliminating the "Cat-Whisker" Contact
- Low Noise Figure – 7.0 dB Max @ 1.0 GHz
- Very Low Capacitance – Less Than 1.0 pF @ Zero Volts
- High Forward Conductance – 0.48 Volts (Typ) @ I_F = 10 mA
- Supplied in Space Saving Miniature Package

SILICON HOT-CARRIER UHF MIXER MICRO-I DIODE



Device Marked with Yellow Top.

MAXIMUM RATINGS

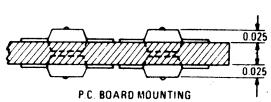
Rating	Symbol	Value	Unit
Reverse Voltage	V_R	4.0	Volts
Forward Power Dissipation @ T_A = 25°C Derate above 25°C	P_F	200 2.0	mW mW/°C
Operating Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μA)	$V_{(BR)R}$	4.0	5.0	–	Volts
Diode Capacitance (V_R = 0, f = 1.0 MHz, Note 1)	C_T	–	0.88	1.0	pF
Forward Voltage (I_F = 10 mA)	V_F(1)	–	0.48	0.60	Volts
Noise Figure (f = 1.0 GHz, Note 2)	NF	–	6.0	7.0	dB
Reverse Leakage (V_R = 3.0 V)	I_R	–	0.02	0.25	μA
Series Inductance (Note 3) (f = 250 MHz, Lead Length ≈ 1/16")	L_S	–	3.0	–	nH
Case Capacitance (Note 1) (f = 1.0 MHz, Lead Length ≈ 1/16")	C_C	–	0.15	–	pF

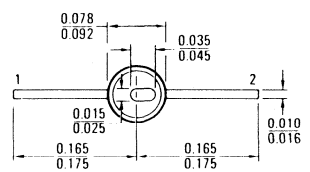
(1) Matched sets available. Contact Motorola Sales Office with specific requirements.

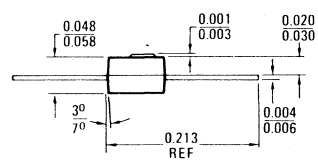
TYPICAL HIGH DENSITY MOUNTING TECHNIQUE



P.C. BOARD MOUNTING

Maximum Solder Temperature 250°C for 10s





STYLE 1:
PIN 1. ANODE
2. CATHODE

Optional Package with Raised Circular Tab Available; Specify Case 166-01.

CASE 166-02

▲Trademark of Motorola Inc.

TYPICAL CHARACTERISTICS
(T_A = 25°C unless noted)

FIGURE 1 – REVERSE LEAKAGE

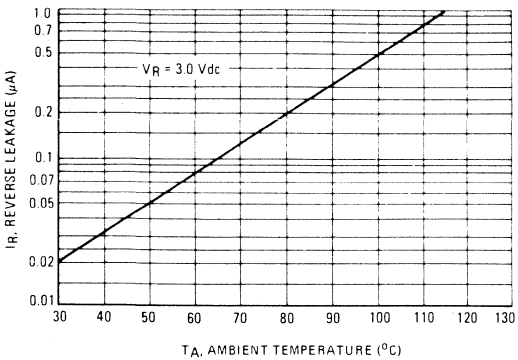


FIGURE 2 – FORWARD VOLTAGE

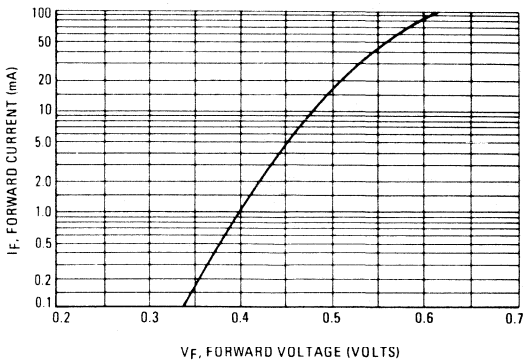


FIGURE 3 – CAPACITANCE

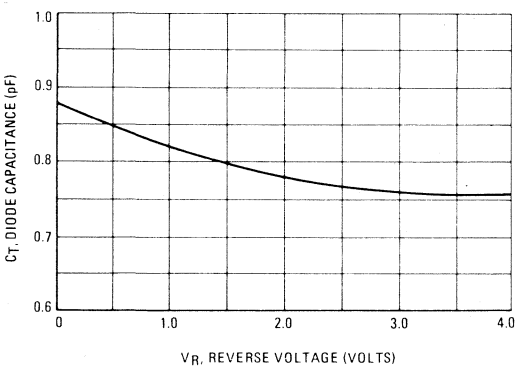


FIGURE 4 – NOISE FIGURE

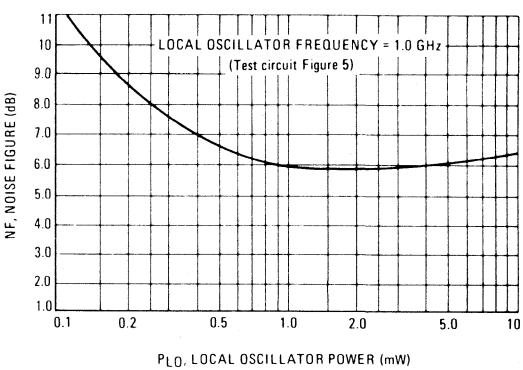
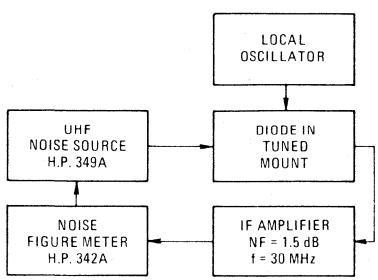


FIGURE 5 – NOISE FIGURE TEST CIRCUIT



NOTES ON TESTING AND SPECIFICATIONS

Note 1 – C_C and C_T are measured using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

Note 2 – Noise figure measured with diode under test in tuned diode mount using UHF noise source and local oscillator (LO) frequency of 1.0 GHz. The LO power is adjusted for 1.0 mW. IF amplifier NF = 1.5 dB, f = 30 MHz, see Figure 5.

Note 3 – L_S is measured on a package having a short instead of a die, using an impedance bridge (Boonton Radio Model 250A RX Meter).

1N5817 MBR115P
1N5818 MBR120P
1N5819 MBR130P
MBR140P

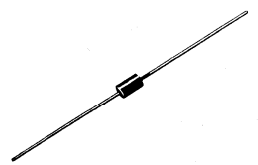
AXIAL LEAD RECTIFIERS

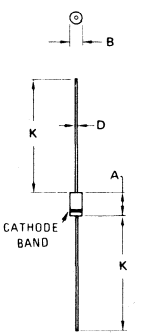
. . . employing the Schottky Barrier principle in a large area metal-to-silicon power diode. State-of-the-art geometry features epitaxial construction with oxide passivation and metal overlap contact. Ideally suited for use as rectifiers in low-voltage, high-frequency inverters, free wheeling diodes, and polarity protection diodes.

- Extremely Low v_F
- Low Stored Charge, Majority Carrier Conduction
- Low Power Loss/High Efficiency

SCHOTTKY BARRIER RECTIFIERS

1 AMPERE
15, 20, 30, 40 VOLTS





	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94	–	1.100	–

CASE 59-04

***MAXIMUM RATINGS**

Rating	Symbol	MBR115P	1N5817 MBR120P	1N5818 MBR130P	1N5819 MBR140P	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	15	20	30	40	V
Non-Repetitive Peak Reverse Voltage	V_{RSM}	15	24	36	48	V
RMS Reverse Voltage	$V_{R(RMS)}$	10	14	21	28	V
Average Rectified Forward Current (2) ($V_{R(equiv)} \leq 0.2\ V_{R(dc)}$, $T_L = 90^oC$, $R_{\theta JA} = 80^oC/W$, P.C. Board Mounting, see Note 2, $T_A = 55^oC$)	I_O	1.0				A
Ambient Temperature (Rated $V_R(dc)$, $P_{F(AV)} = 0$, $R_{\theta JA} = 80^oC/W$)	T_A	90	85	80	75	^oC
Non-Repetitive Peak Surge Current (Surge applied at rated load conditions, half-wave, single phase 60 Hz, $T_L = 70^oC$)	I_{FSM}	25 (for one cycle)				A
Operating and Storage Junction Temperature Range (Reverse Voltage applied)	T_J, T_{stg}	−65 to +125				^oC
Peak Operating Junction Temperature (Forward Current applied)	$T_{J(pk)}$	150				^oC

***THERMAL CHARACTERISTICS** (Note 2)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	80	$^oC/W$

***ELECTRICAL CHARACTERISTICS** ($T_L = 25^oC$ unless otherwise noted) (2)

Characteristic	Symbol	1N5817	1N5818	1N5819	MBR115P MBR120P MBR130P	MBR140P	Unit
Maximum Instantaneous Forward Voltage (1) ($i_F = 0.1$ A) ($i_F = 1.0$ A) ($i_F = 3.0$ A)	v_F	 0.320 0.450 0.750	 0.330 0.550 0.875	 0.340 0.600 0.900	 0.350 0.550 0.850	 0.350 0.600 0.900	V
Maximum Instantaneous Reverse Current @ Rated dc Voltage (1) ($T_L = 25^oC$) ($T_L = 100^oC$)	i_R	 1.0 10	 1.0 10	 1.0 10	 1.0 10	 1.0 10	mA

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.
(2) Lead Temperature reference is cathode lead 1/32" from case.
*Indicates JEDEC Registered Data for 1N5817-19.

MECHANICAL CHARACTERISTICS

CASE . . . . . Void free, transfer molded

FINISH . . . . . All external surfaces corrosion-resistant and the terminal leads are readily solderable

POLARITY . . . . . Cathode indicated by polarity band

MOUNTING POSITIONS . . . . . Any

SOLDERING . . . . . .220°C 1/16" from case for ten seconds

NOTE 1 – DETERMINING MAXIMUM RATINGS

Reverse power dissipation and the possibility of thermal runaway must be considered when operating this rectifier at reverse voltages above 0.1 V_{RWM}. Proper derating may be accomplished by use of equation (1).

$$T_{A(max)} = T_{J(max)} - R_{\theta JA}P_{F(AV)} - R_{\theta JA}P_{R(AV)} \quad (1)$$

where $T_{A(max)}$ = Maximum allowable ambient temperature
$T_{J(max)}$ = Maximum allowable junction temperature (125°C or the temperature at which thermal runaway occurs, whichever is lowest)
$P_{F(AV)}$ = Average forward power dissipation
$P_{R(AV)}$ = Average reverse power dissipation
$R_{\theta JA}$ = Junction-to-ambient thermal resistance

Figures 1, 2, and 3 permit easier use of equation (1) by taking reverse power dissipation and thermal runaway into consideration. The figures solve for a reference temperature as determined by equation (2).

$$T_R = T_{J(max)} - R_{\theta JA}P_{R(AV)} \quad (2)$$

Substituting equation (2) into equation (1) yields:

$$T_{A(max)} = T_R - R_{\theta JA}P_{F(AV)} \quad (3)$$

Inspection of equations (2) and (3) reveals that T_R is the ambient temperature at which thermal runaway occurs or where T_J = 125°C, when forward power is zero. The transition from one boundary condition to the other is evident on the curves of Figures 1, 2, and 3 as a difference in the rate of change of the slope in the vicinity of 115°C. The data of Figures 1, 2, and 3 is based upon dc conditions. For use in common rectifier circuits, Table 1 indicates suggested factors for an equivalent dc voltage to use for conservative design, that is:

$$V_{R(equiv)} = V_{in(PK)} \times F \quad (4)$$

The factor F is derived by considering the properties of the various rectifier circuits and the reverse characteristics of Schottky diodes.

EXAMPLE: Find $T_{A(max)}$ for 1N5818 operated in a 12-volt dc supply using a bridge circuit with capacitive filter such that I_{DC} = 0.4 A ($I_{F(AV)}$ = 0.5 A), $I_{(FM)}/I_{(AV)}$ = 10, Input Voltage = 10 $V_{(rms)}$, $R_{\theta JA}$ = 80°C/W.

Step 1. Find $V_{R(equiv)}$. Read F = 0.65 from Table 1,
$\therefore V_{R(equiv)} = (1.41)(10)(0.65) = 9.2$ V.

Step 2. Find T_R from Figure 2. Read T_R = 109°C
@ V_R = 9.2 V and $R_{\theta JA}$ = 80°C/W.

Step 3. Find $P_{F(AV)}$ from Figure 4. **Read $P_{F(AV)}$ = 0.5 W
@ $\frac{I_{(FM)}}{I_{(AV)}}$ = 10 and $I_{F(AV)}$ = 0.5 A.

Step 4. Find $T_{A(max)}$ from equation (3).
$T_{A(max)} = 109 - (80)(0.5) = 69$°C.

**Values given are for the 1N5818. Power is slightly lower for the 1N5817 because of its lower forward voltage, and higher for the 1N5819. Variations will be similar for the MBR-prefix devices, using $P_{F(AV)}$ from Figure 7.

TABLE 1 – VALUES FOR FACTOR F

Circuit	Half Wave		Full Wave, Bridge		Full Wave, Center Tapped*†	
Load	Resistive	Capacitive*	Resistive	Capacitive	Resistive	Capacitive
Sine Wave	0.5	1.3	0.5	0.65	1.0	1.3
Square Wave	0.75	1.5	0.75	0.75	1.5	1.5

*Note that $V_{R(PK)} \approx 2.0\ V_{in(PK)}$. †Use line to center tap voltage for V_{in}.

FIGURE 1 – MAXIMUM REFERENCE TEMPERATURE 1N5817/MBR115P/MBR120P

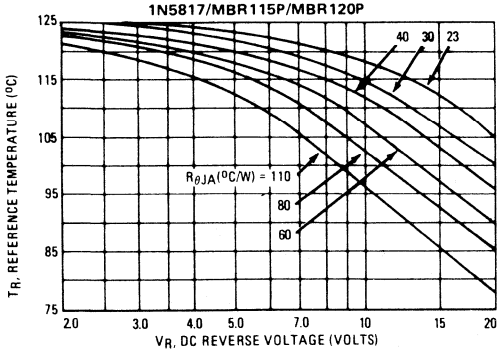


FIGURE 2 – MAXIMUM REFERENCE TEMPERATURE 1N5818/MBR130P

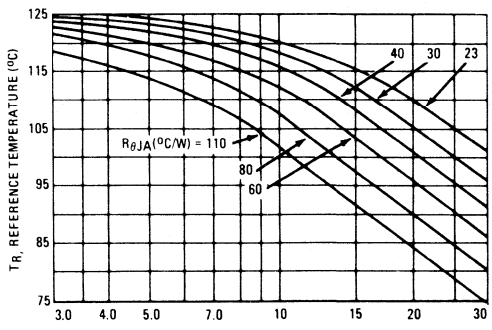


FIGURE 3 – MAXIMUM REFERENCE TEMPERATURE 1N5819/MBR140P

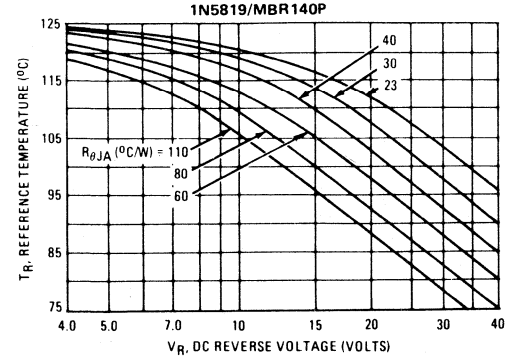
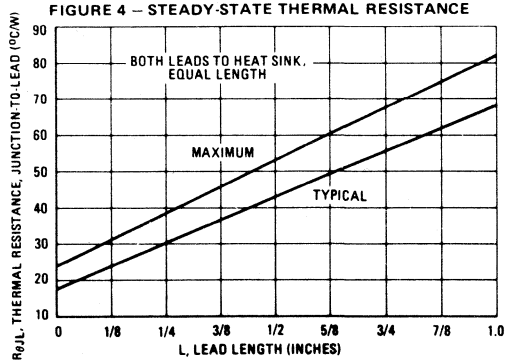


FIGURE 4 – STEADY-STATE THERMAL RESISTANCE



7

THERMAL CHARACTERISTICS

FIGURE 5 – THERMAL RESPONSE

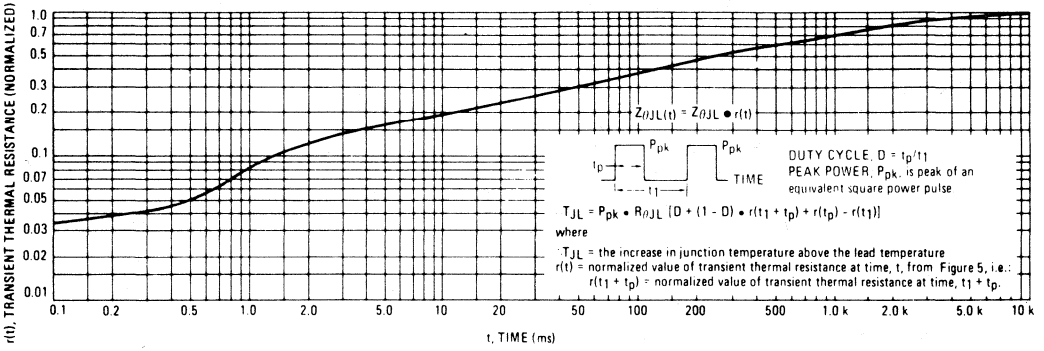


FIGURE 6 – FORWARD POWER DISSIPATION
1N5817-19

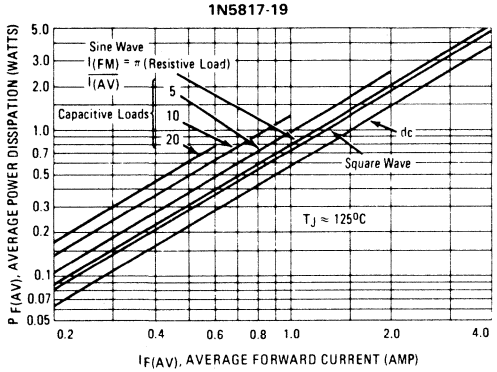
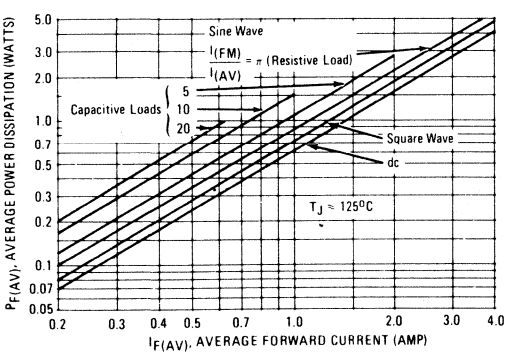


FIGURE 7 – FORWARD POWER DISSIPATION
MBR115P-140P



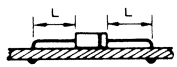
NOTE 2 – MOUNTING DATA

Data shown for thermal resistance junction-to-ambient ($R_{\theta JA}$) for the mountings shown is to be used as typical guideline values for preliminary engineering, or in case the tie point temperature cannot be measured.

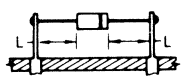
TYPICAL VALUES FOR $R_{\theta JA}$ IN STILL AIR

Mounting Method	Lead Length, L (in)				
	1/8	1/4	1/2	3/4	$R_{\theta JA}$
1	52	65	72	85	°C/W
2	67	80	87	100	°C/W
3		50			°C/W

Mounting Method 1
P.C. Board with 1-1/2" X 1-1/2" copper surface.

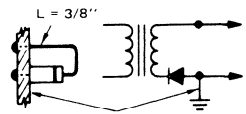


Mounting Method 2



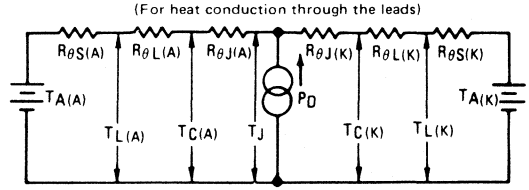
Vector Pin Mounting

Mounting Method 3
P.C. Board with 1-1/2" X 1-1/2" copper surface.



NOTE 3 – THERMAL CIRCUIT MODEL

(For heat conduction through the leads)



Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heat sink. Terms in the model signify:

T_A = Ambient Temperature
T_C = Case Temperature
T_L = Lead Temperature
T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_D = Power Dissipation

(Subscripts A and K refer to anode and cathode sides, respectively.) Values for thermal resistance components are:

$R_{\theta L}$ = 100°C/W/in typically and 120°C/W/in maximum
$R_{\theta J}$ = 36°C/W typically and 46°C/W maximum.

FIGURE 8 – TYPICAL FORWARD VOLTAGE

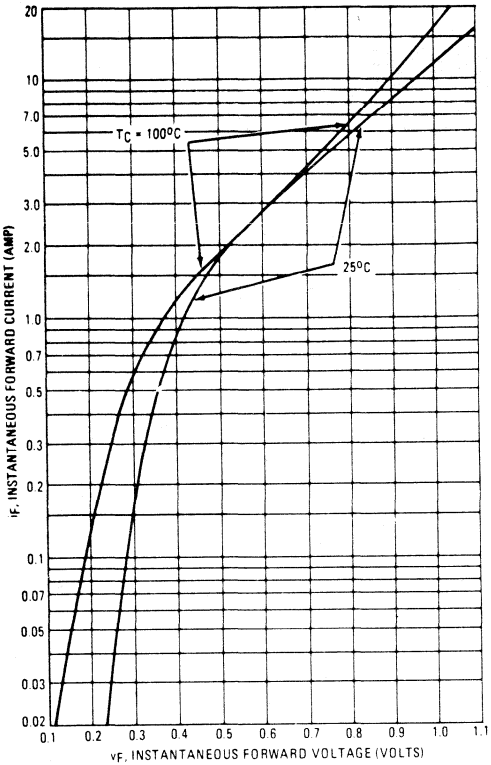


FIGURE 9 – MAXIMUM NON-REPETITIVE SURGE CURRENT

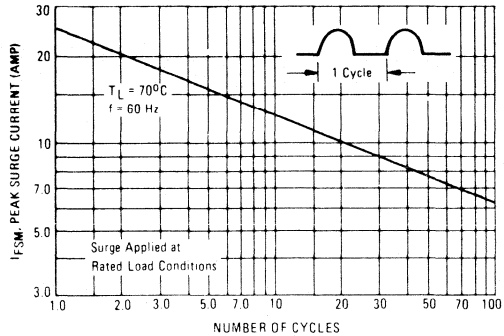


FIGURE 10 – TYPICAL REVERSE CURRENT

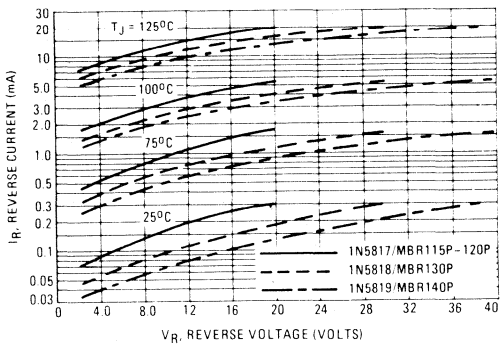
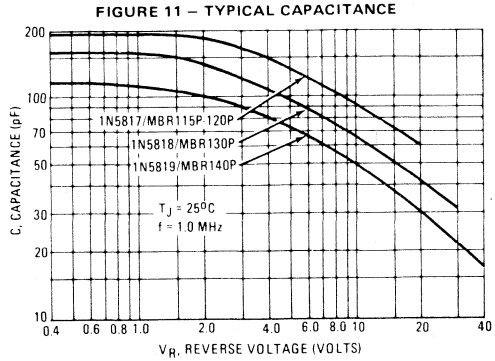


FIGURE 11 – TYPICAL CAPACITANCE



NOTE 4 – HIGH FREQUENCY OPERATION

Since current flow in a Schottky rectifier is the result of majority carrier conduction, it is not subject to junction diode forward and reverse recovery transients due to minority carrier injection and stored charge. Satisfactory circuit analysis work may be performed by using a model consisting of an ideal diode in parallel with a variable capacitance. (See Figure 11.)

Rectification efficiency measurements show that operation will be satisfactory up to several megahertz. For example, relative waveform rectification efficiency is approximately 70 per cent at 2.0 MHz, e.g., the ratio of dc power to RMS power in the load is 0.28 at this frequency, whereas perfect rectification would yield 0.406 for sine wave inputs. However, in contrast to ordinary junction diodes, the loss in waveform efficiency is not indicative of power loss: it is simply a result of reverse current flow through the diode capactiance, which lowers the dc output voltage.

1N5820 MBR320P
1N5821 MBR330P
1N5822 MBR340P

Designers Data Sheet

AXIAL LEAD RECTIFIERS

. . . employing the Schottky Barrier principle in a large area metal-to-silicon power diode. State-of-the-art geometry features epitaxial construction with oxide passivation and metal overlap contact. Ideally suited for use as rectifiers in low-voltage, high-frequency inverters, free wheeling diodes, and polarity protection diodes.

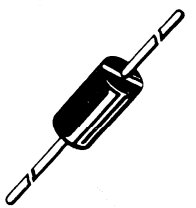
- Extremely Low v_F
- Low Power Loss/High Efficiency
- Low Stored Charge, Majority Carrier Conduction

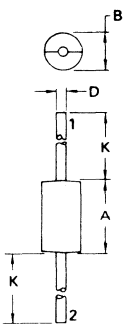
Designer's Data for Worst-Case Conditions

The Designers Data sheets permit the design of most circuits entirely from the information presented. Limit curves—representing boundaries on device characteristics—are given to facilitate worst-case design.

SCHOTTKY BARRIER RECTIFIERS

3.0 AMPERES
20, 30, 40 VOLTS





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.65	0.370	0.380
B	4.83	5.33	0.190	0.210
D	1.22	1.32	0.048	0.052
K	26.97	27.23	1.062	1.072

CASE 267-01

*MAXIMUM RATINGS

Rating	Symbol	1N5820 MBR320P	1N5821 MBR330P	1N5822 MBR340P	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	20	30	40	V
Non-Repetitive Peak Reverse Voltage	V_{RSM}	24	36	48	V
RMS Reverse Voltage	$V_{R(RMS)}$	14	21	28	V
Average Rectified Forward Current (2) $V_{R(equiv)} \leq 0.2\ V_{R(dc)}$, $T_L = 95^oC$ ($R_{\theta JA} = 28^oC/W$, P.C. Board Mounting, see Note 2)	I_O	3.0			A
Ambient Temperature Rated $V_{R(dc)}$, $P_{F(AV)} = 0$ $R_{\theta JA} = 28^oC/W$	T_A	90	85	80	°C
Non-Repetitive Peak Surge Current (Surge applied at rated load conditions, half wave, single phase 60 Hz, $T_L = 75^oC$)	I_{FSM}	80 (for one cycle)			A
Operating and Storage Junction Temperature Range (Reverse Voltage applied)	T_J, T_{stg}	−65 to +125			°C
Peak Operating Junction Temperature (Forward Current Applied)	$T_{J(pk)}$	150			°C

*THERMAL CHARACTERISTICS (Note 2)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	28	°C/W

*ELECTRICAL CHARACTERISTICS ($T_L = 25^oC$ unless otherwise noted) (2)

Characteristic	Symbol	1N5820	1N5821	1N5822	MBR---P	Unit
Maximum Instantaneous Forward Voltage (1)	v_F					V
(i_F = 1.0 Amp)		0.370	0.380	0.390	0.400	
(i_F = 3.0 Amp)		0.475	0.500	0.525	0.550	
(i_F = 9.4 Amp)		0.850	0.900	0.950	0.950	
Maximum Instantaneous Reverse Current @ Rated dc Voltage (1)	i_R					mA
$T_L = 25^oC$		2.0	2.0	2.0	2.0	
$T_L = 100^oC$		20	20	20	20	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.
(2) Lead Temperature reference is cathode lead 1/32" from case.
*Indicates JEDEC Registered Data for 1N5820-22.

MECHANICAL CHARACTERISTICS

CASE . . . . . Void free, transfer molded
FINISH . . . . . All external surfaces corrosion-resistant and the terminal leads are readily solderable
POLARITY . . . . . Cathode indicated by polarity band
MOUNTING POSITIONS . . . . . Any
SOLDERING . . . . . 220°C 1/16" from case for ten seconds

NOTE 1 – DETERMINING MAXIMUM RATINGS

Reverse power dissipation and the possibility of thermal runaway must be considered when operating this rectifier at reverse voltages above 0.1 V_{RWM}. Proper derating may be accomplished by use of equation (1).

$$T_{A(max)} = T_{J(max)} - R_{\theta JA}P_{F(AV)} - R_{\theta JA}P_{R(AV)} \quad (1)$$

where $T_{A(max)}$ = Maximum allowable ambient temperature
$T_{J(max)}$ = Maximum allowable junction temperature (125°C or the temperature at which thermal runaway occurs, whichever is lowest)
$P_{F(AV)}$ = Average forward power dissipation
$P_{R(AV)}$ = Average reverse power dissipation
$R_{\theta JA}$ = Junction-to-ambient thermal resistance

Figures 1, 2, and 3 permit easier use of equation (1) by taking reverse power dissipation and thermal runaway into consideration. The figures solve for a reference temperature as determined by equation (2).

$$T_R = T_{J(max)} - R_{\theta JA}P_{R(AV)} \quad (2)$$

Substituting equation (2) into equation (1) yields:

$$T_{A(max)} = T_R - R_{\theta JA}P_{F(AV)} \quad (3)$$

Inspection of equations (2) and (3) reveals that T_R is the ambient temperature at which thermal runaway occurs or where T_J = 125°C, when forward power is zero. The transition from one boundary condition to the other is evident on the curves of Figures 1, 2, and 3 as a difference in the rate of change of the slope in the vicinity of 115°C. The data of Figures 1, 2, and 3 is based upon dc conditions. For use in common rectifier circuits, Table 1 indicates suggested factors for an equivalent dc voltage to use for conservative design, that is:

$$V_{R(equiv)} = V_{(FM)} \times F \quad (4)$$

The factor F is derived by considering the properties of the various rectifier circuits and the reverse characteristics of Schottky diodes.

EXAMPLE: Find $T_{A(max)}$ for 1N5821 operated in a 12-volt dc supply using a bridge circuit with capacitive filter such that I_{DC} = 2.0 A ($I_{F(AV)}$ = 1.0 A), $I_{(FM)}/I_{(AV)}$ = 10, Input Voltage = 10 $V_{(rms)}$, $R_{\theta JA}$ = 40°C/W.

Step 1. Find $V_{R(equiv)}$. Read F = 0.65 from Table 1,
$\therefore V_{R(equiv)} = (1.41)(10)(0.65) = 9.2$ V.

Step 2. Find T_R from Figure 2. Read T_R = 108°C
@ V_R = 9.2 V and $R_{\theta JA}$ = 40°C/W.

Step 3. Find $P_{F(AV)}$ from Figure 6. **Read $P_{F(AV)}$ = 0.85 W
@ $\frac{I_{(FM)}}{I_{(AV)}}$ = 10 and $I_{F(AV)}$ = 1.0 A.

Step 4. Find $T_{A(max)}$ from equation (3).
$T_{A(max)} = 108 - (0.85)(40) = 74°C$.

**Values given are for the 1N5821. Power is slightly lower for the 1N5820 because of its lower forward voltage, and higher for the 1N5822. Variations will be similar for the MBR-prefix devices, using $P_{F(AV)}$ from Figure 7.

TABLE 1 – VALUES FOR FACTOR F

Circuit	Half Wave		Full Wave, Bridge		Full Wave, Center Tapped*†	
Load	Resistive	Capacitive*	Resistive	Capacitive	Resistive	Capacitive
Sine Wave	0.5	1.3	0.5	0.65	1.0	1.3
Square Wave	0.75	1.5	0.75	0.75	1.5	1.5

*Note that $V_{R(PK)} \approx 2.0\ V_{in(PK)}$. †Use line to center tap voltage for V_{in}.

FIGURE 1 – MAXIMUM REFERENCE TEMPERATURE 1N5820/MBR320P

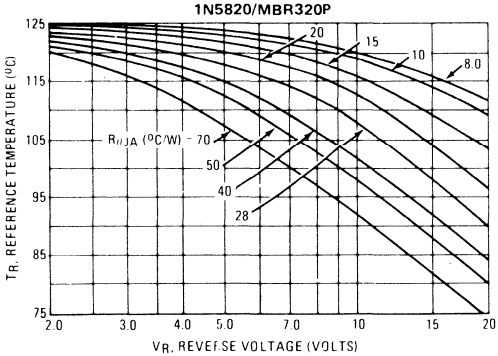


FIGURE 2 – MAXIMUM REFERENCE TEMPERATURE 1N5821/MBR330P

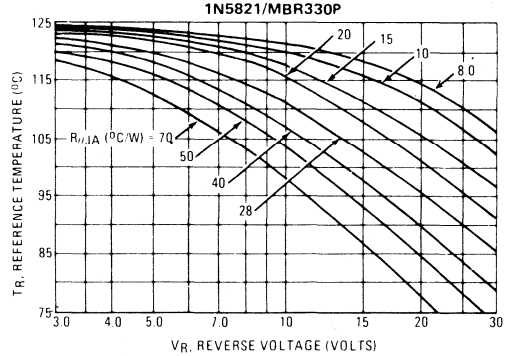


FIGURE 3 – MAXIMUM REFERENCE TEMPERATURE 1N5822/MBR340P

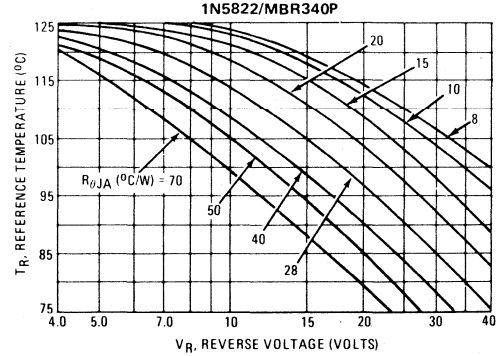
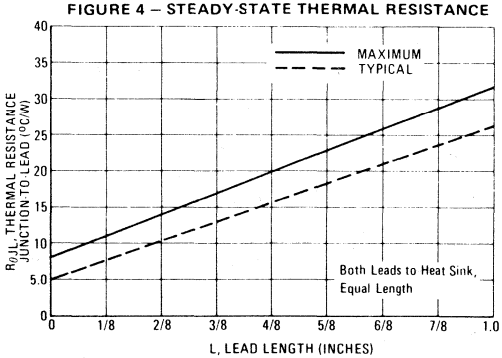


FIGURE 4 – STEADY-STATE THERMAL RESISTANCE



7

FIGURE 5 – THERMAL RESPONSE

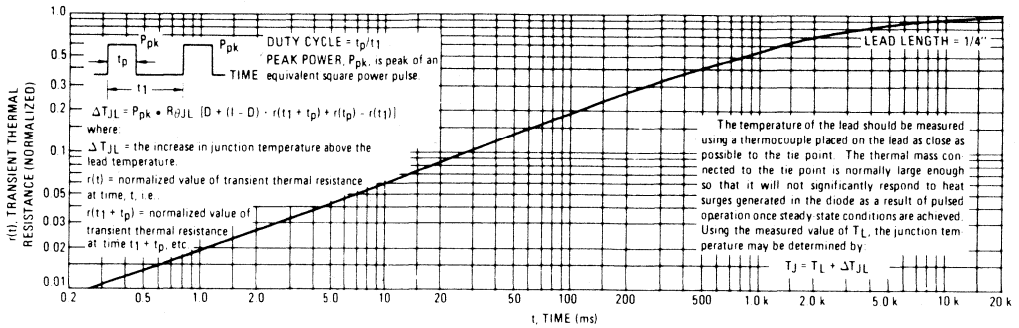


FIGURE 6 – FORWARD POWER DISSIPATION
1N5820-22

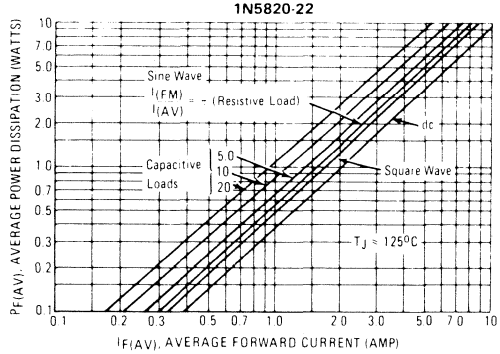
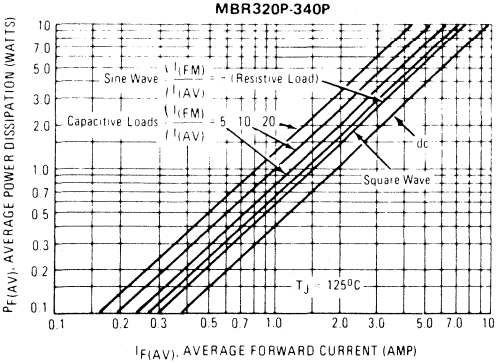


FIGURE 7 – FORWARD POWER DISSIPATION
MBR320P-340P



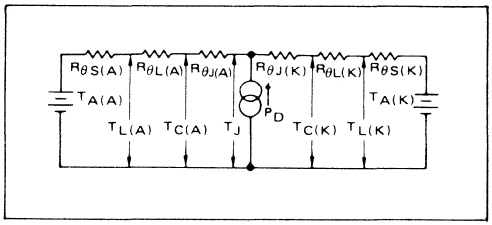
NOTE 2 – MOUNTING DATA

Data shown for thermal resistance junction-to-ambient ($R_{\theta}JA$) for the mountings shown is to be used as typical guideline values for preliminary engineering, or in case the tie point temperature cannot be measured.

TYPICAL VALUES FOR $R_{\theta JA}$ IN STILL AIR

Mounting Method	Lead Length, L (in)				$R_{\theta JA}$
	1/8	1/4	1/2	3/4	
1	50	51	53	55	°C/W
2	58	59	61	63	°C/W
3	28				°C/W

NOTE 3 – APPROXIMATE THERMAL CIRCUIT MODEL



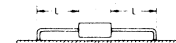
Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heat sink. Terms in the model signify:

T_A = Ambient Temperature T_C = Case Temperature
T_L = Lead Temperature T_J = Junction Temperature
$R_{\theta}S$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta}L$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta}J$ = Thermal Resistance, Junction to Case
P_D = Total Power Dissipation = $P_F + P_R$
P_F = Forward Power Dissipation
P_R = Reverse Power Dissipation
(Subscripts (A) and (K) refer to anode and cathode sides, respectively.) Values for thermal resistance components are:
$R_{\theta}L$ = 42°C/W/in typically and 48°C/W/in maximum
$R_{\theta}J$ = 10°C/W typically and 16°C/W maximum
The maximum lead temperature may be found as follows:

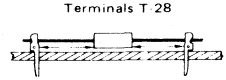
$$T_L = T_{J(max)} - \Delta T_{JL}$$

where $\Delta T_{JL} \approx R_{\theta JL} \cdot P_D$

Mounting Method 1
P.C. Board where available copper surface is small.



Mounting Method 2
Vector Push-In Terminals T-28



Mounting Method 3
P.C. Board with with 2 1/2" X 2-1/2" copper surface.

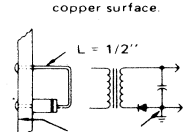


FIGURE 8 – TYPICAL FORWARD VOLTAGE

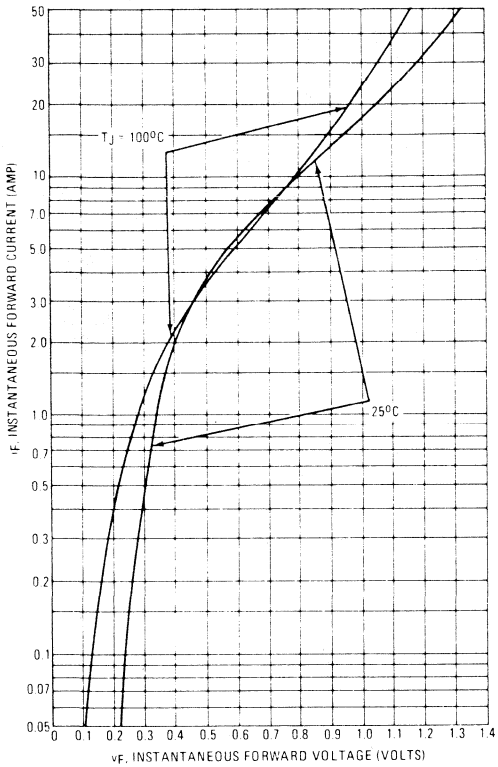


FIGURE 9 – MAXIMUM NON-REPETITIVE SURGE CURRENT

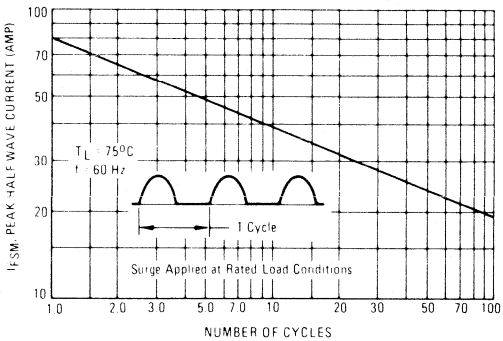


FIGURE 10 – TYPICAL REVERSE CURRENT

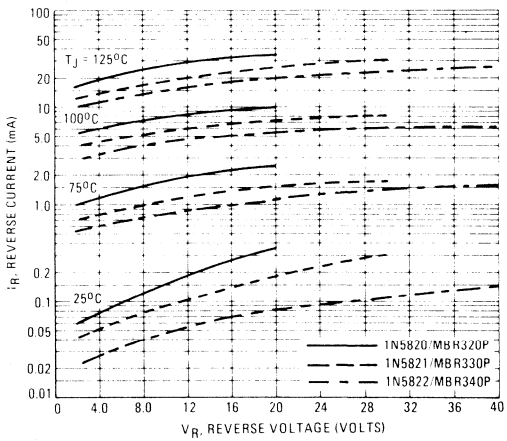
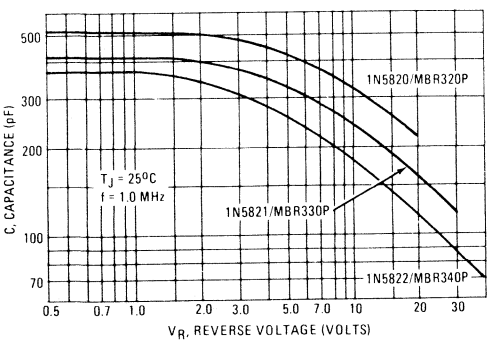


FIGURE 11 – TYPICAL CAPACITANCE



NOTE 4 – HIGH FREQUENCY OPERATION

Since current flow in a Schottky rectifier is the result of majority carrier conduction, it is not subject to junction diode forward and reverse recovery transients due to minority carrier injection and stored charge. Satisfactory circuit analysis work may be performed by using a model consisting of an ideal diode in parallel with a variable capacitance. (See Figure 11.)

7

3N253 thru 3N259
(MDA200 Series)

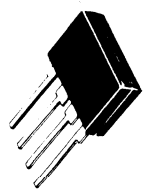
MINIATURE INTEGRAL DIODE ASSEMBLIES

. . . with silicon rectifier chips interconnected and encapsulated into voidless rectifier bridge circuits.

- High Resistance to Shock and Vibration
- High Dielectric Strength
- Built-In Printed Circuit Board Stand-Offs

SINGLE-PHASE
FULL-WAVE BRIDGE

2.0 AMPERES
50-1000 VOLTS



MAXIMUM RATINGS Rating (Per Diode)	Symbol	3N253 MDA200	3N254 MDA201	3N255 MDA202	3N256 MDA204	3N257 MDA206	3N258 MDA208	3N259 MDA210	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	400	600	800	1000	Volts
DC Output Voltage Resistive Load Capacitive Load	 Vdc Vdc	 32 50	 64 100	 127 200	 255 400	 382 600	 510 800	 640 1000	 Volts Volts
Sine Wave RMS Input Voltage	$V_{R(RMS)}$	35	70	140	280	420	560	700	Volts
Average Rectified Forward Current (single phase bridge operation, resistive load, 60 Hz, T_A = 55°C)	I_O	2.0							Amp
Non-Repetitive Peak Surge Current (Preceded and followed by rated current and voltage, T_A = 55°C)	I_{FSM}	60 (for 1 cycle)							Amp
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +165							°C

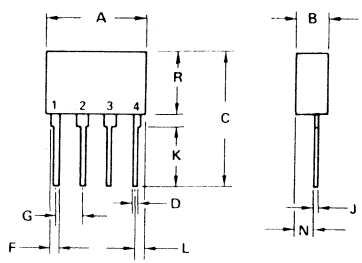
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Instantaneous Forward Voltage (Per Diode) (i_F = 3.14 Amp, T_J = 25°C)	v_F	1.0	1.1	Volts
Reverse Current (Per Diode) (Rated V_R, T_A = 25°C) (Rated V_R, T_A = 100°C)	I_R	 – –	 10 100	μA

MECHANICAL CHARACTERISTICS

CASE: Transfer Molded Plastic
POLARITY: Terminal designation on case
(+) for DC output
(-) for DC output
(AC) for AC input

MOUNTING POSITION: Any
WEIGHT: 1.8 grams (approx)
TERMINALS: Readily solderable connections, corrosion resistant.



STYLE 1:
TERM 1. POS
2. AC
3. AC
4. NEG

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.99	15.49	0.590	0.610
B	4.57	5.08	0.180	0.200
C	–	20.57	–	0.810
D	0.76	1.02	0.030	0.040
F	1.02	1.27	0.040	0.050
G	3.68	3.94	0.145	0.155
J	0.56	0.71	0.022	0.028
K	–	9.02	–	0.355
L	1.78	2.03	0.070	0.080
N	2.54	2.79	0.100	0.110
R	9.40	10.03	0.370	0.395

CASE 312-02

MAXIMUM RATINGS, BRIDGE OPERATION

FIGURE 1 – CURRENT DERATING

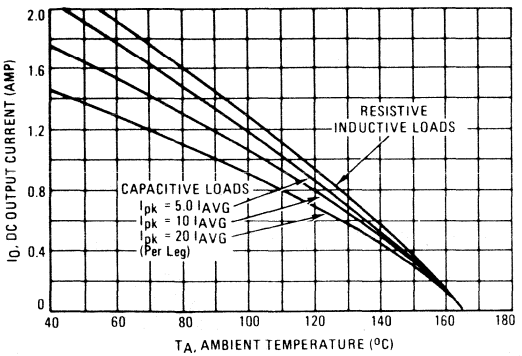


FIGURE 2 – POWER DISSIPATION

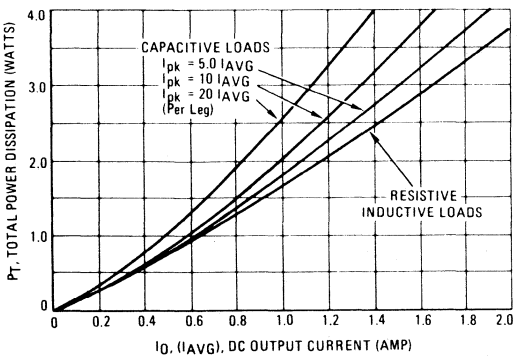
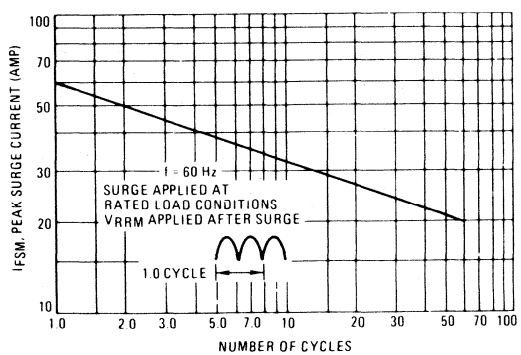


FIGURE 3 – SURGE CURRENT



SINGLE DIODE CHARACTERISTICS

FIGURE 4 – MAXIMUM FORWARD VOLTAGE

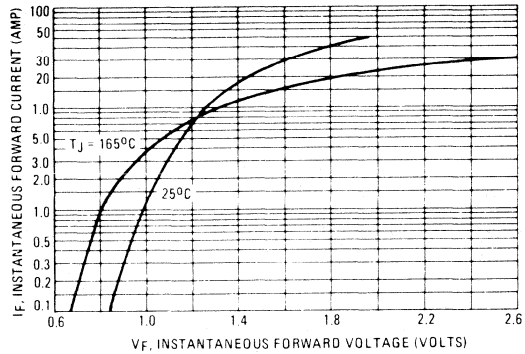


FIGURE 5 – FORWARD RECOVERY TIME

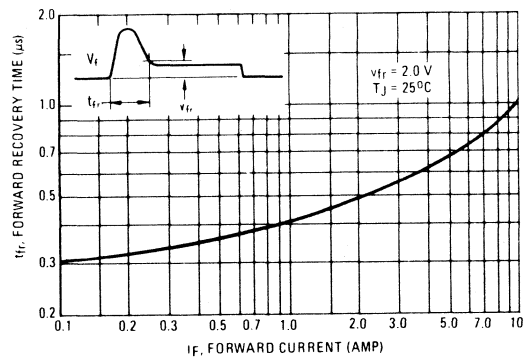
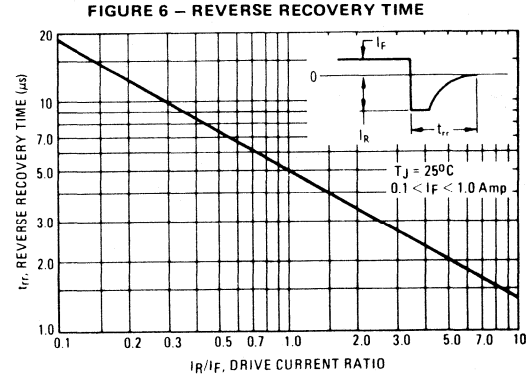


FIGURE 6 – REVERSE RECOVERY TIME



7

Designers Data Sheet

MINIATURE INTEGRAL DIODE ASSEMBLIES

. . . passivated, diffused-silicon dice interconnected and transfer molded into voidless hybrid rectifier circuit assemblies.

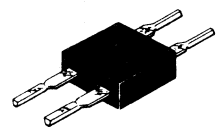
- Large Inrush Surge Capability – 45 A (For 1.0 Cycle)
- Efficient Thermal Management Provides Maximum Power Handling in Minimum Space

Designers Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit curves – representing boundaries on device characteristics – are given to facilitate "worst case" design.

SINGLE-PHASE FULL-WAVE BRIDGE

1.5 AMPERES
25–1000 VOLTS



MAXIMUM RATINGS

Rating (Per Leg)	Symbol	A1	A2	A3	A4	A5	A6	A7	A8	A9	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	25	50	100	200	300	400	600	800	1000	Volts
DC Output Voltage Resistive Load Capacitative Load	 Vdc Vdc	15 25	30 50	62 100	124 200	185 300	250 400	380 600	500 800	620 1000	 Volts Volts
Sine Wave RMS Input Voltage	$V_{R(RMS)}$	18	35	70	140	210	280	420	560	700	Volts
Average Rectified Forward Current (single phase bridge resistive load, 60 Hz, see Figure 6, $T_A = 50^oC$	I_O	1.5									Amp
Non-Repetitive Peak Surge Current, (see Figure 2) rated load, $T_J = 175^oC$	I_{FSM}	45 for 1 cycle									Amp
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +175									^oC

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Maximum Instantaneous Forward Voltage Drop (Per Leg) (I_F = 2.4 Amp, $T_J = 25^oC$) Figure 1	V_F	1.2	Volts
Maximum Reverse Current (Rated dc Voltage across ac terminals, $T_J = 25^oC$)	I_R	20	μA

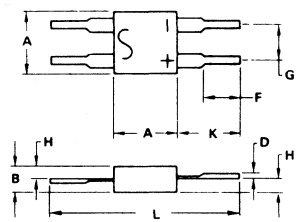
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Effective Bridge Thermal Resistance, Junction to Ambient (Full-Wave Bridge Operation, Typical Printed Circuit Board Mounting)	$R_{\theta JA}$	50	$^oC/W$

MECHANICAL CHARACTERISTICS

CASE: Transfer-molded plastic encapsulation.
POLARITY: Terminal-designation embossed on case +DC output
-DC output
~AC input

MOUNTING POSITION: Any
WEIGHT: 1.0 gram (approx)
TERMINALS: Readily solderable connections, corrosion resistant.



NOTES:
1. LEAD DIM "D" TO BE MEASURED WITHIN "F"
2. LEADS FORMED TO FIT INTO HOLE 0.94 mm (0.037) MIN.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	6.10	6.73	0.240	0.265
B	2.29	2.79	0.090	0.110
D	0.51	0.94	0.020	0.037
F	3.56	6.35	0.140	0.250
G	3.68	3.94	0.145	0.155
H	1.02	1.27	0.040	0.050
K	6.60	10.16	0.260	0.400
L	19.30	27.05	0.760	1.065

CASE 109-03

▲Trademark of Motorola Inc.

FIGURE 1 – FORWARD VOLTAGE (PER LEG)

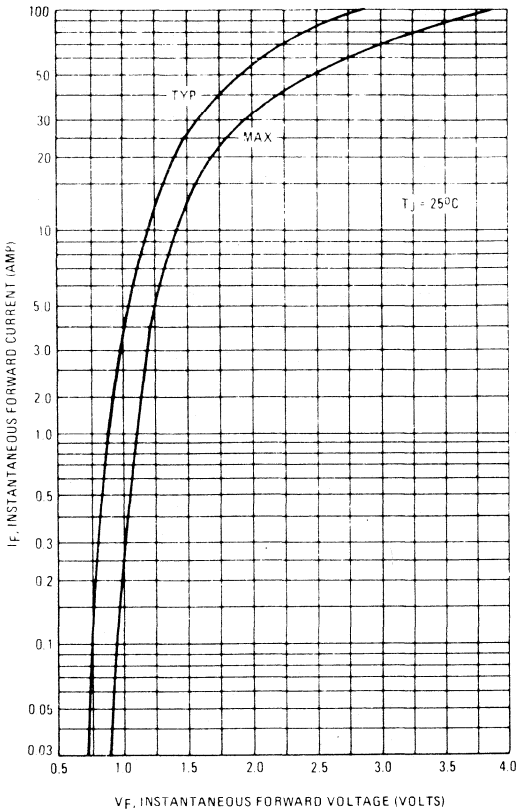


FIGURE 2 – MAXIMUM SURGE CAPABILITY

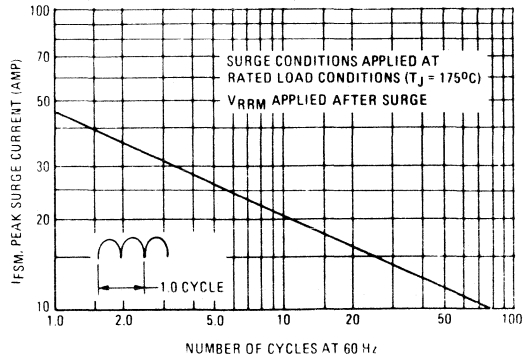


FIGURE 3 – FORWARD VOLTAGE TEMPERATURE COEFFICIENT

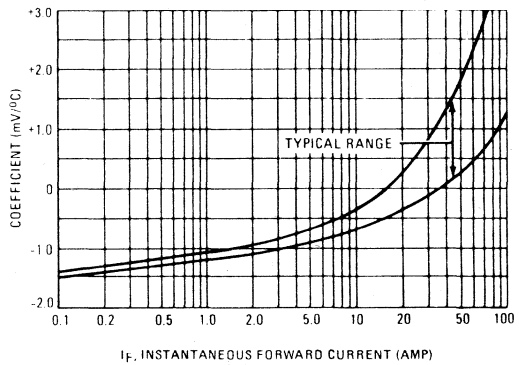


FIGURE 4 – TYPICAL THERMAL RESPONSE

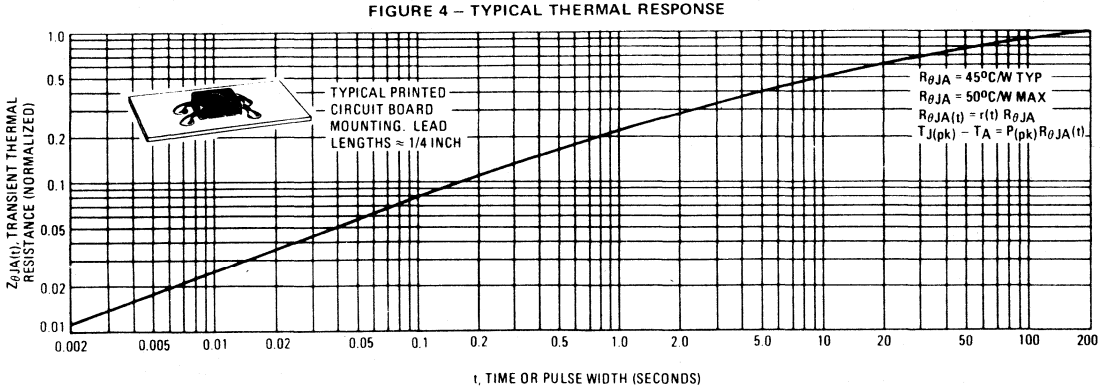


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FIGURE 5 – POWER DISSIPATION

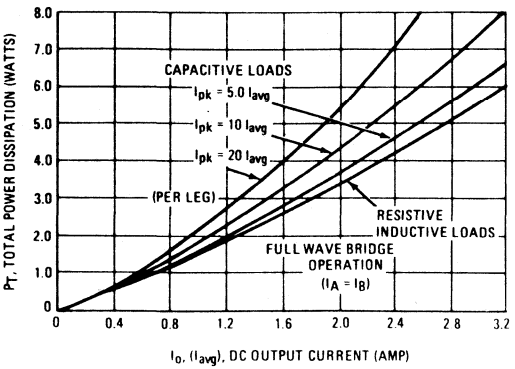


FIGURE 6 – CURRENT DERATING

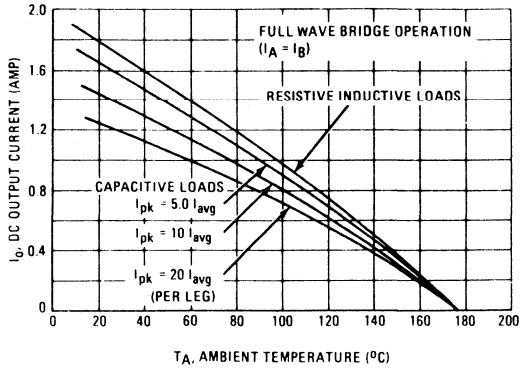
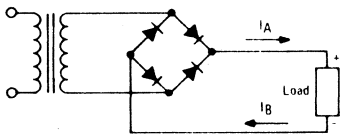
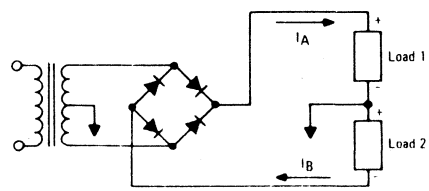


FIGURE 7 – BASIC CIRCUIT USES FOR BRIDGE RECTIFIERS



CIRCUIT A



CIRCUIT B

APPLICATION NOTE

The Data of Figure 4 applies for typical wire terminal or printed circuit board mounting conditions in still air. Under these or similar conditions, the thermal resistance between the diode junctions and the leads at the edge of the case is a small fraction of the thermal resistance from junction to ambient. Consequently, the lead temperature is very close to the junction temperature. Therefore, it is recommended that the lead temperature be measured when the diodes are operating in prototype equipment, in order to determine if operation is within the diode temperature ratings. The lead having the highest thermal resistance to the ambient will yield readings closest to the junction temperature. By measuring temperature as outlined, variations of junction to ambient thermal resistance, caused by the amount of surface area of the terminals or printed circuit board and the degree of air convection, as well as proximity of other heat sources cease to be important design considerations.

Bridge rectifiers are used in two basic circuit configurations as shown by circuits A and B of Figure 7. The current derating data of Figure 6 applies to the standard bridge circuit (A), where $I_A = I_B$. The derating data considers the thermal response of the junction and is based upon the criteria that the junction temperature must not exceed rated $T_{J(max)}$ when peak reverse voltage is applied. However, because of the slow thermal response and the close thermal coupling between the individual semiconductor die in the MDA920A assembly, the maximum ambient temperature is given closely by

$$T_A = T_{J(max)} - R_{\theta JA} P_T$$

where P_T is the total average power dissipation in the assembly.

For the circuit of Figure B, use of the above formula will yield suitable rating information. For example to determine $T_{A(max)}$ for the conditions:

I_A = 0.5 A, I_{pk} = 10 I_{avg}
I_B = 1.0 A, I_{pk} = 18 I_{avg}

From Figure 5: For I_A, read $P_{TA} \approx 0.8$ W
For I_B, read $P_{TB} \approx 2.2$ W

$P_T = (P_{TA} + P_{TB}) \div 2 = 1.5$ W

(Division by 2 is necessary as data from Figure 5 is for full-wave bridge operation.) $\therefore T_{A(max)} = 175^o - (50)\ (1.5) = 100^oC$.

FIGURE 8 – FORWARD RECOVERY TIME

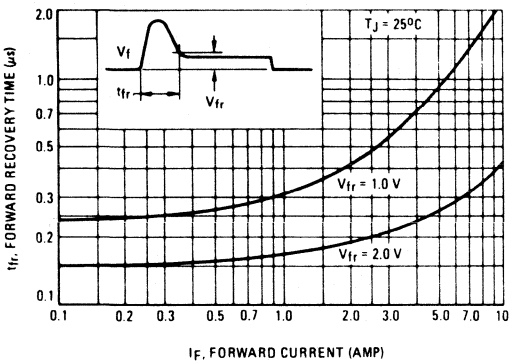


FIGURE 9 – REVERSE RECOVERY TIME

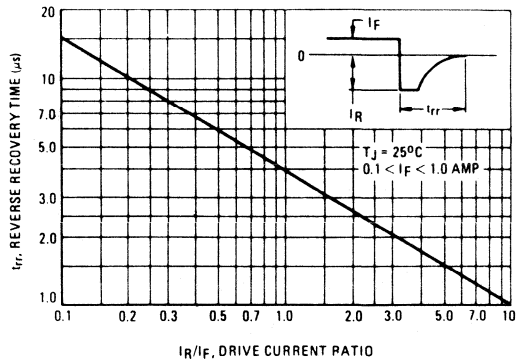


FIGURE 10 – RECTIFICATION WAVEFORM EFFICIENCY

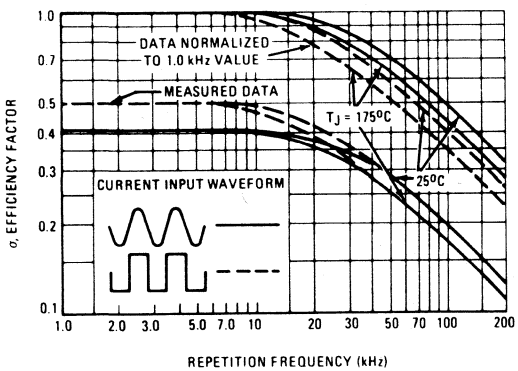
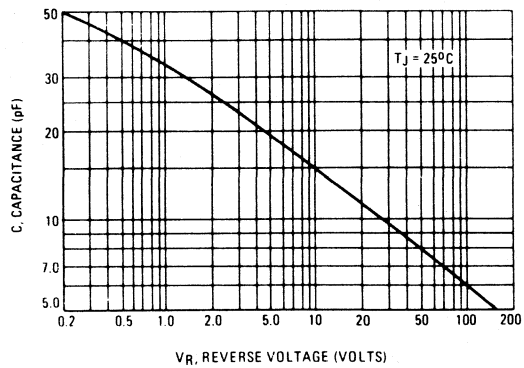
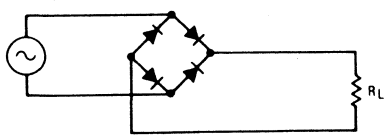


FIGURE 11 – CAPACITANCE



RECTIFIER EFFICIENCY NOTE

FIGURE 12 – SINGLE-PHASE FULL-WAVE BRIDGE RECTIFIER CIRCUIT



The rectification efficiency factor σ shown in Figure 10 was calculated using the formula:

$$\sigma = \frac{P_{(dc)}}{P_{(rms)}} = \frac{\frac{V^2_{o(dc)}}{R_L}}{\frac{V^2_{o(rms)}}{R_L}} \cdot 100\% = \frac{V^2_{o(dc)}}{V^2_{o(ac)} + V^2_{o(dc)}} \cdot 100\% \quad (1)$$

For a sine wave input $V_m \sin(\omega t)$ to the diode, assumed lossless, the maximum theoretical efficiency factor becomes:

$$\sigma_{(sine)} = \frac{\frac{4V^2_m}{\pi^2 R_L}}{\frac{V^2_m}{2R_L}} \cdot 100\% = \frac{8}{\pi^2} \cdot 100\% = 81.2\% \quad (2)$$

For a square wave input of amplitude V_m, the efficiency factor becomes:

$$\sigma_{(square)} = \frac{\frac{V^2_m}{R_L}}{\frac{V^2_m}{R_L}} \cdot 100\% = 100\% \quad (3)$$

As the frequency of the input signal is increased, the reverse recovery time of the diode (Figure 9) becomes significant, resulting in an increasing ac voltage component across R_L which is opposite in polarity to the forward current, thereby reducing the value of the efficiency factor σ, as shown on Figure 10.

It should be emphasized that Figure 10 shows waveform efficiency only; it does not provide a measure of diode losses. Data was obtained by measuring the ac component of V_o with a true rms ac voltmeter and the dc component with a dc voltmeter. The data was used in Equation 1 to obtain points for Figure 10.

7

MR1-1000
MR1-1200
MR1-1400
MR1-1600

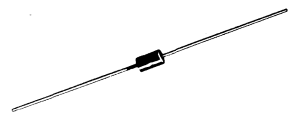
AXIAL LEAD SILICON RECTIFIERS

. . . designed for television "damper" diode service and other high voltage industrial/consumer applications.

- High Current Handling — 1.0 Ampere at 75°C
- Medium Recovery Characteristics
- Low Forward Voltage

HIGH VOLTAGE LEAD MOUNTED SILICON RECTIFIERS

1000, 1200, 1400, 1600 VOLTS
1 AMPERE



MAXIMUM RATINGS

Rating	Symbol	MR1-1000	MR1-1200	MR1-1400	MR1-1600	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	1000	1200	1400	1600	Volts
Average Rectified Forward Current (Single phase, resistive load, $R_{\theta JA}$ = 85°C/W, T_A = 75°C) (1)	I_O	1.0				Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions.)	I_{FSM}	30 (for 1 cycle)				Amp
Operating and Storage Junction Temperature Range (2)	T_J, T_{stg}	-65 to +175				°C

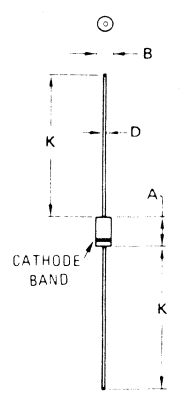
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Typ	Max	Unit
Maximum Instantaneous Forward Voltage (I_F = 1.0 Amp, T_J = 25°C) (I_F = 3.14 Amp, T_J = 25°C)	v_F	 0.95 1.1	 1.1 1.3	Volts
Maximum Reverse Current (rated dc voltage) T_J = 25°C T_J = 100°C	I_R	 0.2 12	 10 100	μA
Capacitance (V_R = 50 volts, f = 1.0 MHz)	C	4.0	7.0	pF
Reverse Recovery Time (I_F = 20 mA, I_R = 2.0 mA)	t_{rr}	17	25	μs
Forward Recovery Time (I_F = 20 mA, V_{fr} = 2.0 V)	t_{fr}	0.7	1.0	μs

(1) Must be derated for reverse power dissipation. See note on Page 3.
(2) Derate as shown in Figure 4.

MECHANICAL CHARACTERISTICS

CASE: Void free, Transfer Molded
MAXIMUM LEAD TEMPERATURE FOR SOLDERING PURPOSES: 350°C, 3/8" case for 10 seconds at 5 lbs. tension
FINISH: All external surfaces are corrosion-resistant, leads are readily solderable
POLARITY: Cathode indicated by color band
WEIGHT: 0.40 Grams (approximately)



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94	-	1.100	-

CASE 59-04

FIGURE 1 – FORWARD POWER DISSIPATION

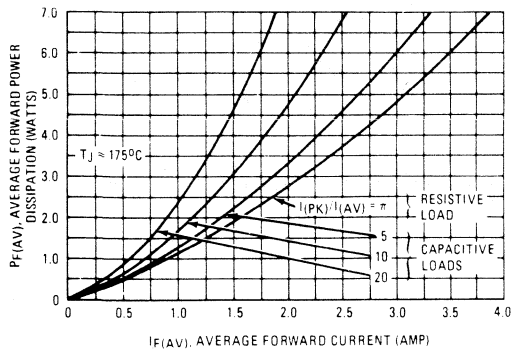


FIGURE 2 – CURRENT DERATING

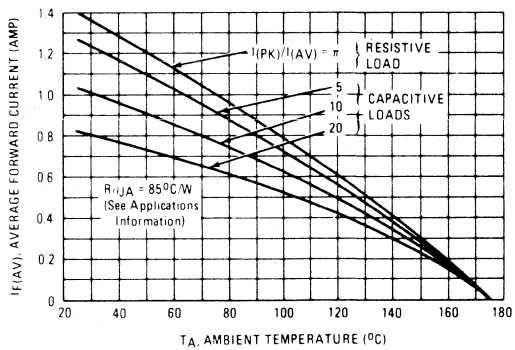


FIGURE 3 – NON-REPETITIVE SURGE CURRENT

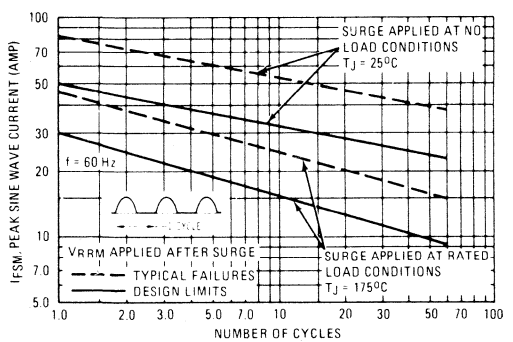
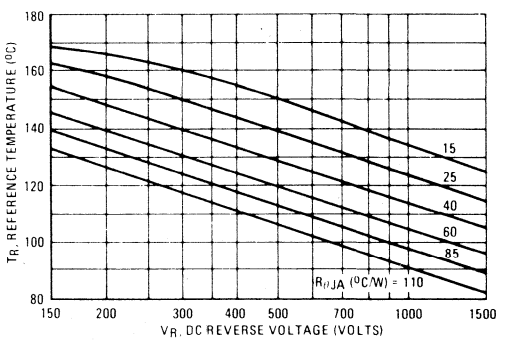


FIGURE 4 – MAXIMUM REFERENCE TEMPERATURE



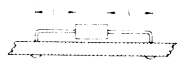
7

APPLICATIONS INFORMATION

TYPICAL VALUES FOR $R_{\theta JA}$ IN STILL AIR

MOUNTING METHOD	LEAD LENGTH, L (IN)			
	1/32	3/8	1	$R_{\theta JA}$
1	–	60	85	°C/W
2	73	85	103	°C/W

MOUNTING METHOD 1
P.C. Board with 1½" x 1½" copper surface



MOUNTING METHOD 2
Vector Push-In Terminals T-28

Reverse power dissipation and the possibility of thermal runaway must be considered when operating this rectifier at reverse voltages above 50 volts. Proper derating may be accomplished by use of equation (1).

$$T_{A(max)} = T_{J(max)} - R_{\theta JA}P_{F(AV)} - R_{\theta JA}P_{R(AV)} \quad (1)$$

where

$T_{A(max)}$ = Maximum allowable ambient temperature

$T_{J(max)}$ = Maximum allowable junction temperature (175°C or the temperature at which thermal runaway occurs, whichever is lowest.)

$P_{F(AV)}$ = Average forward power dissipation

$P_{R(AV)}$ = Average reverse power dissipation

$R_{\theta JA}$ = Junction-to-ambient thermal resistance

Figure 4 permits easier use of equation (1) by taking reverse power dissipation and thermal runaway into consideration. The figure solves for a reference temperature as determined by equation (2).

$$T_R = T_{J(max)} - R_{\theta JA}P_{R(AV)} \quad (2)$$

Substituting equation (2) into equation (1) yields

$$T_{A(max)} = T_R - R_{\theta JA}P_{F(AV)} \quad (3)$$

Inspection of equations (2) and (3) reveals that T_R is the ambient temperature at which thermal runaway occurs or where $T_J = 175°C$ when forward power is zero. The transition from one boundary condition to the other is evident on the curves of Figure 4 as a difference in the rate of change of the slope in the vicinity of 160°C. The data of Figure 4 is based upon dc conditions. For use in common rectifier circuits, Table 1 indicates suggested factors for an equivalent dc voltage to use for conservative design: i.e.:

$$V_{R(equiv)} = V_{in(PK)} \times F \quad (4)$$

The Factor F is derived by considering the properties of the various rectifier circuits and the rectifiers reverse characteristics.

Example: Find $T_{A(max)}$ for MR1-1200 operated in a 500 Volt dc supply using a full wave center-tapped circuit with capacitive filter such that $I_{DC} = 1.0$ A, ($I_{F(AV)} = 0.5$ A), $I_{(PK)}/I_{(AV)} = 10$, Input Voltage = 353 V(rms) (line to center tap), $R_{\theta JA} = 60°C/W$.

Step 1: Find $V_{R(equiv)}$. Read F = 1.11 from Table 1.
$V_{R(equiv)} = 1.41)\ (353)\ (1.11) = 555$ V

Step 2: Find T_R from Figure 4. Read $T_R = 117°C$ @ $V_R = 555$ V @ $R_{\theta JA} = 60°C/W$.

Step 3: Find $P_{F(AV)}$ from Figure 1. Read $P_{F(AV)} = 0.6$ W
@ $\frac{I_{PK}}{I_{AV}} = 10$ & $I_{F(AV)} = 0.5$ A

Step 4: Find $T_{A(max)}$ from equation (3). $T_{A(max)} = 117 - (60)\ (0.6) = 81°C$.

TABLE I – VALUES FOR FACTOR F

Circuit	Half Wave		Full Wave, Bridge		Full Wave Center-Tapped*†	
Load	Resistive	Capacitive*	Resistive	Capacitive	Resistive	Capacitive
Sine Wave	0.45	1.11	0.45	0.55	0.90	1.11
Square Wave	0.61	1.22	0.61	0.61	1.22	1.22

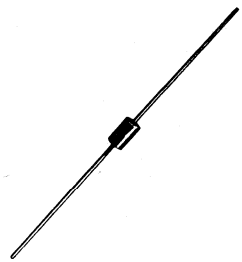
*Note that $V_{R(PK)} \approx 2\ V_{in(PK)}$ †Use line to center tap voltage for V_{in}

MR250-1 thru MR250-5

HIGH VOLTAGE, LOW CURRENT RECTIFIERS

. . . designed for use in applications where small packages are required. These devices feature high surge current capability and low reverse power loss.

HIGH VOLTAGE RECTIFIERS
250 MILLIAMPERES
1000-5000 VOLTS



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	MR250-1	MR250-2	MR250-3	MR250-4	MR250-5	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} $V_{R(RMS)}$	1000	2000	3000	4000	5000	Volts
Average Rectified Forward Current (single phase, resistive load, 60 Hz, T_A = 75°C)	I_O	← 250 →					mA
Peak Repetitive Forward Current T_A = 75°C	I_{FRM}	← 2.0 →					Amp
Non-Repetitive Peak Surge Current (superimposed on rated current at rated voltage, T_A = 75°C)	I_{FSM}	← 20 (for 1/2 cycle) →					Amp
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →					°C

THERMAL CHARACTERISTICS

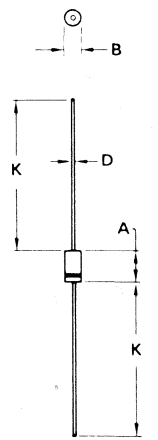
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient (1 inch lead length)	$R_{\theta JA}$	100	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Instantaneous Forward Voltage (i_F = 0.785 Adc, T_A = 25°C)	v_F	3.75	Volts
DC Reverse Current, Rated V_R T_A = 25°C T_A = 100°C	I_R	 10 50	μA

MECHANICAL CHARACTERISTICS

CASE: Void free, transfer molded
FINISH: All external surfaces corrosion-reisitant and leads readily solderable
POLARITY: Indicated by polarity band
MOUNTING POSITIONS: Any
WEIGHT: 0.40 Gram (approx)
MAXIMUM LEAD TEMPERATURE FOR SOLDERING PURPOSES: 350°C, 3/8" from case for 10 seconds



NOTE:
1. POLARITY MARK – CATHODE BAND

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	11.56	11.81	0.455	0.465
B	3.73	3.89	0.147	0.153
D	0.76	0.86	0.030	0.034
K	24.13	29.21	0.950	1.150

CASE 169-02

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FIGURE 1 – MAXIMUM FORWARD VOLTAGE

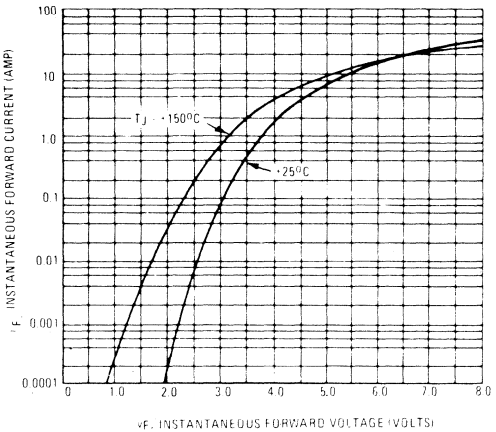


FIGURE 2 – TYPICAL REVERSE CURRENT

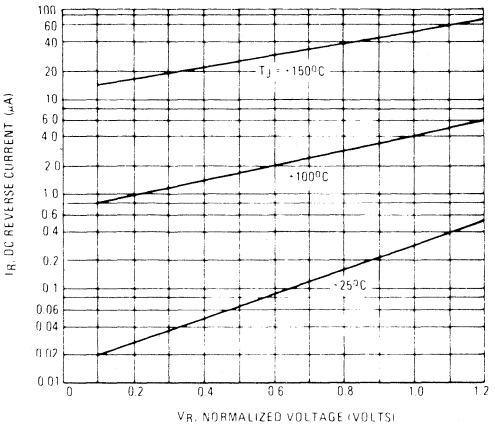
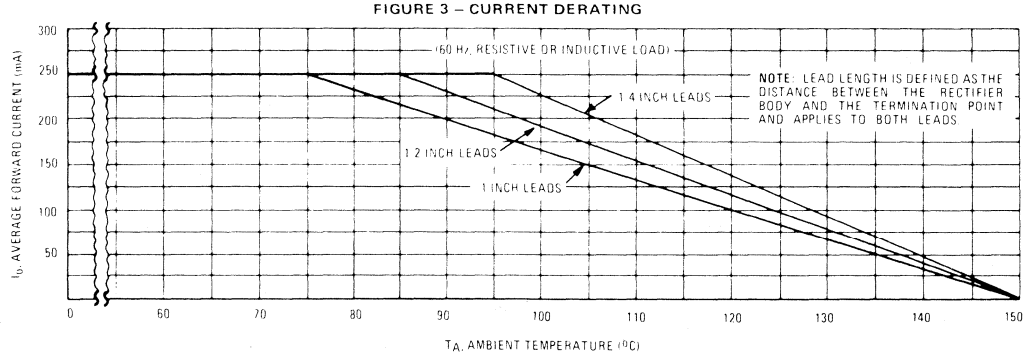
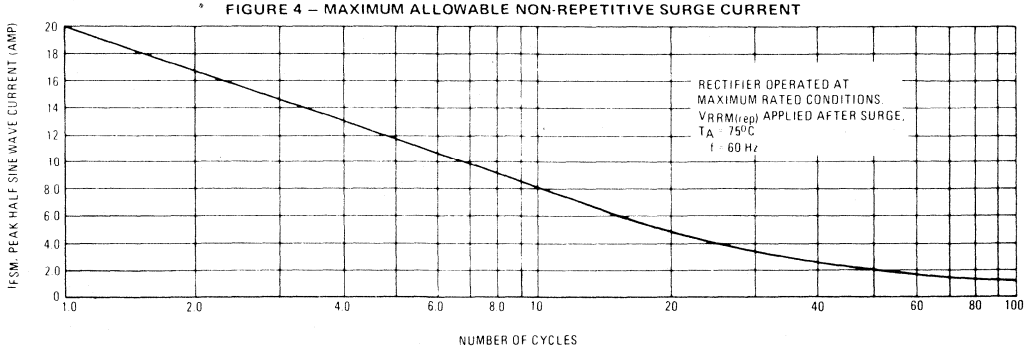


FIGURE 3 – CURRENT DERATING



* FIGURE 4 – MAXIMUM ALLOWABLE NON-REPETITIVE SURGE CURRENT



MR500 MR501 MR502 MR504 MR506 MR508 MR510

Designers Data Sheet

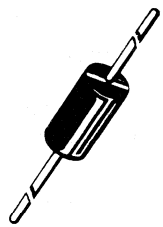
STANDARD RECOVERY POWER RECTIFIERS

50-1000 VOLTS
3 AMPERE

MINIATURE SIZE, AXIAL LEAD MOUNTED STANDARD RECOVERY POWER RECTIFIERS

. . . designed for use in power supplies and other applications having need of a device with the following features:

- High Current to Small Size
- High Surge Current Capability
- Low Forward Voltage Drop
- Void-Free Economical Plastic Package
- Available in Volume Quantities



Designer's Data for "Worst Case" Conditions

The Designers Data sheets permit the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MAXIMUM RATINGS

Rating	Symbol	MR500	MR501	MR502	MR504	MR506	MR508	MR510	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	400	600	800	1000	Volts
Non-Repetitive Peak Reverse Voltage	V_{RSM}	75	150	250	450	650	850	1050	Volts
Average Rectified Forward Current (Single phase resistive load, T_Z = 95°C, PC Board Mounting) (1)	I_O	3.0							Amp
(EIA Standard Conditions L = 1/32", T_L = 85°C)		8.0							
Non-Repetitive Peak Surge Current (surge applied at rated load conditions)	I_{FSM}	100 (one cycle)							Amp
Operating and Storage Junction Temperature Range (2)	T_J, T_{stg}	-65 to +175							°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient (Recommended Printed Circuit Board Mounting, See Note 2 on Page 4).	$R_{\theta JA}$	28	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Instantaneous Forward Voltage (3)	v_F				Volts
(i_F = 9.4 Amp, T_J = 175°C)		–	0.9	1.0	
(i_F = 9.4 Amp, T_J = 25°C)		–	1.04	1.1	
Reverse Current (rated dc voltage) (3)	I_R				μA
T_J = 25°C		–	0.1	5.0	
T_J = 100°C		–	2.8	25	

(1) Derate for reverse power dissipation. See Note on Page 2.
(2) Derate as shown in Figure 1.
(3) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

MECHANICAL CHARACTERISTICS

Case: Void Free, Transfer Molded
Finish: External Leads are Plated, Leads are readily Solderable
Polarity: Indicated by Cathode Band
Weight: 1.1 Grams (Approximately)
Maximum Lead Temperature for Soldering Purposes:
300°C, 1/8" from case for 10 s at 5.0 lb. tension

7

NOTE 1: DETERMINING MAXIMUM RATINGS

Reverse power dissipation and the possibility of thermal runaway must be considered when operating this rectifier at reverse voltages above 200 volts. Proper derating may be accomplished by use of equation (1):

$$T_{A(max)} = T_{J(max)} - R_{\theta JA}P_{F(AV)} - R_{\theta JA}P_{R(AV)} \quad (1)$$

where

$T_{A(max)}$ = Maximum allowable ambient temperature

$T_{J(max)}$ = Maximum allowable junction temperature (175°C or the temperature at which thermal runaway occurs, whichever is lowest.)

$P_{F(AV)}$ = Average forward power dissipation

$P_{R(AV)}$ = Average reverse power dissipation

$R_{\theta JA}$ = Junction-to-ambient thermal resistance

Figure 1 permits easier use of equation (1) by taking reverse power dissipation and thermal runaway into consideration. The figure solves for a reference temperature as determined by equation (2):

$$T_R = T_{J(max)} - R_{\theta JA}P_{R(AV)} \quad (2)$$

Substituting equation (2) into equation (1) yields:

$$T_{A(max)} = T_R - R_{\theta JA}P_{F(AV)} \quad (3)$$

Inspection of equations (2) and (3) reveals that T_R is the ambient temperature at which thermal runaway occurs or where T_J = 175°C, when forward power is zero. The transition from one boundary condition to the other is evident on the curves of Figure 1 as a difference in the rate of change of the slope in the vicinity of 165°C. The data of Figure 1 is based upon dc conditions. For use in common rectifier circuits, Table 1 indicates suggested factors for an equivalent dc voltage to use for conservative design; i.e.:

$$V_{R(equiv)} = V_{in(PK)} \times F \quad (4)$$

The Factor F is derived by considering the properties of the various rectifier circuits and the rectifiers reverse characteristics.

Example: Find $T_{A(max)}$ for MR510 operated in a 400 Volt dc supply using a full wave center-tapped circuit with capacitive filter such that I_{DC} = 6.0 A, ($I_{F(AV)}$ = 3.0 A), $I_{(PK)}/I_{(AV)}$ = 10, Input Voltage = 283 V(rms) (line to center tap), $R_{\theta JA}$ = 28°C/W.

Step 1: Find $V_{R(equiv)}$. Read F = 1.11 from Table 1 ∴
$V_{R(equiv)} = 1.41)(283)(1.11) = 444$ V

Step 2: Find T_R from Figure 1. Read T_R = 167°C @ V_R = 444 V & $R_{\theta JA}$ = 28°C/W.

Step 3: Find $P_{F(AV)}$ from Figure 8. Read $P_{F(AV)}$ = 4 W @ $\frac{I_{PK}}{I_{AV}}$ = 10 & $I_{F(AV)}$ = 3.0 A

Step 4: Find $T_{A(max)}$ from equation (3). $T_{A(max)}$ = 167-(28)(4) = 55°C.

TABLE I – VALUES FOR FACTOR F

Circuit	Half Wave		Full Wave, Bridge		Full Wave Center-Tapped*†	
Load	Resistive	Capacitive*	Resistive	Capacitive	Resistive	Capacitive
Sine Wave	0.45	1.11	0.45	0.55	0.90	1.11
Square Wave	0.61	1.22	0.61	0.61	1.22	1.22

*Note that $V_{R(PK)} \approx 2\ V_{in(PK)}$ †Use line to center tap voltage for V_{in}.

FIGURE 1 – MAXIMUM REFERENCE TEMPERATURE

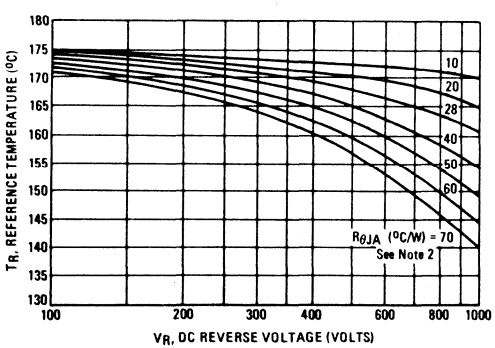
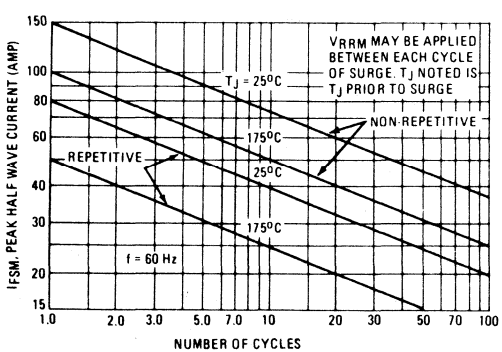


FIGURE 2 – MAXIMUM SURGE CAPABILITY



CURRENT DERATING

(Reverse Power Loss Neglected)

FIGURE 3 – PC BOARD MOUNTING

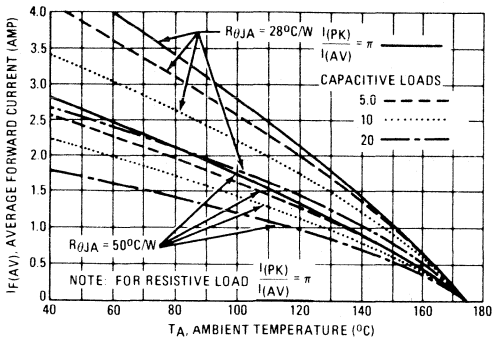


FIGURE 4 – SEVERAL LEAD LENGTHS

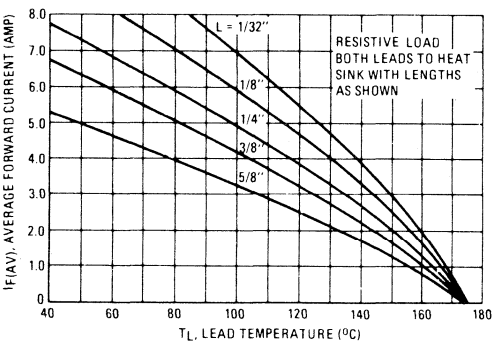


FIGURE 5 – 1/8" LEAD LENGTH

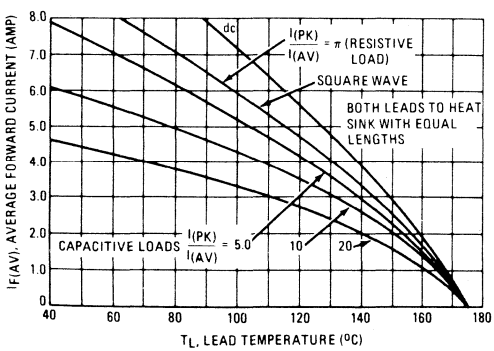


FIGURE 6 – MAXIMUM FORWARD VOLTAGE

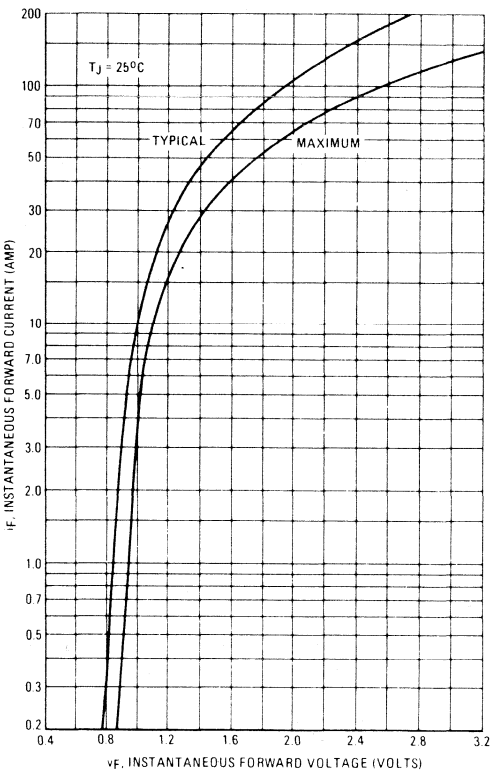


FIGURE 7 – FORWARD VOLTAGE TEMPERATURE COEFFICIENT

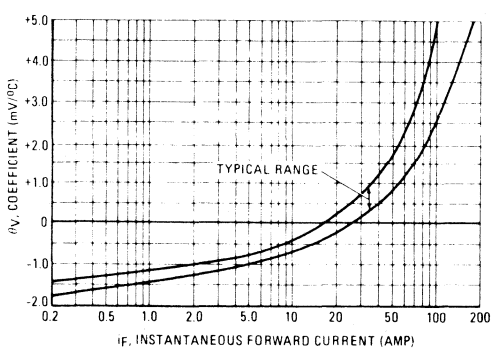


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FIGURE 8 – FORWARD POWER DISSIPATION

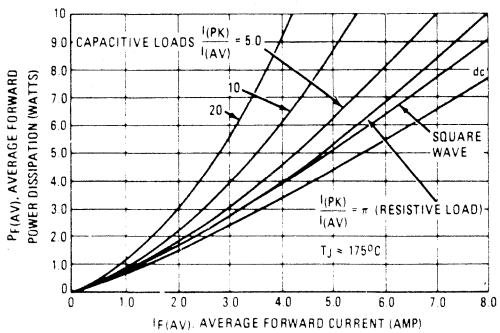
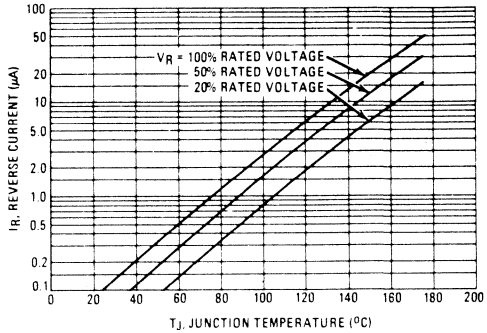


FIGURE 9 – TYPICAL REVERSE CURRENT



THERMAL CHARACTERISTICS

FIGURE 10 – THERMAL RESPONSE

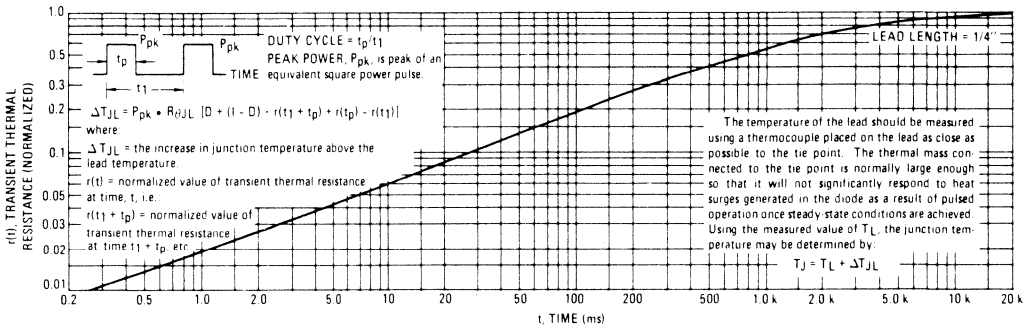
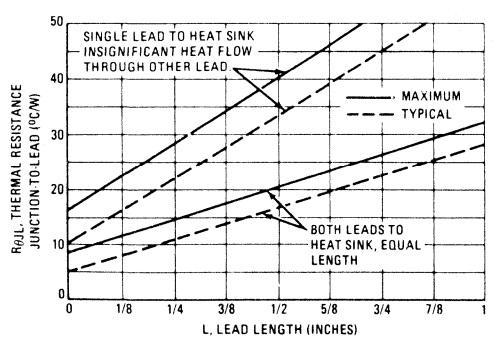


FIGURE 11 – STEADY-STATE THERMAL RESISTANCE



NOTE 2 – AMBIENT MOUNTING DATA

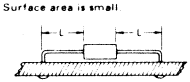
Data shown for thermal resistance junction-to-ambient ($R_{\theta JA}$) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

TYPICAL VALUES FOR $R_{\theta JA}$ IN STILL AIR

MOUNTING METHOD	LEAD LENGTH, L (IN) 1/8	1/4	1/2	3/4	$R_{\theta JA}$
1	50	51	53	55	°C/W
2	58	59	61	63	°C/W
3	28				°C/W

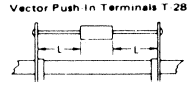
MOUNTING METHOD 1

P.C. Board Where Available Copper Surface area is small.



MOUNTING METHOD 2

Vector Push-In Terminals T-28



MOUNTING METHOD 3

P.C. Board with 1-1/2" x 1-1/2" Copper Surface

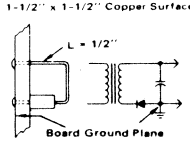
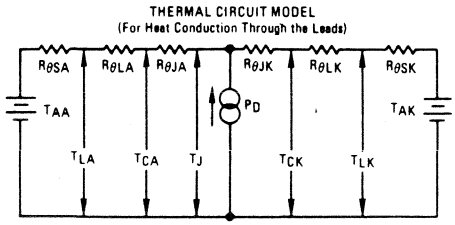


FIGURE 12 – APPROXIMATE THERMAL CIRCUIT MODEL



Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heat sink. Terms in the model signify.

T_A = Ambient Temperature
T_L = Lead Temperature
T_C = Case Temperature
T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_D = Total Power Dissipation = $P_F + P_R$
P_F = Forward Power Dissipation
P_R = Reverse Power Dissipation

(Subscripts A and K refer to anode and cathode sides respectively.)
Values for thermal resistance components are:

$R_{\theta L}$ = 46°C/W/IN. Typically and 48°C/W/IN Maximum
$R_{\theta J}$ = 10°C/W Typically and 16°C/W Maximum

The maximum lead temperature may be found as follows:

$$T_L = T_{J(max)} - \Delta T_{JL}$$

where $\Delta T_{JL} \approx R_{\theta JL}$

TYPICAL DYNAMIC CHARACTERISTICS

(T_J = 25°C)

FIGURE 13 – FORWARD RECOVERY TIME

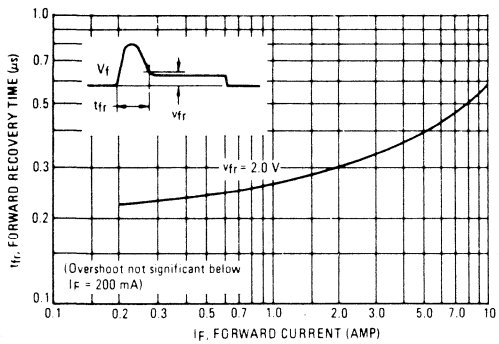


FIGURE 14 – REVERSE RECOVERY TIME

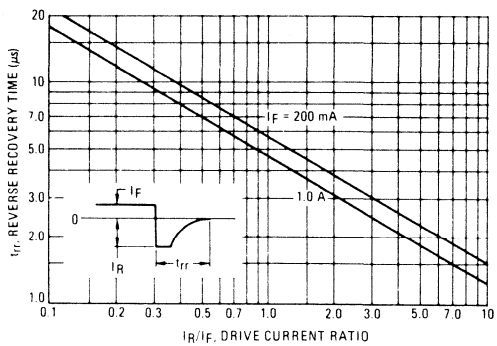


FIGURE 15 – RECTIFICATION WAVEFORM EFFICIENCY

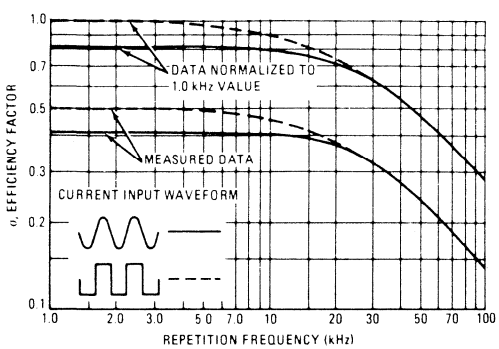
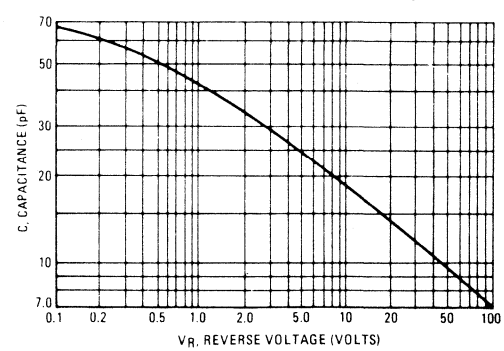


FIGURE 16 – JUNCTION CAPACITANCE



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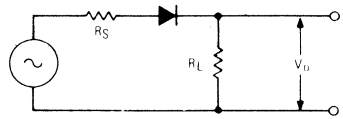
RECTIFIER EFFICIENCY NOTE

FIGURE 17 – SINGLE-PHASE HALF-WAVE RECTIFIER CIRCUIT



The rectification efficiency factor σ shown in Figure 15 was calculated using the formula:

$$\sigma = \frac{P_{(dc)}}{P_{(rms)}} = \frac{\frac{V^2_o(dc)}{R_L}}{\frac{V^2_o(rms)}{R_L}} \cdot 100\% = \frac{V^2_o(dc)}{V^2_o(ac) + V^2_o(dc)} \cdot 100\% \quad (1)$$

For a sine wave input $V_m \sin(\omega t)$ to the diode, assumed lossless, the maximum theoretical efficiency factor becomes:

$$\sigma_{(sine)} = \frac{\frac{V^2_m}{\pi^2 R_L}}{\frac{V^2_m}{4R_L}} \cdot 100\% = \frac{4}{\pi^2} \cdot 100\% = 40.6\% \quad (2)$$

For a square wave input of amplitude V_m, the efficiency factor becomes:

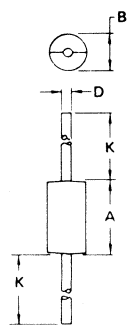
$$\sigma_{(square)} = \frac{\frac{V^2_m}{2R_L}}{\frac{V^2_m}{R_L}} \cdot 100\% = 50\% \quad (3)$$

(A full wave circuit has twice these efficiencies)

As the frequency of the input signal is increased, the reverse recovery time of the diode (Figure 14) becomes significant, resulting in an increasing ac voltage component across R_L which is opposite in polarity to the forward current, thereby reducing the value of the efficiency factor σ, as shown on Figure 15.

It should be emphasized that Figure 15 shows waveform efficiency only; it does not provide a measure of diode losses. Data was obtained by measuring the ac component of V_o with a true rms ac voltmeter and the dc component with a dc voltmeter. The data was used in Equation 1 to obtain points for the figure.

OUTLINE DIMENSIONS



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	9.65	0.370	0.380
B	4.83	5.33	0.190	0.210
D	1.22	1.32	0.048	0.052
K	26.97	27.23	1.062	1.072

CASE 267-01

MR 750 SERIES

Designers Data Sheet

HIGH CURRENT LEAD MOUNTED RECTIFIERS

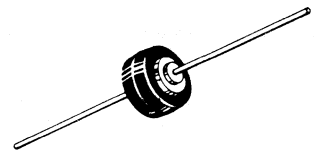
- Current Capacity Comparable To Chassis Mounted Rectifiers
- Very High Surge Capacity
- Insulated Case

Designer's Data for "Worst Case" Conditions

The Designers Data sheets permit the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

HIGH CURRENT LEAD MOUNTED SILICON RECTIFIERS

50–1000 VOLTS
DIFFUSED JUNCTION



MAXIMUM RATINGS

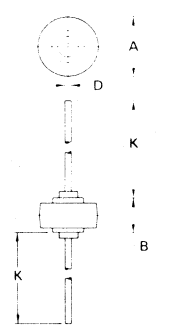
Characteristic	Symbol	MR750	MR751	MR752	MR754	MR756	MR758	MR760	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	400	600	800	1000	Volts
Non-Repetitive Peak Reverse Voltage (halfwave, single phase, 60 Hz peak)	V_{RSM}	60	120	240	480	720	960	1200	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	35	70	140	280	420	560	700	Volts
Average Rectified Forward Current (single phase, resistive load, 60 Hz.) See Figures 5 and 6	I_O	22 (T_L = 60°C, 1/8" Lead Lengths) 6.0 (T_A = 60°C, P.C. Board mounting)							Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions)	I_{FSM}	400 (for 1 cycle)							Amp
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +175							°C

ELECTRICAL CHARACTERISTICS

Characteristic and Conditions	Symbol	Max	Unit
Maximum Instantaneous Forward Voltage Drop (i_F = 100 Amp, T_J = 25°C)	v_F	1.25	Volts
Maximum Forward Voltage Drop (I_F = 6.0 Amp, T_A = 25°C, 3/8" leads)	V_F	0.90	Volts
Maximum Reverse Current (rated dc voltage) T_J = 25°C T_J = 100°C	I_R	0.25 1.0	mA

MECHANICAL CHARACTERISTICS

CASE: Void free, Transfer Molded
MAXIMUM LEAD TEMPERATURE FOR SOLDERING PURPOSES: 350°C 3/8" from case for 10 seconds at 5.0 lbs. tension
FINISH: All external surfaces are corrosion-resistant, leads are readily solderable
POLARITY: Indicated by diode symbol
WEIGHT: 2.5 Grams (approx.)



NOTE:
1. CATHODE SYMBOL ON PKG.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.03	10.29	0.395	0.405
B	5.94	6.25	0.234	0.246
D	1.27	1.35	0.050	0.053
K	25.15	25.65	0.990	1.010

CASE 194-01

7

FIGURE 1 – FORWARD VOLTAGE

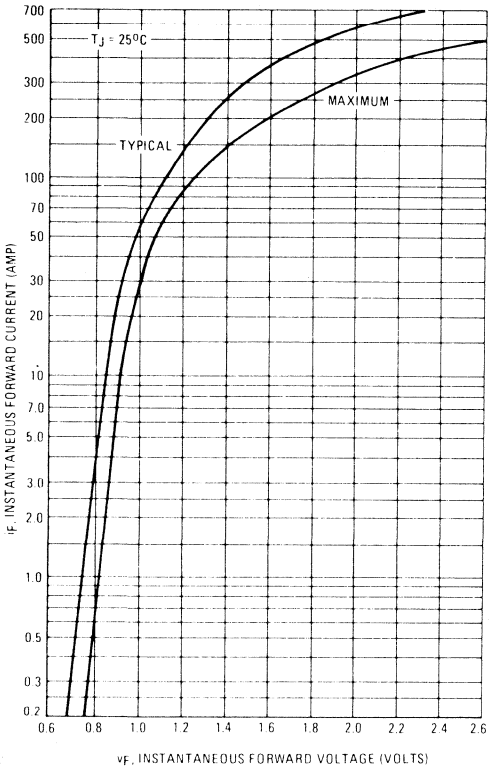


FIGURE 2 – MAXIMUM SURGE CAPABILITY

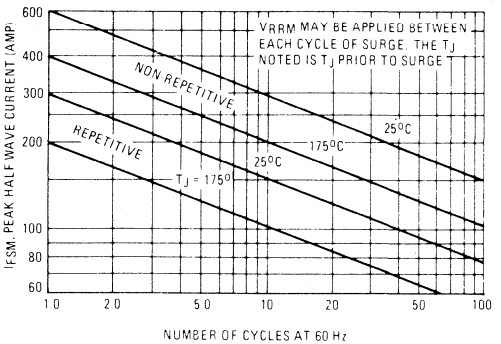


FIGURE 3 – FORWARD VOLTAGE TEMPERATURE COEFFICIENT

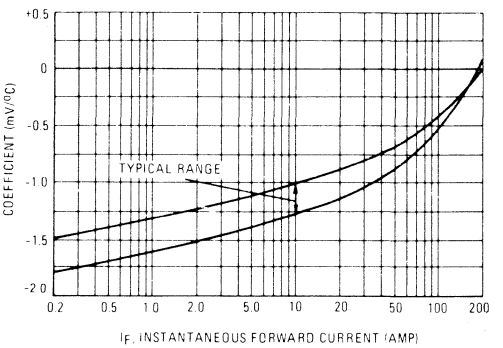


FIGURE 4 – TYPICAL TRANSIENT THERMAL RESISTANCE

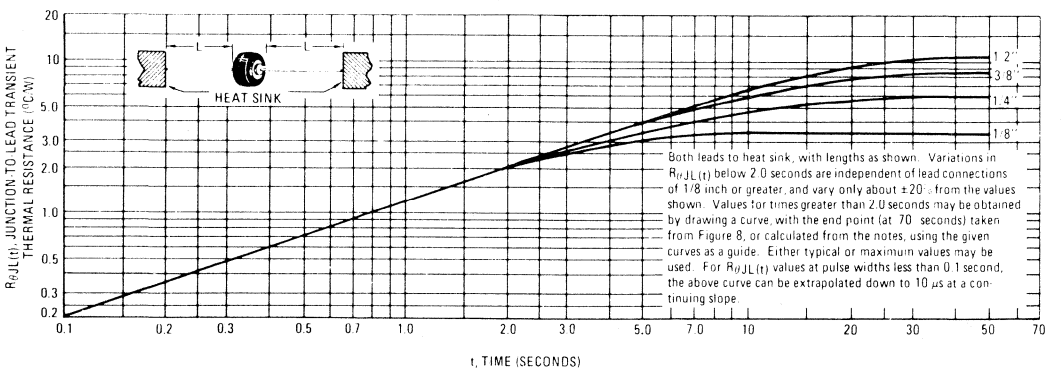


FIGURE 5 – MAXIMUM CURRENT RATINGS

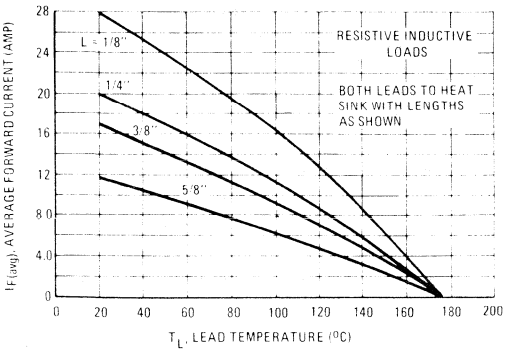


FIGURE 6 – MAXIMUM CURRENT RATINGS

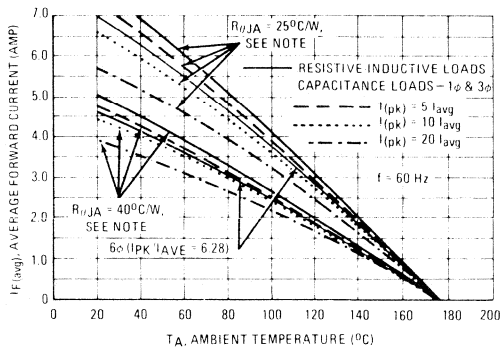


FIGURE 7 – POWER DISSIPATION

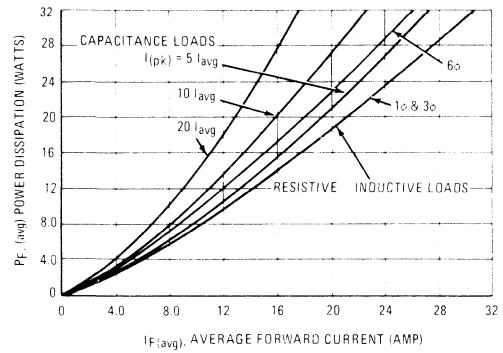
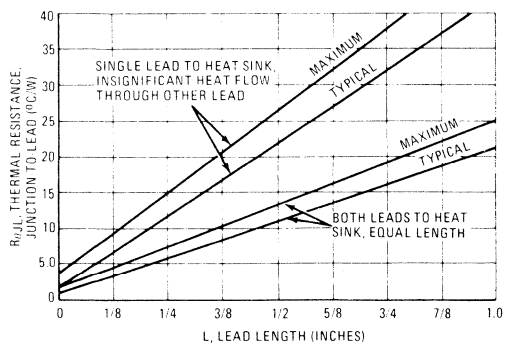


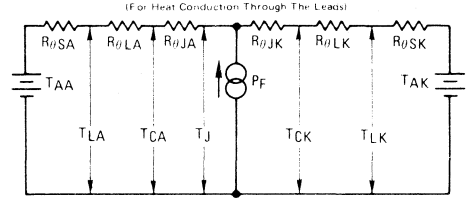
FIGURE 8 – STEADY STATE THERMAL RESISTANCE



NOTES

THERMAL CIRCUIT MODEL

(For Heat Conduction Through The Leads)



Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. Lowest values occur when one side of the rectifier is brought as close as possible to the heat sink as shown below. Terms in the model signify:

T_A = Ambient Temperature
T_L = Lead Temperature
T_C = Case Temperature
T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_F = Power Dissipation

(Subscripts A and K refer to anode and cathode sides respectively.)

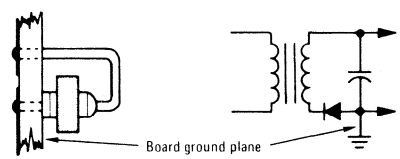
Values for thermal resistance components are:

$R_{\theta L}$ = 40°C/W/IN Typically and 44°C/W/IN Maximum

$R_{\theta J}$ = 2°C/W Typically and 4°C/W Maximum

Since $R_{\theta J}$ is so low, measurements of the case temperature, T_C, will be approximately equal to junction temperature in practical lead mounted applications. When used as a 60 Hz rectifier, the slow thermal response holds $T_{J(PK)}$ close to $T_{J(AVG)}$. Therefore maximum lead temperature may be found from: $T_L = 175° - R_{\theta JL} P_F$. P_F may be found from Figure 7.

The recommended method of mounting to a P.C. board is shown on the sketch, where $R_{\theta JA}$ is approximately 25°C/W for a 1 1/2" x 1-1/2" copper surface area. Values of 40°C/W are typical for mounting to terminal strips or P.C. boards where available surface area is small.



Recommended mounting for half wave circuit

7

TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 9 – RECTIFICATION EFFICIENCY

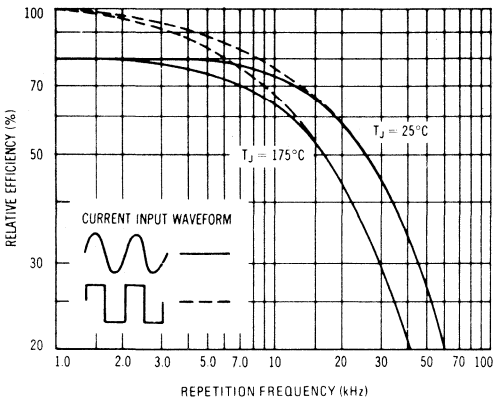


FIGURE 10 – REVERSE RECOVERY TIME

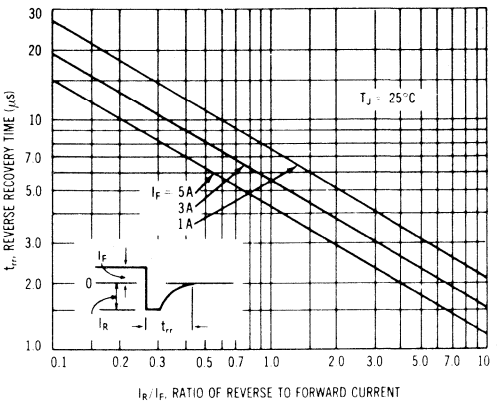


FIGURE 11 – JUNCTION CAPACITANCE

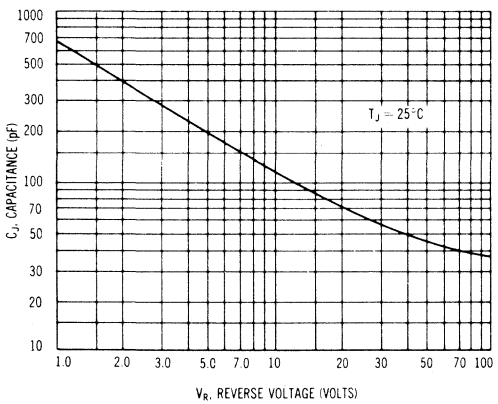


FIGURE 12 – FORWARD RECOVERY TIME

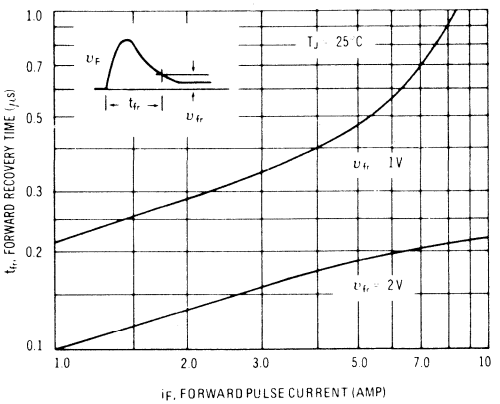
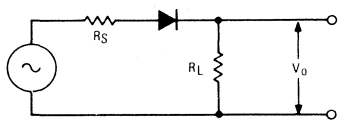


FIGURE 13 – SINGLE-PHASE HALF-WAVE RECTIFIER CIRCUIT



The rectification efficiency factor σ shown in Figure 9 was calculated using the formula:

$$\sigma = \frac{P_{(dc)}}{P_{(rms)}} = \frac{\frac{V^2_{o(dc)}}{R_L}}{\frac{V^2_{o(rms)}}{R_L}} \cdot 100\% = \frac{V^2_{o(dc)}}{V^2_{o(ac)} + V^2_{o(dc)}} \cdot 100\% \quad (1)$$

For a sine wave input $V_m \sin(\omega t)$ to the diode, assumed lossless, the maximum theoretical efficiency factor becomes:

$$\sigma_{(sine)} = \frac{\frac{V^2_m}{\pi^2 R_L}}{\frac{V^2_m}{4R_L}} \cdot 100\% = \frac{4}{\pi^2} \cdot 100\% = 40.6\% \quad (2)$$

For a square wave input of amplitude V_m, the efficiency factor becomes:

$$\sigma_{(square)} = \frac{\frac{V^2_m}{2R_L}}{\frac{V^2_m}{R_L}} \cdot 100\% = 50\% \quad (3)$$

(A full wave circuit has twice these efficiencies)

As the frequency of the input signal is increased, the reverse recovery time of the diode (Figure 10) becomes significant, resulting in an increasing ac voltage component across R_L which is opposite in polarity to the forward current, thereby reducing the value of the efficiency factor σ, as shown on Figure 9.

It should be emphasized that Figure 9 shows waveform efficiency only; it does not provide a measure of diode losses. Data was obtained by measuring the ac component of V_o with a true rms ac voltmeter and the dc component with a dc voltmeter. The data was used in Equation 1 to obtain points for Figure 9.

MR810 thru MR814
MR816 thru MR818

Designers Data Sheet

SUBMINIATURE SIZE, AXIAL LEAD MOUNTED FAST RECOVERY POWER RECTIFIERS

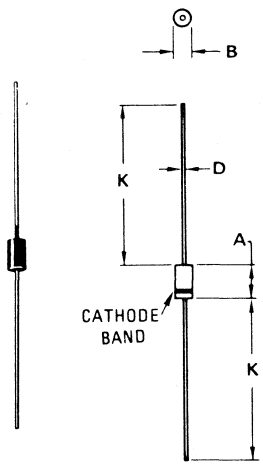
. . . designed for special applications such as dc power supplies, inverters, converters, ultrasonic systems, choppers, low RF interference and free-wheeling diodes. A complete line of fast recovery rectifiers having typical recovery time of 350 nanoseconds providing high efficiency at frequencies to 100 kHz.

DESIGNER'S DATA FOR "WORST CASE" CONDITIONS

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit curves – representing device characteristic boundaries – are given to facilitate "worst case" design.

FAST RECOVERY POWER RECTIFIERS

50-1000 VOLTS
1 AMPERE



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94	–	1.100	–

CASE 59-04

MAXIMUM RATINGS

Rating	Symbol	MR810	MR811	MR812	MR813	MR814	MR816	MR817	MR818	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	300	400	500	800	1000	Volts
Non-Repetitive Peak Reverse Voltage	V_{RSM}	100	200	300	400	500	800	1000	1200	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	35	70	140	210	280	420	560	700	Volts
Average Rectified Forward Current (Single phase, resistive load, T_A = 75°C)	I_O	1.0								Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions) (T_A = 75°C)	I_{FSM}	30								Amps
Operating Junction Temperature Range	T_J	-65 to +150								°C
Storage Temperature Range	T_{stg}	-65 to +175								°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient (Typical Printed Circuit Board Mounting)	$R_{\theta JA}$	65	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Instantaneous Forward Voltage (i_F = 3.14 Amp, T_J = 150°C)	v_F	–	1.1	1.2	Volts
Forward Voltage (I_F = 1.0 Amp, T_A = 25°C)	V_F	–	1.0	1.2	Volts
Reverse Current (rated dc voltage) T_A = 25°C T_A = 100°C	I_R	– –	1.0 50	10 100	μA

REVERSE RECOVERY CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Recovery Time (I_F = 1.0 Amp to V_R = 30 Vdc) (Figure 21) (I_F = 20 mA, I_R = 2.0 mA, Tektronix S-Plug-In) (Figure 22)	t_{rr}	– –	350 1.5	750 3.0	ns μs
Reverse Recovery Current (I_F = 1.0 Amp to V_R = 30 Vdc) (Figure 21)	$I_{RM(REC)}$	–	–	3.0	Amp

MECHANICAL CHARACTERISTICS

CASE: Void Free, Transfer Molded

FINISH: External leads are plated and are readily solderable

POLARITY: Cathode indicated by Polarity band

WEIGHT: 0.4 Grams (Approximately)

7

FIGURE 1 – FORWARD VOLTAGE

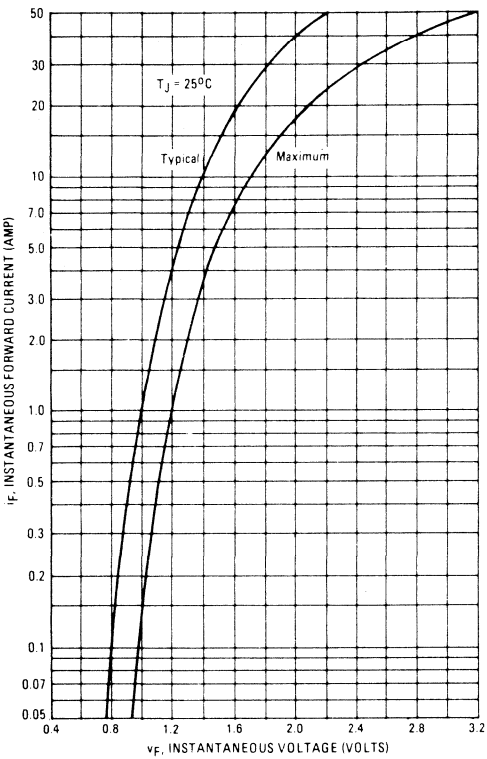


FIGURE 2 – MAXIMUM SURGE CAPABILITY

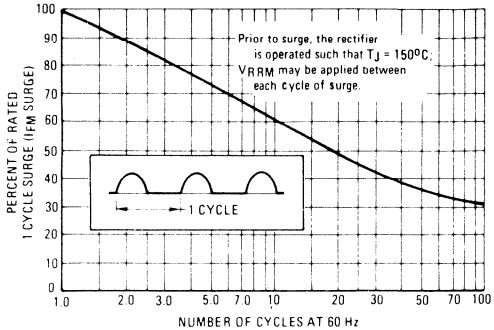


FIGURE 3 – TEMPERATURE COEFFICIENT

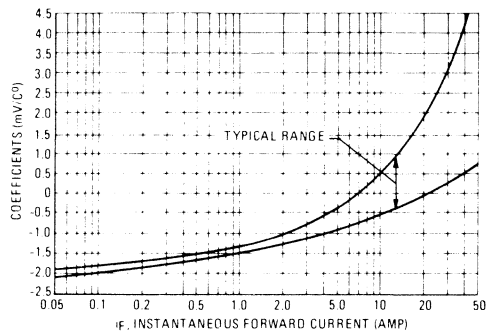


FIGURE 4 – FORWARD POWER DISSIPATION

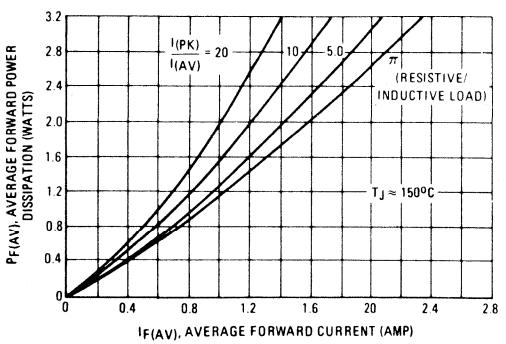
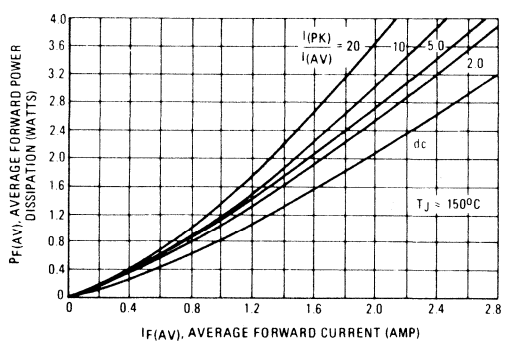


FIGURE 5 – FORWARD POWER DISSIPATION



MAXIMUM CURRENT RATINGS
(SEE NOTES 1 and 2)

SINE WAVE INPUT

FIGURE 6 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

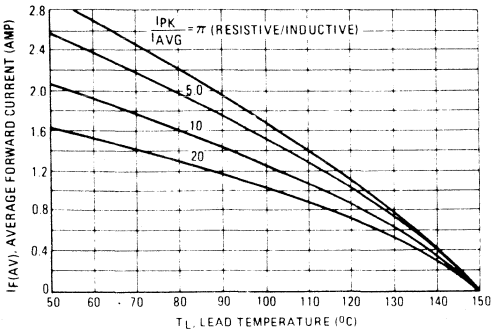


FIGURE 8 – 1/8" LEAD LENGTH, VARIOUS LOADS

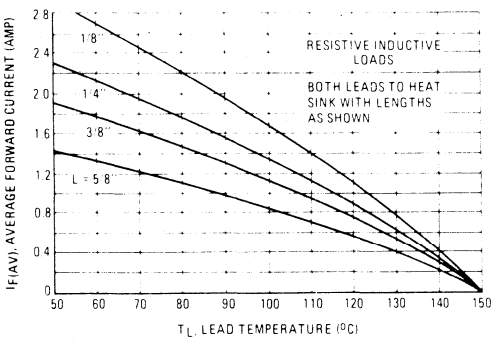
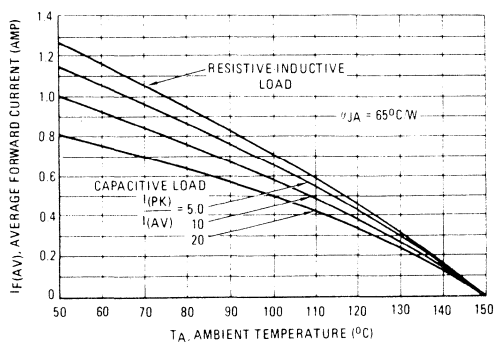


FIGURE 10 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS



SQUARE WAVE INPUT

FIGURE 7 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

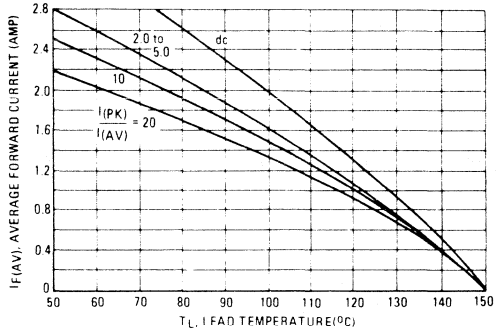


FIGURE 9 – 1/8" LEAD LENGTH, VARIOUS LOADS

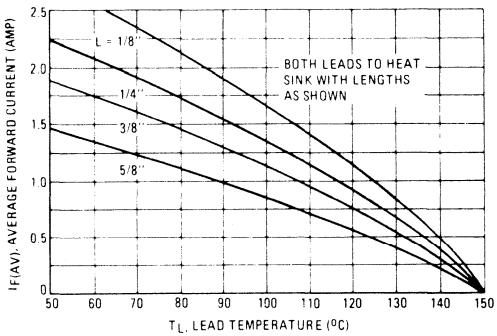


FIGURE 11 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS

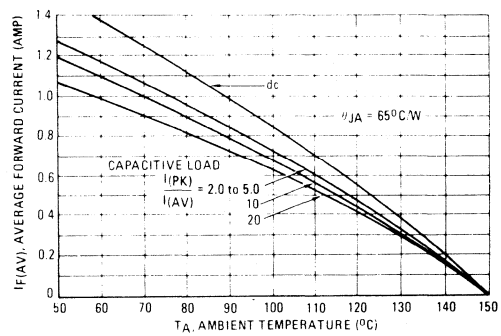


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FIGURE 12 – THERMAL RESPONSE

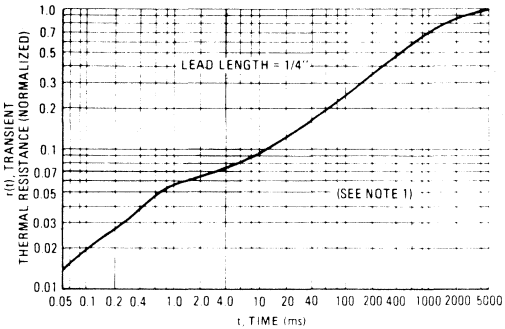
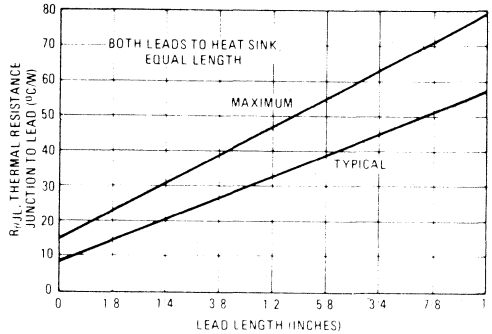
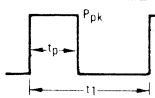


FIGURE 13 – THERMAL RESISTANCE



NOTE 1



DUTY CYCLE, D = t_p / t_1

PEAK POWER, P_{pk}, is peak of an equivalent square power pulse.

To determine maximum junction temperature of the diode in a given situation, the following procedure is recommended:

The temperature of the case should be measured using a thermocouple placed on the case as close as possible to the tie point. The thermal mass connected to the tie point is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady-**state conditions are achieved. Using the measured value of T_C,** the junction temperature may be determined by:

$$T_J = T_C + T_{JC}$$

where T_{JC} is the increase in junction temperature above the case temperature. It may be determined by:

$$\therefore T_{JC} = P_{pk} \cdot R_{\theta JC} \left[D + (1 - D) \cdot r(t_1 + t_p) + r(t_p) - r(t_1) \right]$$

where:

r(t) = normalized value of transient thermal resistance at time, t, from Figure 12, i.e.:

$r(t_1 + t_p)$ = normalized value of transient thermal resistance at time $t_1 + t_p$.

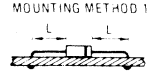
NOTE 2

Data shown for thermal resistance junction to ambient ($R_{\theta JA}$) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

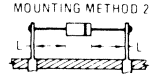
TYPICAL VALUES FOR $R_{\theta JA}$ IN STILL AIR

MOUNTING METHOD	LEAD LENGTH, L (IN.) 1/8	1/4	1/2	3/4	$R_{\theta JA}$
1					
2					
3					

MOUNTING METHOD 1



MOUNTING METHOD 2

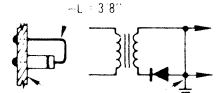


Vector pin mounting

MOUNTING METHOD 3

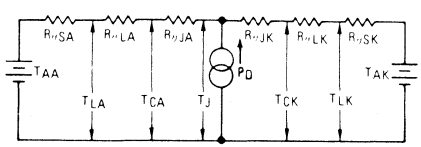
P.C. Board with 1 1/2" x 1 1/2" copper surface

L = 3/8"



Board Ground Plane

FIGURE 14 – THERMAL CIRCUIT MODEL



Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heat sink. Terms in the model signify:

T_A = Ambient Temperature
T_L = Lead Temperature
T_C = Case Temperature
T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_D = Power Dissipation

(Subscripts A and K refer to anode and cathode sides respectively.) Values for thermal resistance components are:

$R_{\theta L}$ = 112°C/W/IN. Typically and 128°C/W/IN Maximum.

$R_{\theta J}$ = 18°C/W Typically and 30°C/W Maximum.

The maximum lead temperature may be calculated as follows:

$$T_L = 150^\circ - T_{JL}$$

T_{JL} can be calculated as shown in NOTE 1 or it may be approximated as follows:

$$T_{JL} \approx R_{\theta JL} \bullet P_F$$

P_F may be formulated for sine-wave operation from Figure 3 or from Figure 4 for square wave operation.

TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 15 – FORWARD RECOVERY TIME

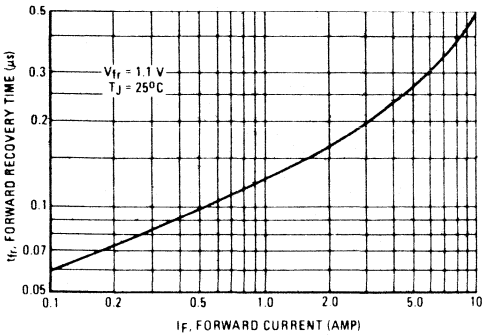
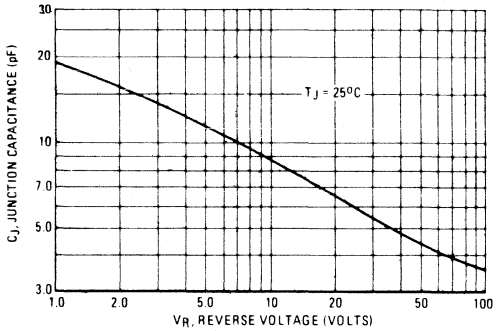


FIGURE 16 – JUNCTION CAPACITANCE



TYPICAL RECOVERED STORED CHARGE DATA
(SEE NOTE 3)

FIGURE 17 – T_J = 25°C

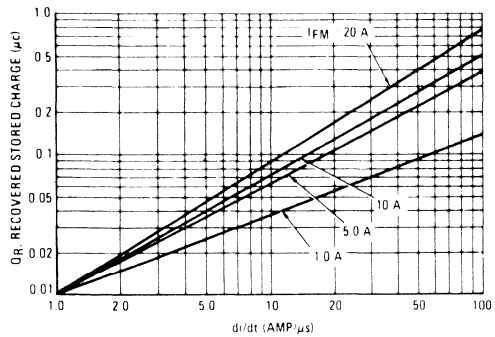


FIGURE 18 – T_J = 75°C

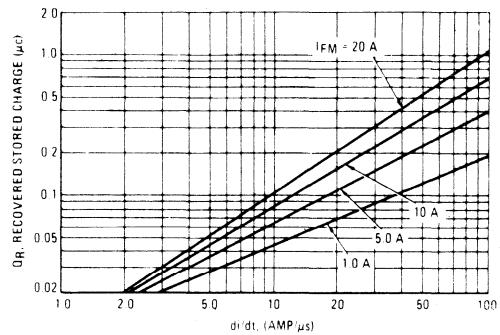


FIGURE 19 – T_J = 100°C

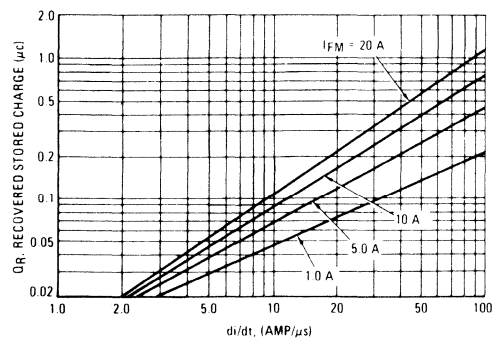


FIGURE 20 – T_J = 150°C

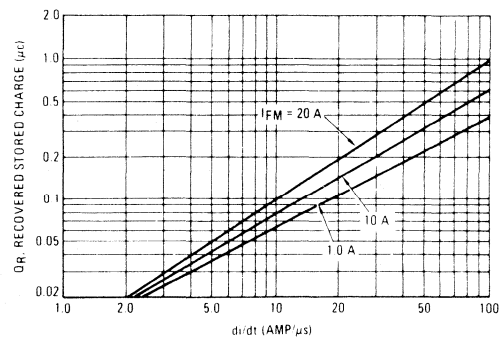


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FIGURE 21 – REVERSE RECOVERY CIRCUIT

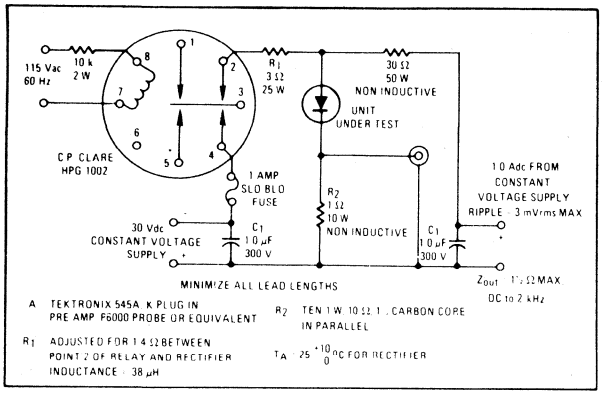
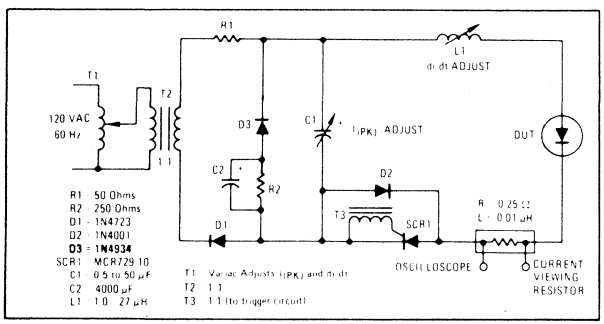


FIGURE 22 – JEDEC REVERSE RECOVERY CIRCUIT



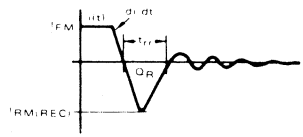
NOTE 3

Reverse recovery time is the period which elapses from the time that the current, thru a previously forward biased rectifier diode, passes thru zero going negatively until the reverse current recovers to a point which is less than 10% peak reverse current.

Reverse recovery time is a direct function of the forward current prior to the application of reverse voltage.

For any given rectifier, recovery time is very circuit dependent. Typical and maximum recovery time of all Motorola fast recovery power rectifiers are rated under a fixed set of conditions using I_F = 1.0 A, V_R = 30 V. In order to cover all circuit conditions, curves are given for typical recovered stored charge versus commutation di/dt for various levels of forward current and for junction temperatures of 25°C, 75°C, 100°C, and 150°C.

To use these curves, it is necessary to know the forward current level just before commutation, the circuit commutation di/dt, and the operating junction temperature. The reverse recovery test current waveform for all Motorola fast recovery rectifiers is shown.



From stored charge curves versus di/dt, recovery time (t_{rr}) and peak reverse recovery current ($I_{RM(REC)}$) can be closely approximated using the following formulas:

$$t_{rr} = 1.41 \times \left[\frac{Q_R}{di/dt}\right]^{1.2}$$

$$I_{RM(REC)} = 1.41 \times \left[Q_R \times di/dt\right]^{1.2}$$

FIGURE 23 – TYPICAL REVERSE LEAKAGE

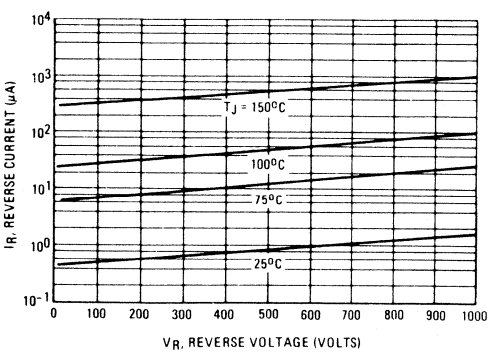
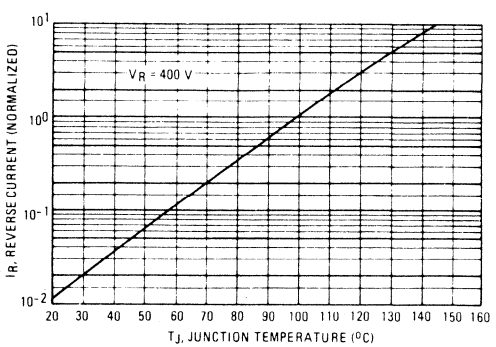


FIGURE 24 – TYPICAL REVERSE LEAKAGE



MR850 MR851 MR852 MR854 MR856

Designers Data Sheet

SUBMINIATURE SIZE, AXIAL LEAD MOUNTED FAST RECOVERY POWER RECTIFIERS

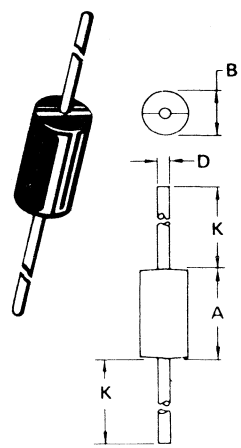
. . . designed for special applications such as dc power supplies, inverters, converters, ultrasonic systems, choppers, low RF interference and free wheeling diodes. A complete line of fast recovery rectifiers having typical recovery time of 150 nanoseconds providing high efficiency at frequencies to 250 kHz.

Designer's Data for "Worst Case" Conditions

The Designers Data sheets permit the design of most circuits entirely from the information presented. Limit curves – representing boundaries on device characteristics – are given to facilitate "worst case" design.

FAST RECOVERY POWER RECTIFIERS

50-600 VOLTS
3 AMPERE



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.65	0.370	0.380
B	4.83	5.33	0.190	0.210
D	1.22	1.32	0.048	0.052
K	26.97	27.23	1.062	1.072

CASE 267-01

MAXIMUM RATINGS

Rating	Symbol	MR850	MR851	MR852	MR854	MR856	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	400	600	Volts
Non-Repetitive Peak Reverse Voltage	V_{RSM}	75	150	250	450	650	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	35	70	140	280	420	Volts
Average Rectified Forward Current (Single phase resistive load, T_A = 90°C) (1)	I_O	3.0					Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions)	I_{FSM}	100 (one cycle)					Amp
Operating and Storage Junction Temperature Range (2)	T_J,T_{stg}	-65 to +175					°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient (Recommended Printed Circuit Board Mouting, See Note 6, Page 8)	$R_{\theta JA}$	28	°C W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Instantaneous Forward Voltage (i_F = 9.4 Amp, T_J = 175°C)	v_F	-	0.9	1.1	Volts
Forward Voltage (I_F = 3.0 Amp, T_J = 25°C)	V_F		1.04	1.25	Volts
Reverse Current (rated dc voltage) T_J = 25°C	I_R	-	2.0	10	µA
T_J = 100°C MR850		-	-	150	
T_J = 100°C MR851		-	60	150	
T_J = 100°C MR852		-	-	200	
T_J = 100°C MR854		-	-	250	
T_J = 100°C MR856		-	100	300	

REVERSE RECOVERY CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Recovery Time (I_F = 1.0 Amp to V_R = 30 Vdc, Figure 25) (I_F = 15 Amp, di/dt = 10 A/µs, Figure 26)	t_{rr}	- -	150 200	200 300	ns
Reverse Recovery Current (I_F = 1.0 Amp to V_R = 30 Vdc, Figure 25)	$I_{RM(REC)}$	-	-	2.0	Amp

(1) Must be derated for reverse power dissipation. See Note 2, Page 4.
(2) Derate as shown in Figure 1

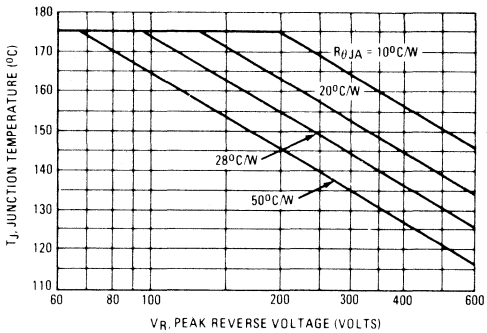
MECHANICAL CHARACTERISTICS

Case: Void Free, Transfer Molded
Finish: External Leads are Plated, Leads are readily Solderable
Polarity: Cathode Indicated by Polarity Band
Weight: 1.1 Grams (Approximately)
Maximum Lead Temperature for Soldering Purposes:
300°C, 1/8" from case for 10 s at 5.0 lb. tension

7

MAXIMUM CURRENT AND TEMPERATURE RATINGS

FIGURE 1 – MAXIMUM ALLOWABLE JUNCTION TEMPERATURE



NOTE 1
MAXIMUM JUNCTION TEMPERATURE DERATING

When operating this rectifier at junction temperatures over 120°C, reverse power dissipation and the possibility of thermal runaway must be considered. The data of Figure 1 is based upon worst case reverse power and should be used to derate $T_{J(max)}$ from its maximum value of 175°C. See Note 2 for additional information on derating for reverse power dissipation.

When current ratings are computed from $T_{J(max)}$ and reverse power dissipation is also included, ratings vary with reverse voltage as shown on Figures 2 thru 5.

RESISTIVE LOAD RATINGS

Printed Circuit Board Mounting – See Note 6, Page 8

FIGURE 2 – SINE WAVE INPUT

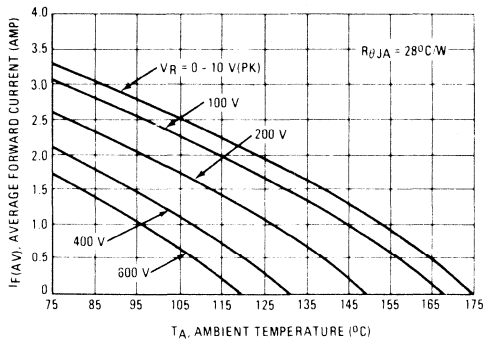


FIGURE 3 – SQUARE WAVE INPUT

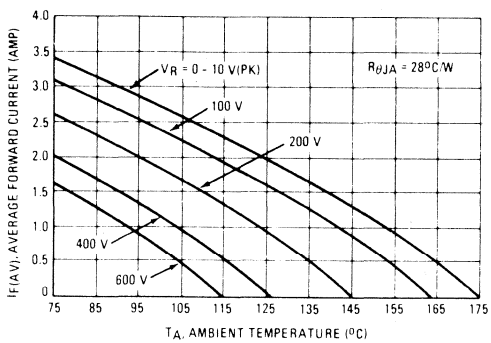


FIGURE 4 – SINE WAVE INPUT

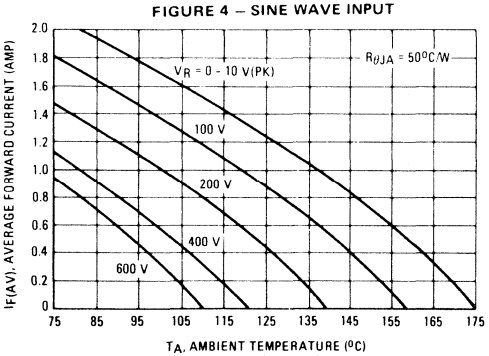
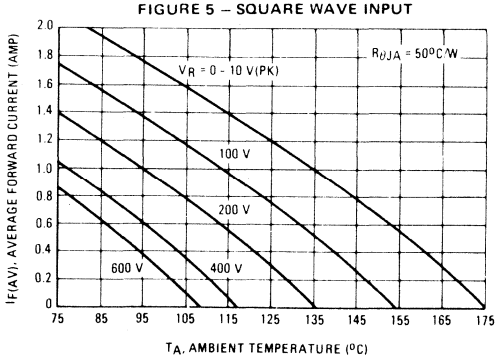


FIGURE 5 – SQUARE WAVE INPUT



MAXIMUM CURRENT RATINGS

Current derating data is based upon the thermal response data of Figure 29 and the forward power dissipation data of Figures 19 and 20. Since reverse power dissipation is not considered in Figures 6 thru 11, additional derating for reverse voltage and for junction to ambient thermal resistance must be applied. See Note 2.

SINE WAVE INPUTS

FIGURE 6 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

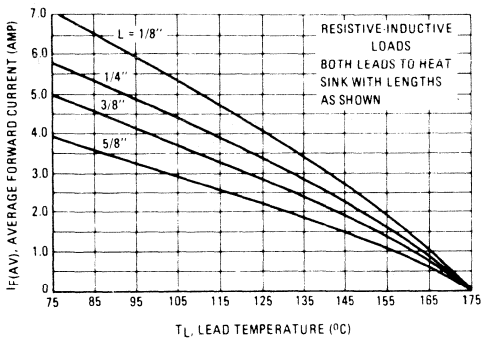


FIGURE 8 – 1/8" LEAD LENGTH, VARIOUS LOADS

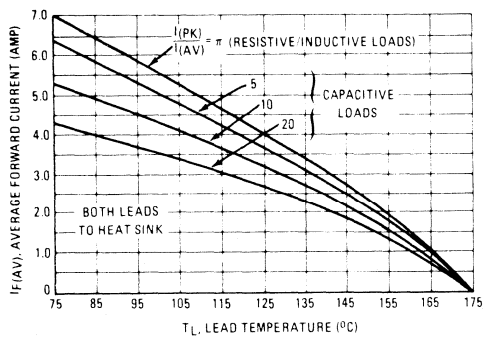
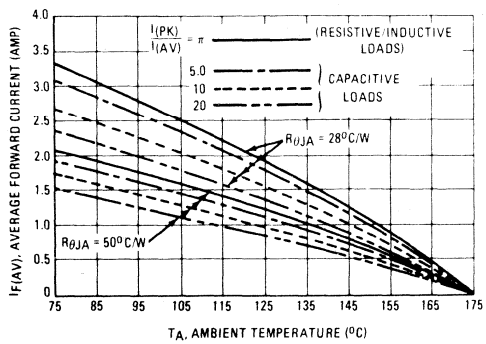


FIGURE 10 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS



SQUARE WAVE INPUTS

FIGURE 7 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

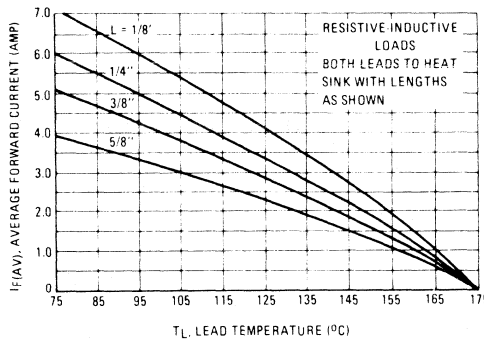


FIGURE 9 – 1/8" LEAD LENGTH, VARIOUS LOADS

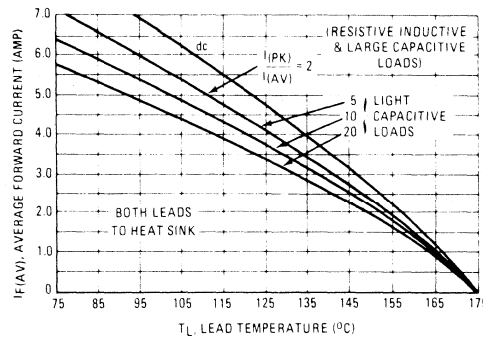
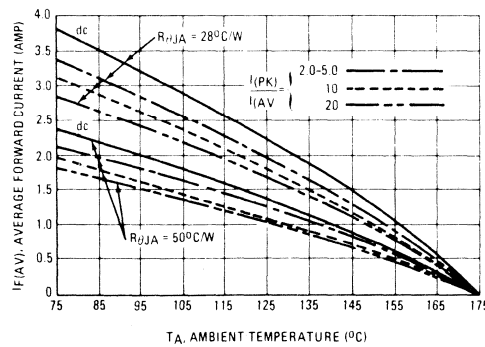


FIGURE 11 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS



7

REVERSE POWER DISSIPATION AND CURRENT

NOTE 2
DERATING FOR REVERSE POWER DISSIPATION

In this rectifier, power loss due to reverse current is generally not negligible. For reliable circuit design, the maximum junction temperature must be limited to either 175°C or the temperature which results in thermal runaway. Proper derating may be accomplished by use of equation 1 or equation 2.

Equation 1 $T_A = T_1 - (175 - T_{J(max)}) - P_R R_{\theta JA}$

Where: T_1 = Maximum Allowable Ambient Temperature neglecting reverse power dissipation (from Figures 10 or 11)

$T_{J(max)}$ = Maximum Allowable Junction Temperature to prevent thermal runaway or 175°C, whichever is lower. (See Figure 1).

P_R = Reverse Power Dissipation (From Figure 12 or 13, adjusted for $T_{J(max)}$ as shown below)

$R_{\theta JA}$ = Thermal Resistance, Junction to Ambient.

When thermal resistance, junction to ambient, is over 20°C/W, the effect of thermal response is negligible. Satisfactory derating may be found by using

Equation 2 $T_A = T_{J(max)} - (P_R + P_F) R_{\theta JA}$

P_F = Forward Power Dissipation (See Figures 19 & 20)

Other terms defined above.

The reverse power given on Figures 12 and 13 is calculated for T_J = 150°C. When T_J is lower, P_R will decrease, its value can be found by multiplying P_R by the normalized reverse current from Figure 14 at the temperature of interest.

The reverse power data is calculated for half wave rectification circuits. For full wave rectification using either a bridge or a center-tapped transformer, the data for resistive loads is equivalent when Vp is the line to line voltage across the rectifiers. For capacitive loads, it is recommended that the dc case on Figure 13 be used, regardless of input waveform, for bridge circuits. For capacitively loaded full wave center-tapped circuits, the 20:1 data of Figure 12 should be used for sine wave inputs and the capacitive load data of Figure 13 should be used for square wave inputs regardless of $I_{(pk)}/I_{(av)}$. For these two cases, Vp is the voltage across one leg of the transformer.

Example 1 Find maximum ambient temperature for I_{AV} = 2 A, capacitive load of I_{PK}/I_{AV} = 20, Input Voltage = 60 V (rms), sine wave, $R_{\theta JA}$ = 28°C/W, half wave circuit.

Solution 1 (using Equation 1)

Step 1 Find Vp: $V_P = \sqrt{2}\, V_{in} = 85$ V, $V_{R(pk)} = 170$

Step 2 Find $T_{J(max)}$ from Figure 1. Read $T_{J(max)}$ = 157°C

Step 3 Find $P_{R(max)}$ from Figure 12. Read P_R = 360 mW @ 150°C

Step 4 Find I_R normalized from Figure 14. Read $I_{R(norm)}$ = 1.5

Step 5 Correct P_R to $T_{J(max)}$: $P_R = I_{R(norm)} \times P_R$ (Figure 12) P_R = 1.5 x 360 = 540 mW

Step 6 Find $T_A = T_1$ from Figure 10. Read T_1 = 94°C

Step 7 Compute T_A from $T_A = T_1 - (175 - T_{J(max)}) - P_R R_{\theta JA}$
$T_A = 94 - (175 - 157) - (0.54)(28)$
T_A = 61°C

Solution 2 (using Equation 2)

Steps 1 thru 5 are as Solution 1

Step 6 Find P_F from Figure 19. Read P_F = 3.0 W

Step 7 Compute T_A from $T_A = T_{J(max)} - (P_R + P_F) R_{\theta JA}$
$T_A = 157 - (0.54 + 3)28$
T_A = 58°C

The discrepancy occurs because thermal response is factored into solution 1, and advantage is taken of the cooling time after the power pulse and before reverse voltage achieves its maximum. 61°C is a satisfactory ambient temperature.

FIGURE 12 – REVERSE POWER DISSIPATION, SINE WAVE

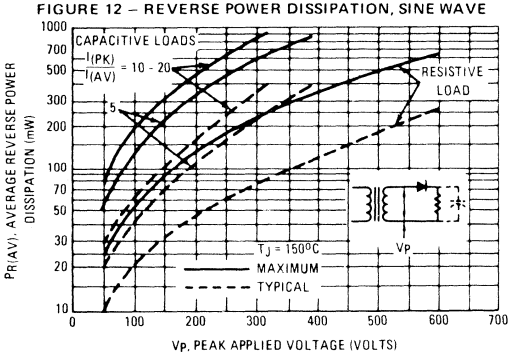


FIGURE 13 – REVERSE POWER DISSIPATION, SQUARE WAVE

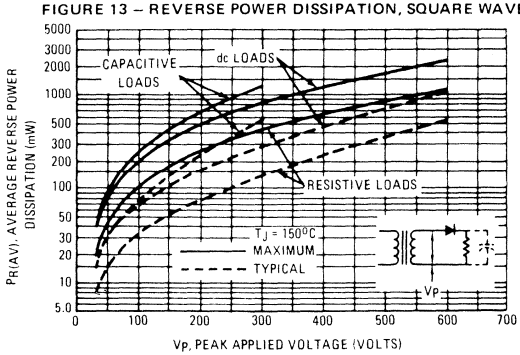


FIGURE 14 – NORMALIZED REVERSE CURRENT

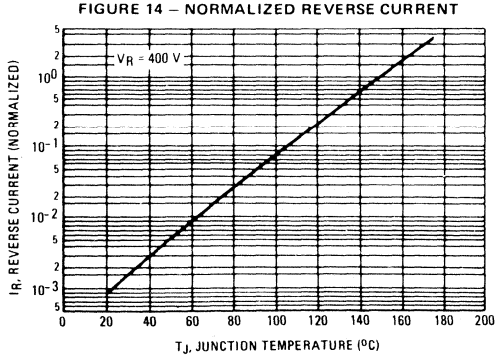
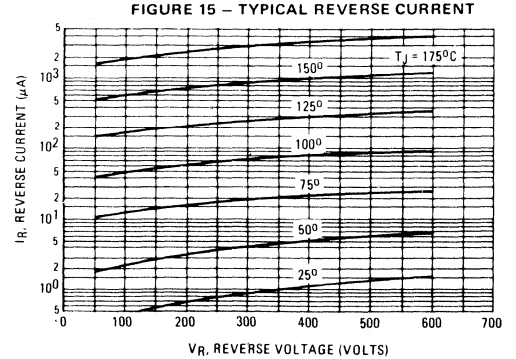


FIGURE 15 – TYPICAL REVERSE CURRENT



STATIC CHARACTERISTICS

FIGURE 16 – FORWARD VOLTAGE

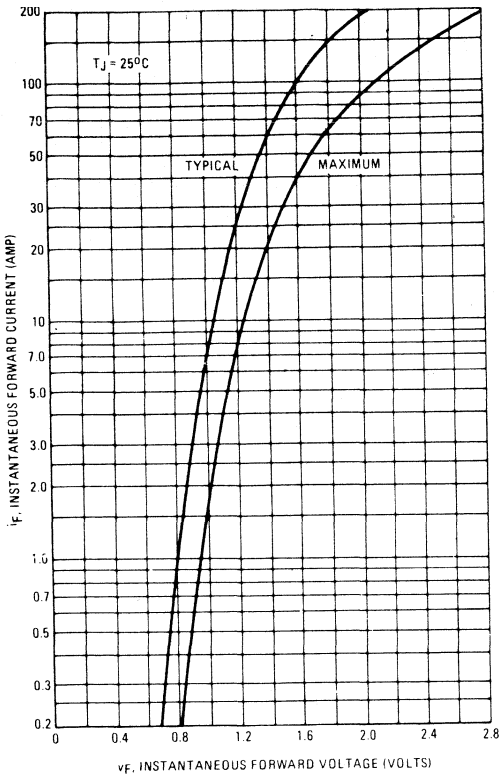


FIGURE 17 – MAXIMUM SURGE CAPABILITY

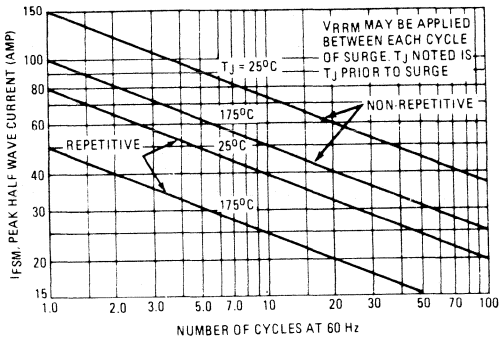
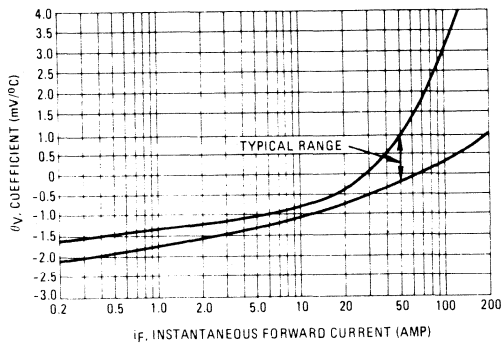
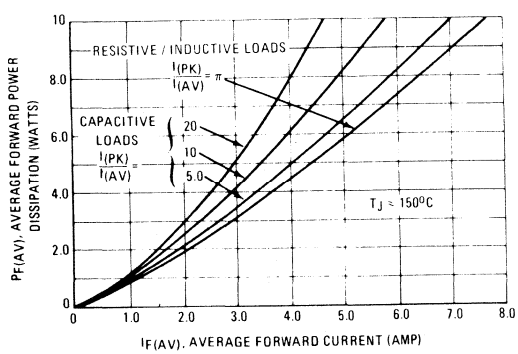


FIGURE 18 – FORWARD VOLTAGE TEMPERATURE COEFFICIENT



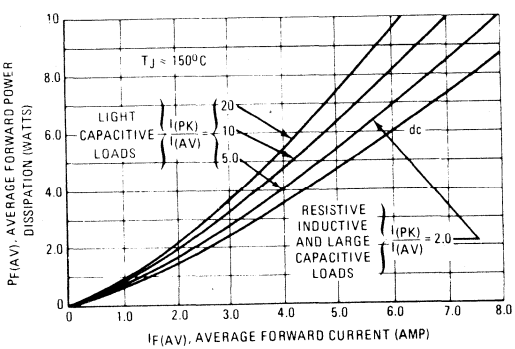
SINE WAVE INPUT

FIGURE 19 – FORWARD POWER DISSIPATION



SQUARE WAVE INPUT

FIGURE 20 – FORWARD POWER DISSIPATION



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TYPICAL RECOVERED STORED CHARAGE DATA

(See Note 3)

FIGURE 21 – T_J = 25°C

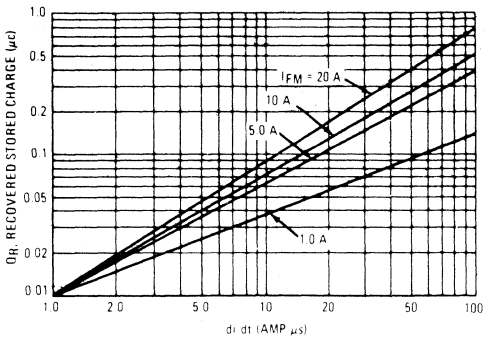


FIGURE 22 – T_J = 75°C

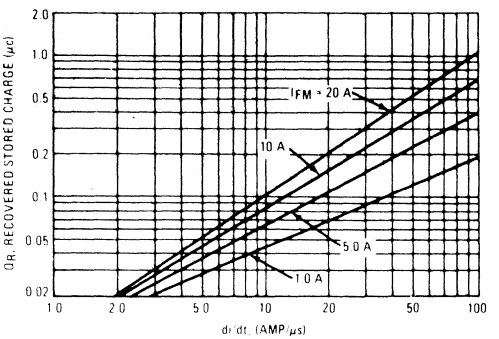


FIGURE 23 – T_J = 100°C

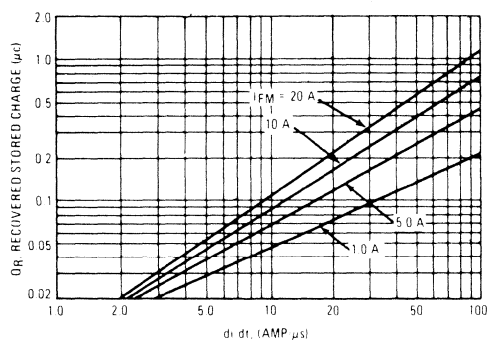
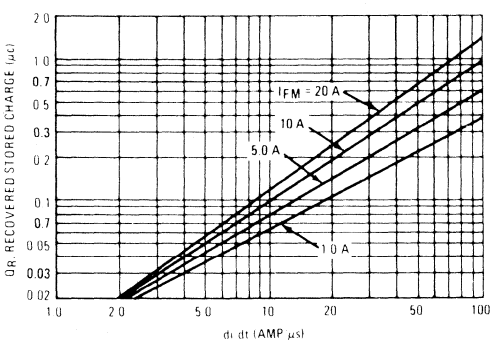


FIGURE 24 – T_J = 150°C



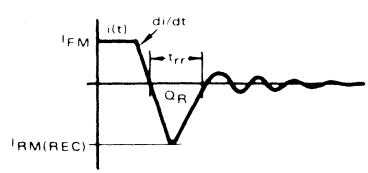
NOTE 3

Reverse recovery time is the period which elapses from the time that the current, thru a previously forward biased rectifier diode, passes thru zero going negatively until the reverse current recovers to a point which is less than 10% peak reverse current.

Reverse recovery time is a direct function of the forward current prior to the application of reverse voltage.

For any given rectifier, recovery time is very circuit dependent. Typical and maximum recovery time of all Motorola fast recovery power rectifiers are rated under a fixed set of conditions using I_F = 1.0 A, V_R = 30 V. In order to cover all circuit conditions, curves are given for typical recovered stored charge versus commutation di/dt for various levels of forward current and for junction temperatures of 25°C, 75°C, 100°C, and 150°C.

To use these curves, it is necessary to know the forward current level just before commutation, the circuit commutation di/dt, and the operating junction temperature. The reverse recovery test current waveform for all Motorola fast recovery rectifiers is shown.



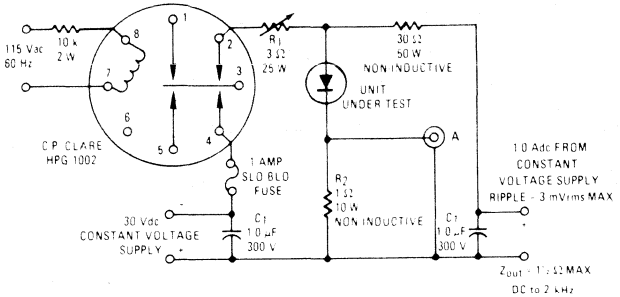
From stored charge curves versus di/dt, recovery time (t_{rr}) and peak reverse recovery current ($I_{RM(REC)}$) can be closely approximated using the following formulas:

$$t_{rr} = 1.41 \times \left[\frac{Q_R}{di/dt}\right]^{1/2}$$

$$I_{RM(REC)} = 1.41 \times \left[Q_R \times di/dt\right]^{1/2}$$

DYNAMIC CHARACTERISTICS

FIGURE 25 – REVERSE RECOVERY CIRCUIT



MINIMIZE ALL LEAD LENGTHS

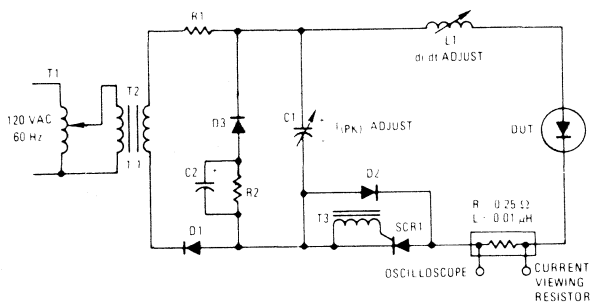
A TEKTRONIX 545A K PLUG IN PRE AMP, P6000 PROBE OR EQUIVALENT

R_1 ADJUSTED FOR 1.4 Ω BETWEEN POINT 2 OF RELAY AND RECTIFIER INDUCTANCE = 38 μH

R_2 TEN 1 W, 10 Ω, 1% CARBON CORE IN PARALLEL

$T_A = 25\ ^{+10}_{0}\ ^{\circ}C$ FOR RECTIFIER

FIGURE 26 – JEDEC REVERSE RECOVERY CIRCUIT



R1 = 50 Ohms
R2 = 250 Ohms
D1 = 1N4723
D2 = 1N4001
D3 = 1N4934
SCR1 = MCR729-10
C1 = 0.5 to 50 μF
C2 = 4000 μF
L1 = 1.0 – 27 μH

T1 Variac Adjusts $I_{(PK)}$ and di/dt
T2 = 1:1
T3 = 1:1 (to trigger circuit)

FIGURE 27 – FORWARD RECOVERY TIME

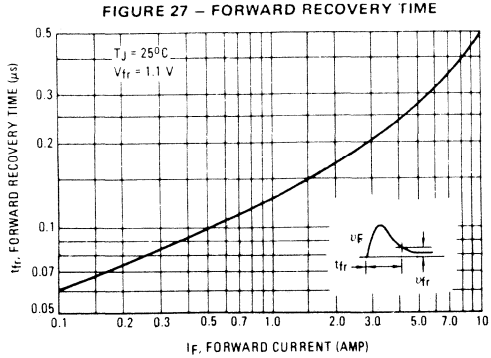


FIGURE 28 – JUNCTION CAPACITANCE

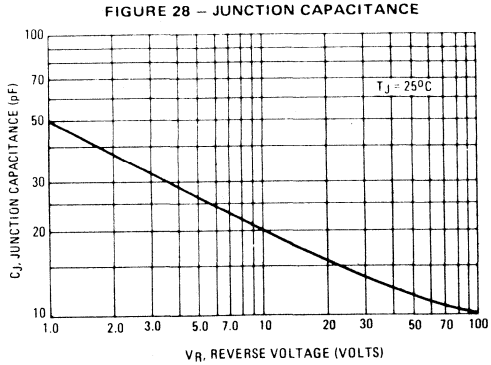


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FIGURE 29 – THERMAL RESPONSE

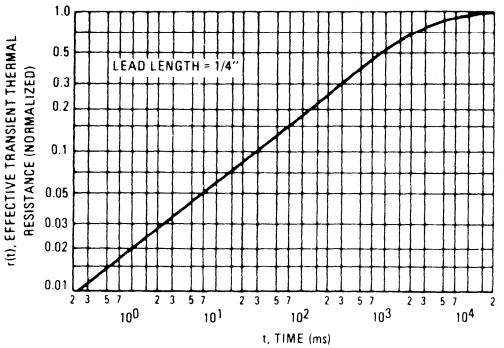
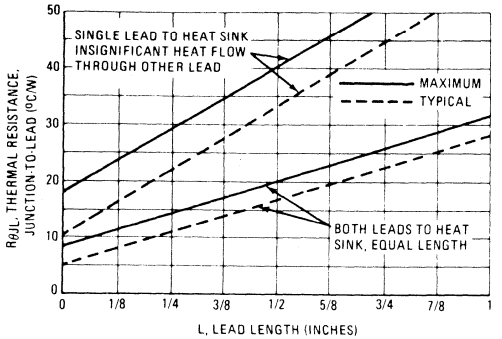


FIGURE 30 – STEADY-STATE THERMAL RESISTANCE



NOTE 4

To determine maximum junction temperature of the diode in a given situation, the following procedure is recommended.

The temperature of the lead should be measured using a thermocouple placed on the lead as close as possible to the tie point. The thermal mass connected to the tie point is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady state conditions are achieved. Using the measured value of T_L, the junction temperature may be determined by:

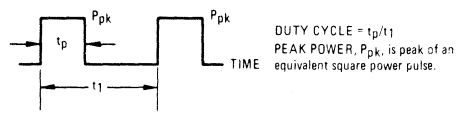
$$T_J = T_L + \Delta T_{JL}$$

where ΔT_{JL} is the increase in junction temperature above the lead temperature. It may be determined by:

$$\Delta T_{JL} = P_{pk} \cdot R_{\theta JL} [D + (1 - D) \cdot r(t_1 + t_p) + r(t_p) - r(t_1)]$$

where $r(t)$ = normalized value of transient thermal resistance at time t from Figure 29, i.e.:

$r(t_1 + t_p)$ = normalized value of transient thermal resistance at time $t_1 + t_p$.



DUTY CYCLE = t_p/t_1

PEAK POWER, P_{pk}, is peak of an equivalent square power pulse.

NOTE 5

Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heat sink. Terms in the model signify:

T_A = Ambient Temperature
T_L = Lead Temperature
T_C = Case Temperature
T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_D = Total Power Dissipation = $P_F + P_R$
P_F = Forward Power Dissipation
P_R = Reverse Power Dissipation

(Subscripts A and K refer to anode and cathode sides respectively.) Values for thermal resistance components are:

$R_{\theta L}$ = 46°C/W/IN. Typically and 48°C/W/IN Maximum.
$R_{\theta J}$ = 10°C/W Typically and 16°C/W Maximum.

The maximum lead temperature may be found as follows:

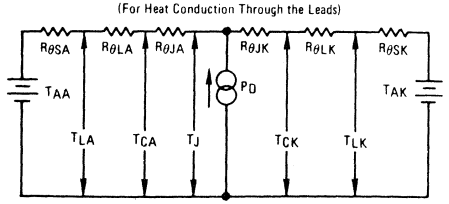
$$T_L = T_{J(max)} - \Delta T_{JL}$$

where

ΔT_{JL} can be approximated as follows:

$\Delta T_{JL} \approx R_{\theta JL} \cdot P_D$. P_D is the sum of forward and reverse power dissipation shown in Figures 2 and 4 for sine wave operation and Figures 3 and 5 for square wave operation.

THERMAL CIRCUIT MODEL
(For Heat Conduction Through the Leads)



NOTE 6

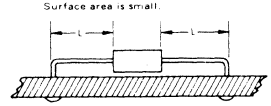
Data shown for thermal resistance junction-to-ambient ($R_{\theta JA}$) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

TYPICAL VALUES FOR $R_{\theta JA}$ IN STILL AIR

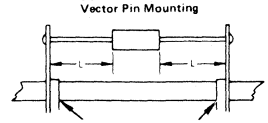
MOUNTING METHOD	LEAD LENGTH, L (IN)				$R_{\theta JA}$
	1/8	1/4	1/2	3/4	
1	50	51	53	55	°C/W
2	58	59	61	63	°C/W
3	28				°C/W

MOUNTING METHOD 1

P.C. Board Where Available Copper Surface area is small.

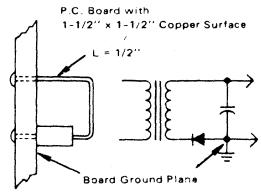


MOUNTING METHOD 2
Vector Pin Mounting



MOUNTING METHOD 3

P.C. Board with 1-1/2" x 1-1/2" Copper Surface



MR 910 SERIES

Designers Data Sheet

SUBMINIATURE SIZE, AXIAL LEAD MOUNTED FAST RECOVERY POWER RECTIFIERS

. . . designed for special applications such as dc power supplies, inverters, converters, ultrasonic systems, choppers, low RF interference and free wheeling diodes. A complete line of fast recovery rectifiers having typical recovery time of 500 nanoseconds providing high efficiency at frequencies to 100 kHz.

FAST RECOVERY POWER RECTIFIERS

50-1000 VOLTS
3 AMPERE

MAXIMUM RATINGS

Rating	Symbol	MR 910	MR 911	MR 912	MR 914	MR 916	MR 917	MR 918	Units
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	400	600	800	1000	Volts
Non-Repetitive Peak Reverse Voltage	V_{RSM}	100	200	300	525	800	1000	1200	Volts
Average Rectified Forward Current (Single phase resistive load, T_A = 90°C)	I_O	3.0							Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions)	I_{FSM}	100 (one cycle)							Amp
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +175							°C

THERMAL CHARACTERISTICS

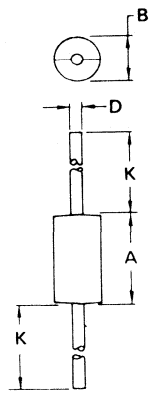
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	28	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Instantaneous Forward Voltage (I_F = 9.4 Amp, T_J = 175°C)	v_F	–	0.9	1.1	Volts
Forward Voltage (I_F = 3.0 Amp, T_J = 25°C)	V_F	–	1.04	1.25	Volts
Reverse Current (rated dc voltage) T_J = 25°C	I_R	–		10	μA
T_J = 100°C		–	–	300	μA

REVERSE RECOVERY CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Recovery Time (I_F = 1.0 Amp to V_R = 30 Vdc	t_{rr}	–		750	ns
Reverse Recovery Current (I_F = 1.0 Amp to V_R = 30 Vdc	$I_{RM(REC)}$	–	–	3.0	Amp



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.65	0.370	0.380
B	4.83	5.33	0.190	0.210
D	1.22	1.32	0.048	0.052
K	26.97	27.23	1.062	1.072

CASE 267-01

MECHANICAL CHARACTERISTICS

Case: Void Free, Transfer Molded
Finish: External Leads are Plated, Leads are readily Solderable
Polarity: Indicated by Cathode Band

Weight: 1.1 Grams (Approximately)
Maximum Lead Temperature for Soldering Purposes:
240°C, 1/8" from case for 10 s at 5.0 lb. tension

7

STATIC CHARACTERISTICS

FIGURE 1 – FORWARD VOLTAGE

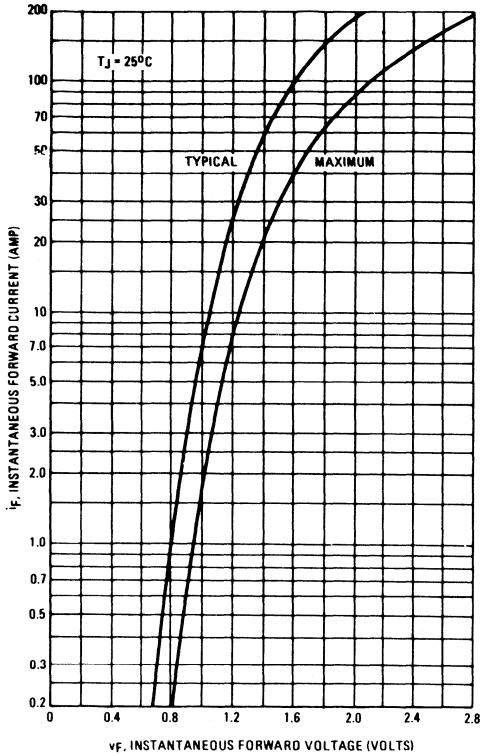


FIGURE 2 – MAXIMUM SURGE CAPABILITY

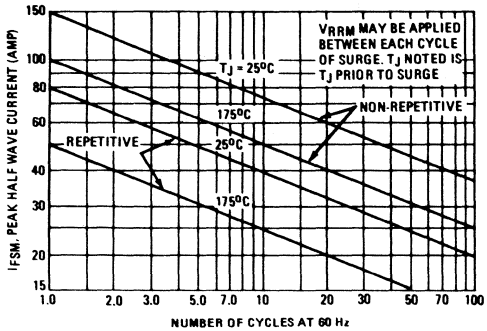
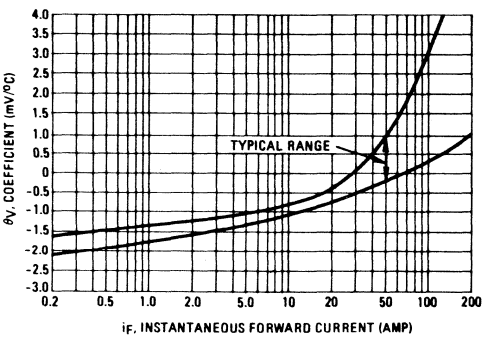
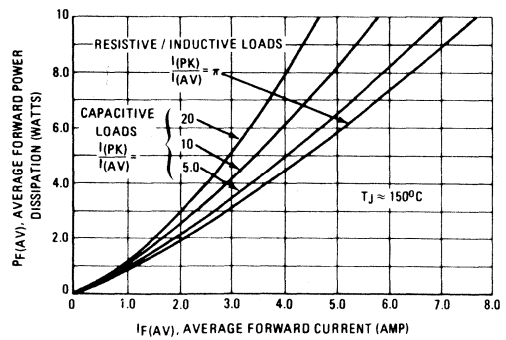


FIGURE 3 – FORWARD VOLTAGE TEMPERATURE COEFFICIENT



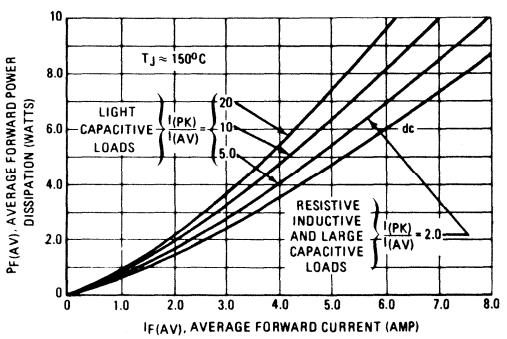
SINE WAVE INPUT

FIGURE 4 – FORWARD POWER DISSIPATION



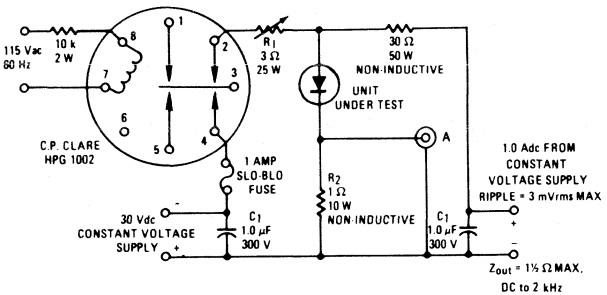
SQUARE WAVE INPUT

FIGURE 5 – FORWARD POWER DISSIPATION



DYNAMIC CHARACTERISTICS

FIGURE 6 – REVERSE RECOVERY CIRCUIT



MINIMIZE ALL LEAD LENGTHS

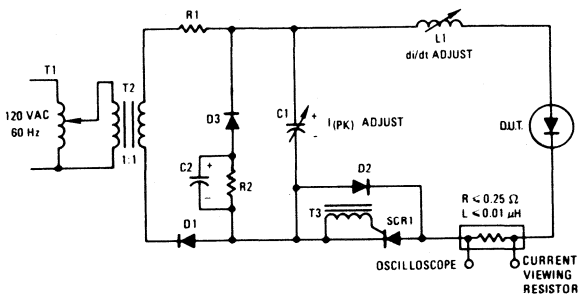
A – TEKTRONIX 545A, K PLUG IN PRE-AMP, P6000 PROBE OR EQUIVALENT

R_1 – ADJUSTED FOR 1.4 Ω BETWEEN POINT 2 OF RELAY AND RECTIFIER INDUCTANCE ≈ 38 μH

R_2 – TEN-1 W, 10 Ω, 1% CARBON CORE IN PARALLEL

$T_A = 25\ ^{+10}_{-0}$ °C FOR RECTIFIER

FIGURE 7 – JEDEC REVERSE RECOVERY CIRCUIT



R1 = 50 Ohms
R2 = 250 Ohms
D1 = 1N4723
D2 = 1N4001
D3 = 1N4934
SCR1 = MCR729-10
C1 = 0.5 to 50 μF
C2 = 4000 μF
L1 = 1.0 - 27 μH

T1 = Variac Adjusts $I_{(PK)}$ and di/dt
T2 = 1:1
T3 = 1:1 (to trigger circuit)

FIGURE 8 – FORWARD RECOVERY TIME

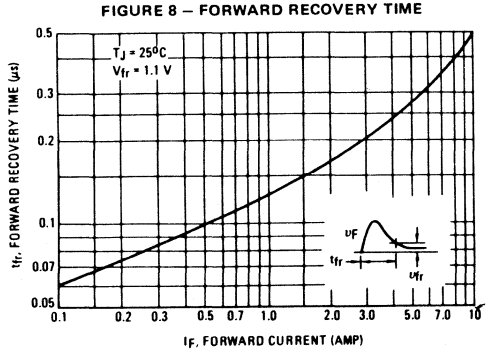
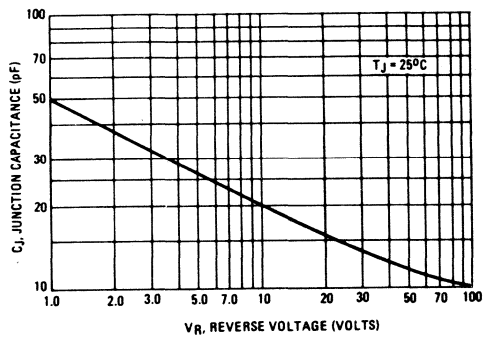


FIGURE 9 – JUNCTION CAPACITANCE



7

FIGURE 10 – THERMAL RESPONSE

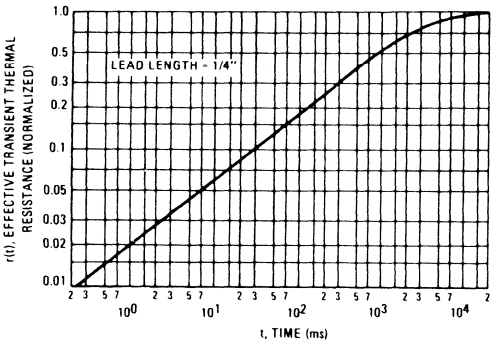
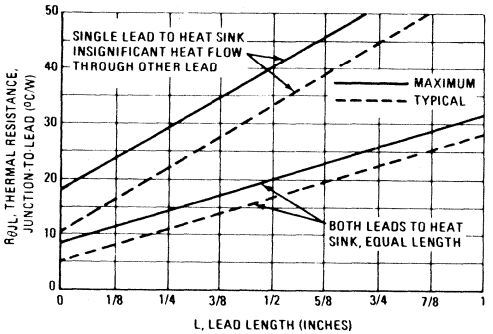


FIGURE 11 – STEADY STATE THERMAL RESISTANCE



NOTE 1

To determine maximum junction temperature of the diode in a given situation, the following procedure is recommended:

The temperature of the lead should be measured using a thermocouple placed on the lead as close as possible to the tie point. The thermal mass connected to the tie point is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady-state conditions are achieved. Using the measured value of T_L, the junction temperature may be determined by:

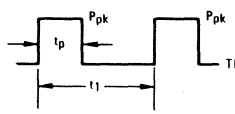
$$T_J = T_L + \Delta T_{JL}$$

where ΔT_{JL} is the increase in junction temperature above the lead temperature. It may be determined by:

$$\Delta T_{JL} = P_{pk} \cdot R_{\theta JL} [D + (1 - D) \cdot r(t_1 + t_p) + r(t_p) - r(t_1)]$$

where r(t) = normalized value of transient thermal resistance at time t from Figure 29, i.e.

$r(t_1 + t_p)$ = normalized value of transient thermal resistance at time $t_1 + t_p$



DUTY CYCLE = t_p/t_1

PEAK POWER, P_{pk}, is peak of an equivalent square power pulse.

NOTE 2

Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heat sink. Terms in the model signify:

T_A = Ambient Temperature
T_L = Lead Temperature
T_C = Case Temperature
T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_D = Total Power Dissipation = $P_F + P_R$
P_F = Forward Power Dissipation
P_R = Reverse Power Dissipation

(Subscripts A and K refer to anode and cathode sides respectively.) Values for thermal resistance components are:

$R_{\theta L}$ = 46°C/W/IN. Typically and 48°C/W/IN Maximum.
$R_{\theta J}$ = 10°C/W Typically and 16°C/W Maximum.

The maximum lead temperature may be found as follows:

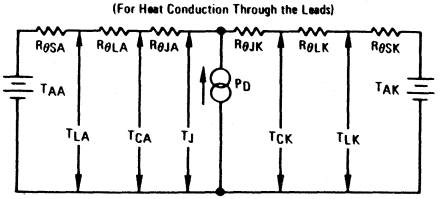
$$T_L = T_{J(max)} - \Delta T_{JL}$$

where

ΔT_{JL} can be approximated as follows:

$\Delta T_{JL} \approx R_{\theta JL} \cdot P_D$. P_D is the sum of forward and reverse power dissipation shown in Figures 2 and 4 for sine wave operation and Figures 3 and 5 for square wave operation.

THERMAL CIRCUIT MODEL
(For Heat Conduction Through the Leads)



NOTE 3

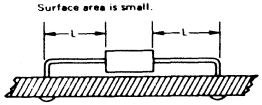
Data shown for thermal resistance junction-to-ambient ($R_{\theta JA}$) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

TYPICAL VALUES FOR $R_{\theta JA}$ IN STILL AIR

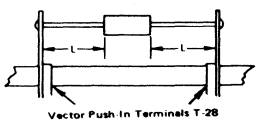
MOUNTING METHOD	LEAD LENGTH, L (IN) 1/8	1/4	1/2	3/4	$R_{\theta JA}$
1	50	51	53	55	°C/W
2	58	59	61	63	°C/W
3	28				°C/W

MOUNTING METHOD 1

P.C. Board Where Available Copper Surface area is small.

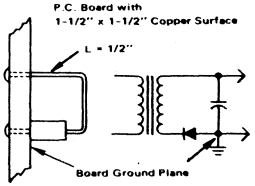


MOUNTING METHOD 2
Vector Pin Mounting



MOUNTING METHOD 3

P.C. Board with 1-1/2" x 1-1/2" Copper Surface



MV104

VVC

SILICON EPICAP▲ DIODES

. . . designed for FM tuning, general frequency control and tuning, or any top-of-the-line application requiring back-to-back diode configurations for minimum signal distortion and detuning. This device is supplied in the popular TO-92 plastic package for high volume, economical requirements of consumer and industrial applications.

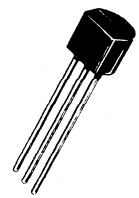
- Guaranteed Capacitance Range – 37-42 pF @ V_R = 3.0 Vdc
- Dual Diodes – Save Space and Reduce Cost
- TO-92 Package for Easy Handling and Mounting
- Guaranteed Matching* Tolerance From Diode to Diode and Group to Group
- Monolithic Chip Provides Near Perfect Matching – Guaranteed ±1% (Max) Over Specified Tuning Range.

*Upon request, diodes are available in matched sets of any number or in matched groups. All diodes in a set or group can be matched for capacitance to ±1.5% or 0.1 pF (whichever is greater) over the specified tuning range.

DUAL VOLTAGE-VARIABLE CAPACITANCE DIODES

37–42 pF

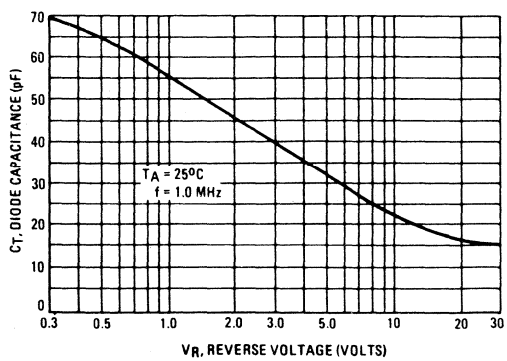
32 VOLTS

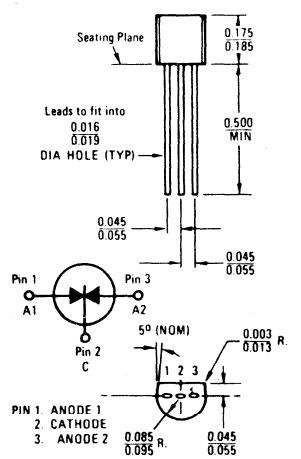


MAXIMUM RATINGS (Each Device)

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	32	Volts
Forward Current	I_F	200	mA
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	280 2.8	mW mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 1 – DIODE CAPACITANCE (Each Device)





To convert inches to millimeters multiply by 25.4

All JEDEC dimensions and notes apply

CASE 29-01 (15)
TO-92

▲Trademark of Motorola Inc.

7

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, Each Device)

Characteristic—All Types	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	BV_R	32	–	–	Vdc
Reverse Voltage Leakage Current (V_R = 30 Vdc) T_A = 25°C T_A = 60°C	I_R	– –	– –	50 500	nAdc
Series Inductance (f = 250 MHz, Lead Length ≈ 1/16")	L_S	–	6.0	–	nH
Case Capacitance (f = 1.0 MHz, Lead Length ≈ 1/16")	C_C	–	0.18	–	pF
Diode Capacitance Temperature Coefficient (V_R = 4.0 Vdc, f = 1.0 MHz)	TC_C	–	280	400	ppm/°C

	C_T, Diode Capacitance V_R = 3.0 Vdc, f = 1.0 MHz pF		Q, Figure of Merit V_R = 3.0 Vdc f = 100 MHz	C_R, Capacitance Ratio C_3/C_{30} f = 1.0 MHz	
Device	Min	Max	Min	Min	Max
MV104	37	42	100	2.5	2.8

TYPICAL CHARACTERISTICS (Each Device)

FIGURE 2 – FIGURE OF MERIT

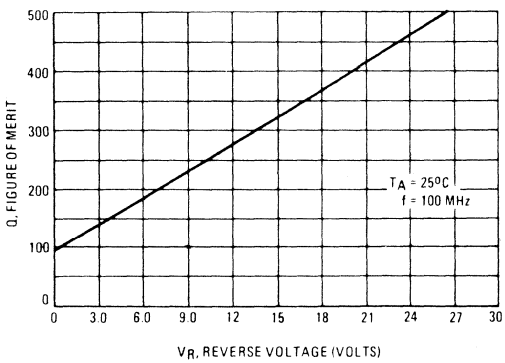


FIGURE 3 – FIGURE OF MERIT

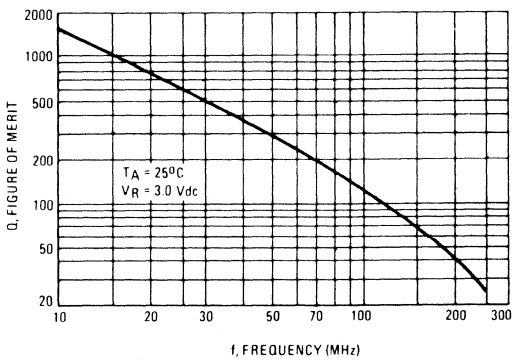


FIGURE 4 – DIODE CAPACITANCE

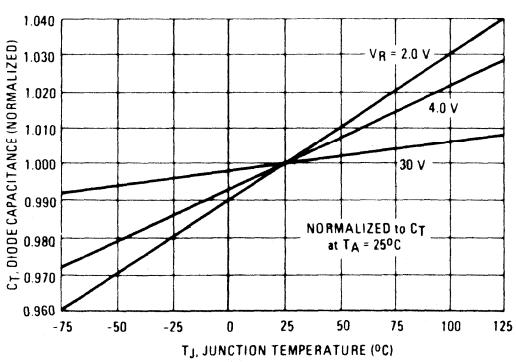
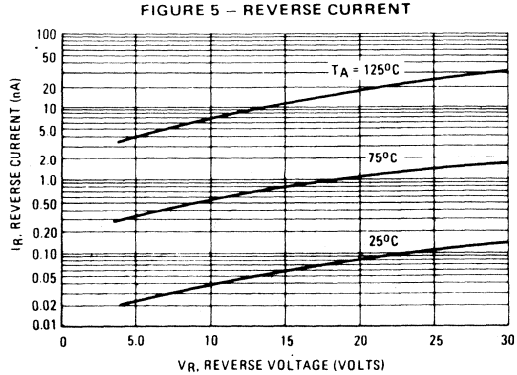


FIGURE 5 – REVERSE CURRENT



MV209

VVC

SILICON EPICAP▲ DIODE

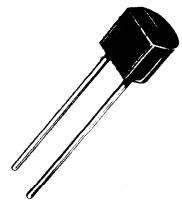
. . . designed for VHF TV tuning, AFC, general frequency control and tuning applications; providing solid-state reliability in replacement of mechanical tuning methods.

- High Q With Guaranteed Minimum Values at VHF Frequencies
- Controlled and Uniform Tuning Ratio
- Guaranteed Matching(1) Tolerance From Diode to Diode and Group to Group
- Supplied in One-Piece, Unibloc▲ Package for High Reliability.

(1) Upon request, diodes are available in matched sets of any number or in matched groups. All diodes in a set or group can be matched for capacitance to ±3% or 0.1 pF (whichever is greater) along the entire specified tuning range.

VOLTAGE VARIABLE CAPACITANCE DIODE

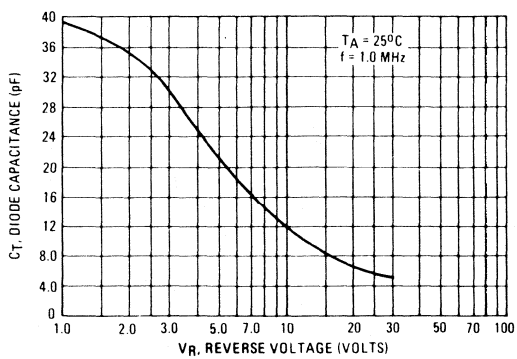
26-32 pF

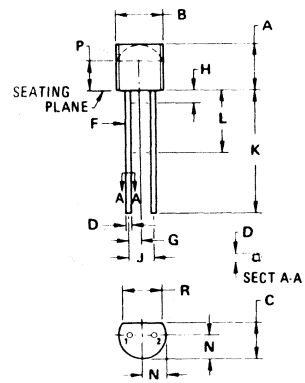


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	30	Volts
Forward Current	I_F	200	mA
Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	280 2.8	mW mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 1 – DIODE CAPACITANCE





STYLE 2:
PIN 1. CATHODE
2. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.356	0.533	0.014	0.021
F	0.407	0.482	0.016	0.019
G	1.27 BSC		0.050 BSC	
H	–	1.27	–	0.050
J	2.54 BSC		0.100 BSC	
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.66	0.080	0.105
P	2.93	–	0.115	–
R	3.43	–	0.135	–

All JEDEC dimensions and notes apply.

CASE 182-02

▲Trademark of Motorola Inc.

7

ELECTRICAL CHARACTERISTICS (T_A 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	BV_R	30	–	–	Vdc
Reverse Voltage Leakage Current (V_R = 25 Vdc)	I_R	–	–	0.1	μAdc
Series Inductance (Note 1) (f = 250 MHz, Lead Length ≈ 1/8")	L_S	–	6.0	–	nH
Case Capacitance (Note 2) (f = 1.0 MHz)	C_C	–	0.2	–	pF
Diode Capacitance Temperature Coefficient (V_R = 3.0 Vdc, f = 1.0 MHz)	TC_C	–	300	400	ppm/°C

	C_t, Diode Capacitance V_R = 3.0 Vdc, f = 1.0 MHz pF			Q, Figure of Merit V_R = 3.0 Vdc f = 50 MHz (Note 3)	C_R, Capacitance Ratio C_3/C_{25} f = 1.0 MHz (Note 4)	
Device	Min	Nom	Max	Min	Min	Max
MV209	26	29	32	200	5.0	6.5

FIGURE 2 – FIGURE OF MERIT

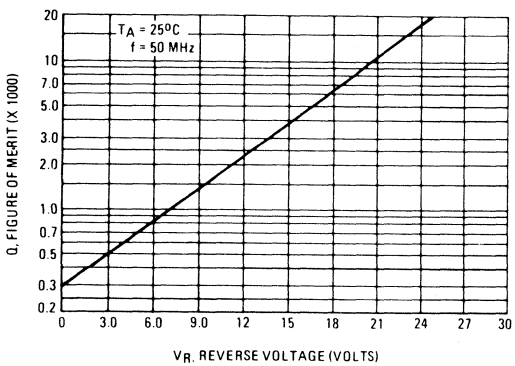


FIGURE 3 – LEAKAGE CURRENT

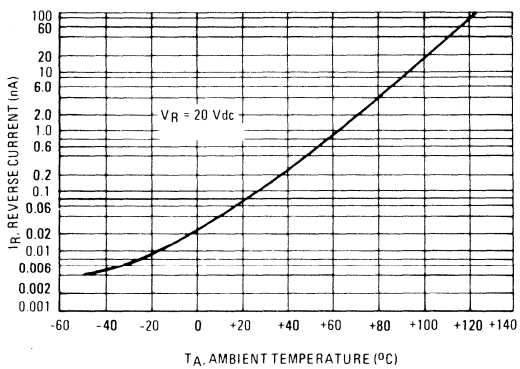
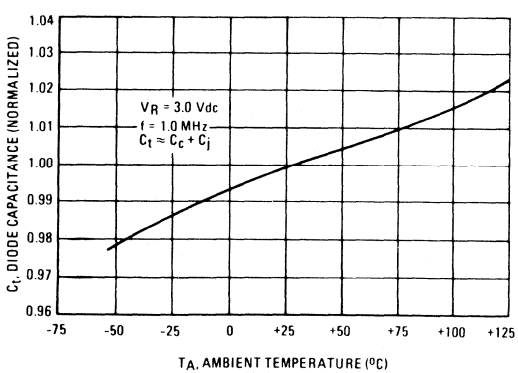


FIGURE 4 – DIODE CAPACITANCE



NOTES ON TESTING AND SPECIFICATIONS

1. L_S is measured on a package having a short instead of a die, using an impedance bridge (Boonton Radio Model 250A RX Meter).
2. C_C is measured on a package without a die, using a capacitance bridge (Boonton Electronics Model 75A or equivalent).
3. Q is calculated by taking the G and C readings of an admittance bridge, such as Boonton Electronics Model 33AS8, at the specified frequency and substituting in the following equation:

$$Q = \frac{2\pi fC}{G}$$

4. C_R is the ratio of C_t measured at 3.0 Vdc divided by C_t measured at 25 Vdc.

MVAM115
MVAM125

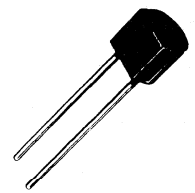
VVC

SILICON TUNING DIODE

. . . designed for electronic tuning of AM receivers.

- High Capacitance Ratio – C_R = 15 (Min)
- Guaranteed Diode Capacitance – C_t = 440 pF (Min) – 560 pF (Max) @ V_R = 1.0 Vdc, f = 1.0 MHz
- Guaranteed Figure of Merit – Q = 150 (Min) @ V_R = 1.0 Vdc, f = 1.0 MHz

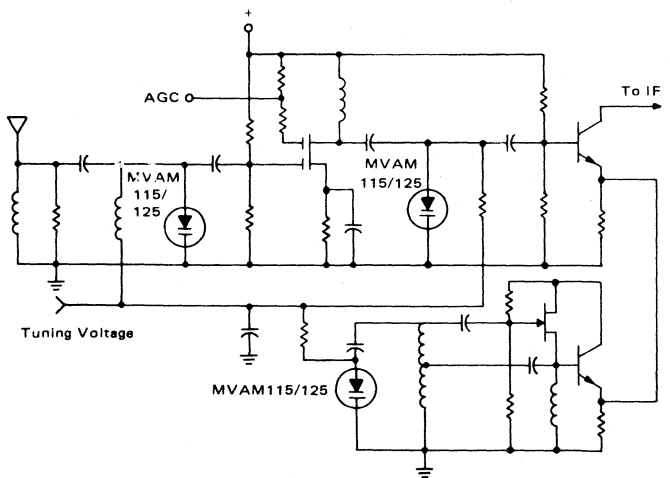
VARACTOR DIODES FOR AM TUNING

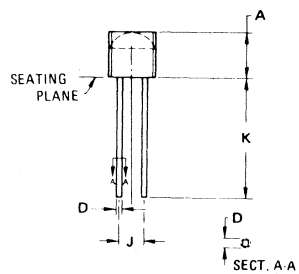


MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Reverse Voltage	MVAM125 MVAM115	V_R	28 18	Volts
Forward Current		I_F	50	mA
Power Dissipation @ T_A = 25°C Derate above 25°C		P_D	280 2.8	mW mW/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	-65 to +125	°C

FIGURE 1 – TYPICAL AM RADIO APPLICATION





STYLE 1:
PIN 1. ANODE
2. CATHODE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.45	4.70	0.175	0.185
D	0.41	0.48	0.016	0.019
J	2.29	2.79	0.090	0.110
K	12.70	–	0.500	–

CASE 182-03

7

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, Each Device)

Characteristic – All Types		Symbol	Min	Typ	Max	Unit
Breakdown Voltage (I_R = 10 μAdc)	MVAM125 MVAM115	$V_{(BR)}$	28 18	– –	– –	Vdc
Reverse Current (V_R = 25 V) (V_R = 15 V)	 MVAM125 MVAM115	I_R	–	–	100	nAdc
Diode Capacitance Temperature Coefficient (1) (V_R = 1.0 Vdc, f = 1.0 MHz, T_A = -40°C to +85°C)		TC_C	–	435	–	ppm/°C
Case Capacitance (f = 1.0 MHz, Lead Length 1/16")		C_C	–	0.18	–	pF
Diode Capacitance (2) (V_R = 1.0 Vdc, f = 1.0 MHz)		C_t	440	500	560	pF
Figure of Merit (V_R = 1.0 Vdc, f = 1.0 MHz)		Q	150	–	–	–
Capacitance Ratio (f = 1.0 MHz)	MVAM115 MVAM125	C1/C15 C1/C25	15 15	– –	– –	–

Notes:

(1) The effect of increasing temperature 1.0°C, at any operating point, is equivalent to lowering the effective tuning voltage 1.25 mV. The percent change of capacitance per °C is nearly constant from -40°C to +100°C.

(2) Upon request, diodes are available in matched sets. All diodes in a set can be matched for capacitance to ± 1.5% or 0.1 pF (whichever is greater) at all points along the specified tuning range.

FIGURE 2 – CAPACITANCE versus REVERSE VOLTAGE

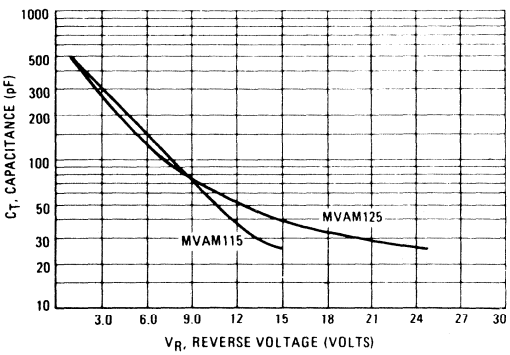
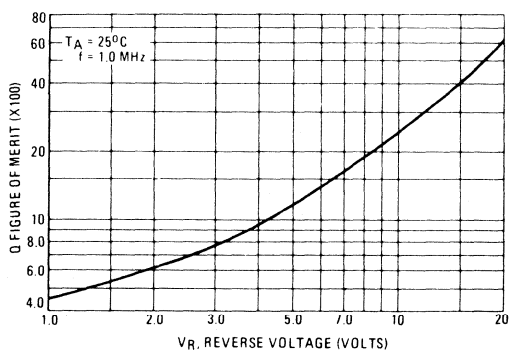


FIGURE 3 – FIGURE OF MERIT



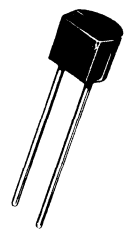
MVS240

MONOLITHIC TEMPERATURE COMPENSATED VOLTAGE REFERENCE DIODE

Highly reliable temperature compensated monolithic integrated circuit voltage stabilizer designed for use in television and FM radios that use variable capacitance diode tuners.

- Low Dynamic Operating Impedance
- Low Operating Voltage Change over Temperature Range
- $\frac{\triangle V_Z}{\triangle T}$ = -0.20 mV/°C (Typ) @ I_{ZT} = 5.0 mA

24 VOLT STABILIZER



MAXIMUM RATINGS

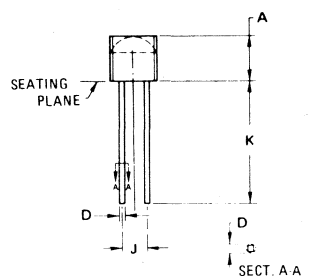
Rating	Symbol	Value	Unit
Operating Current for 24 Vz	I_Z	26	mA
Power Dissipation @ T_A = 25°C	P_D	625	mW
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.083	°C/mW
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	0.200	°C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Voltage (I_{ZT} = 5.0 mA)	V_Z	23	24	25	Volts
Operating Voltage Change (I_{ZT} = 5.0 mA, 0 to 70°C)	$\frac{\Delta V_Z}{\Delta T}$	-1.55	-0.20	+1.55	mV/°C
Operating Dynamic Impedance (I_Z = 5.0 mA)	Z_z	–	9.0	25	Ohms



STYLE 1:
PIN 1. ANODE
2. CATHODE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.45	4.70	0.175	0.185
D	0.41	0.48	0.016	0.019
J	2.29	2.79	0.090	0.110
K	12.70	–	0.500	–

CASE 182-03

7

FIGURE 1 – POWER DERATING

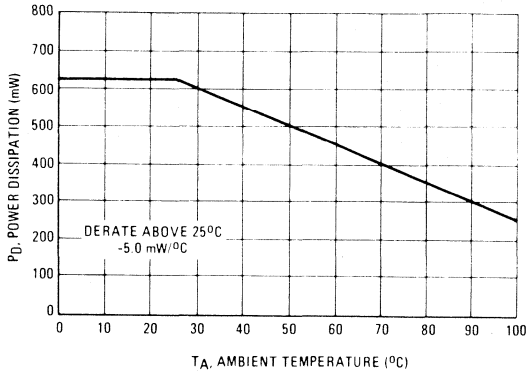


FIGURE 2 – CURRENT DERATING

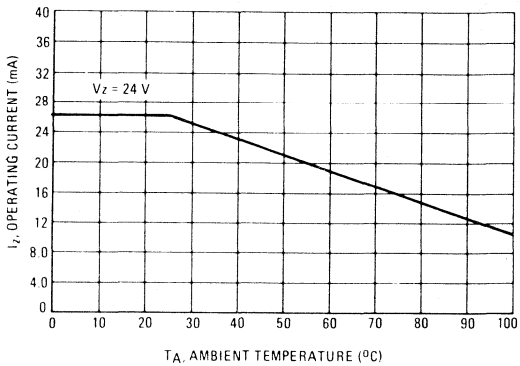


FIGURE 3 – OPERATING VOLTAGE CHANGE

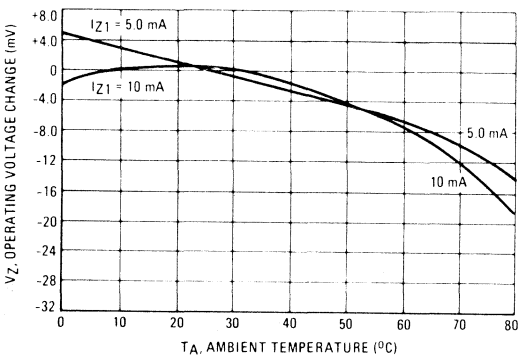


FIGURE 4 – OPERATING VOLTAGE CHANGE TEST CIRCUIT

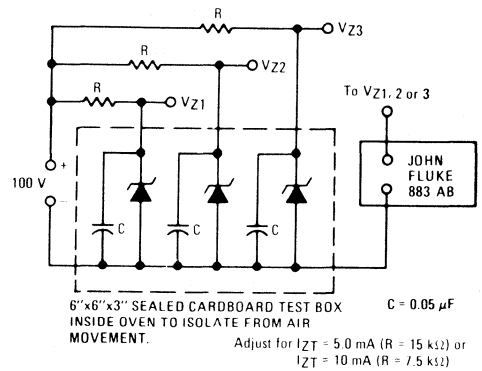


FIGURE 5 – OPERATING IMPEDANCE TEST CIRCUIT

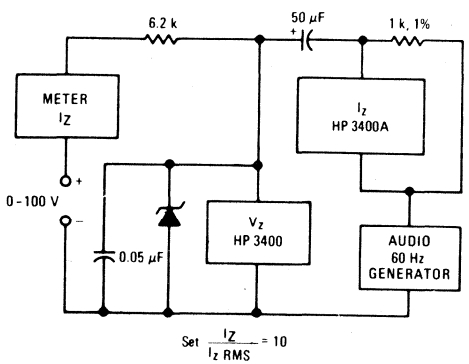
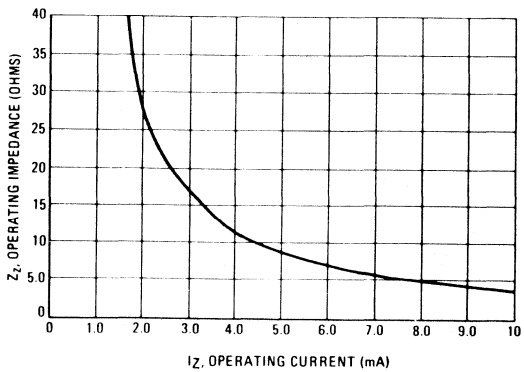


FIGURE 6 – OPERATING IMPEDANCE



MVS460

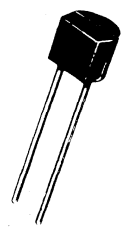
MONOLITHIC TEMPERATURE COMPENSATED VOLTAGE REFERENCE DIODE

Highly reliable temperature compensated monolithic integrated circuit voltage stabilizer designed for use in television and FM radios that use variable capacitance diode tuners.

- Low Dynamic Operating Impedance
- Low Operating Voltage Change over Temperature Range
- Available in the Following Voltage Ranges:

31 to 32 volts	MVS460-1	red top
32 to 34 volts	MVS460-2	yellow top
34 to 35 volts	MVS460-3	green top

TUNING DIODE REGULATOR



MAXIMUM RATINGS

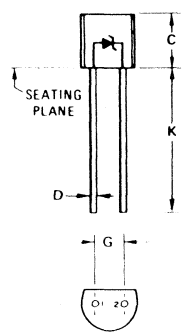
Rating	Symbol	Value	Unit
Operating Current for 33 V_Z	I_Z	18	mA
Power Dissipation @ $T_A = 25^oC$	P_D	625	mW
Operating Junction Temperature	T_J	150	^oC
Storage Temperature Range	T_{stg}	-40 to +150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.083	$^oC/mW$
Thermal Resistance, Junction to Ambient	θ_{JA}	0.200	$^oC/mW$

ELECTRICAL CHARACTERISTICS ($T_A = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Voltage (I_{ZT} = 5.0 mA)	V_Z	31	33	35	Volts
Operating Voltage Change (I_{ZT} = 5.0 mA, 0 to 70°C)	$\frac{\Delta V_Z}{\Delta T}$	-3.1	-2.3	+1.55	mV/°C
Operating Dynamic Impedance (I_Z = 5.0 mA)	Z_z	–	9.0	25	Ohms



STYLE 1
PIN 1. ANODE
2. CATHODE

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
C	0.175	0.185	4.45	4.70
D	0.016	0.019	0.406	0.483
G	0.090	0.110	2.29	2.79
K	0.594		15.09	

CASE 182-01

7

FIGURE 1 – POWER DERATING

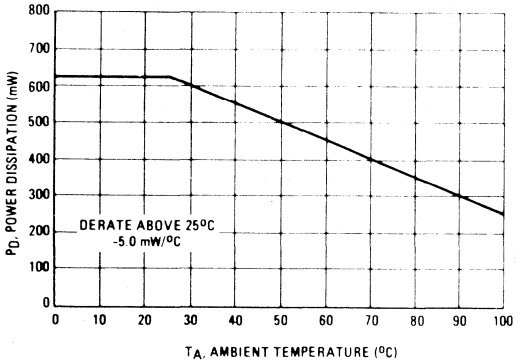


FIGURE 2 – CURRENT DERATING

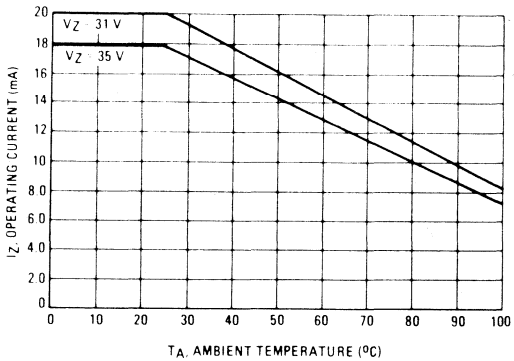


FIGURE 3 – OPERATING VOLTAGE CHANGE

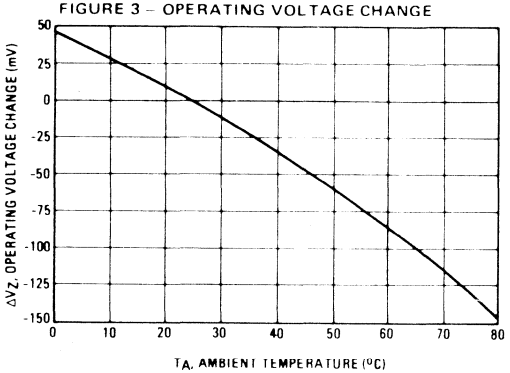


FIGURE 4 – OPERATING VOLTAGE CHANGE TEST CIRCUIT

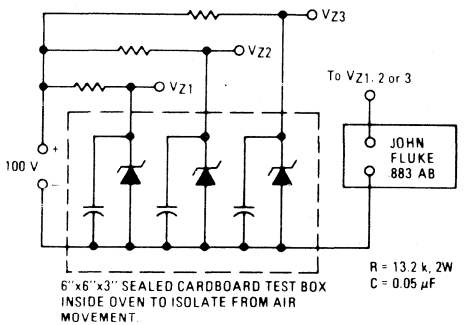


FIGURE 5 – OPERATING IMPEDANCE TEST CIRCUIT

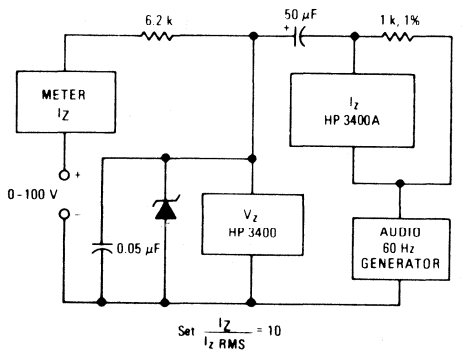
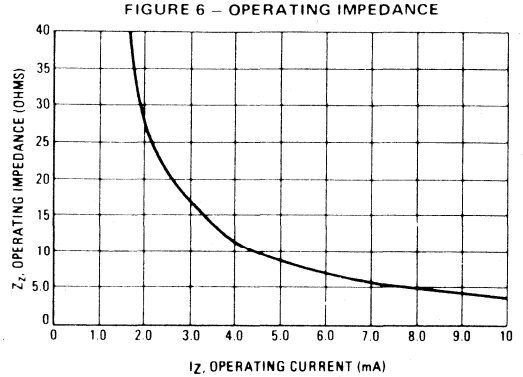


FIGURE 6 – OPERATING IMPEDANCE



MZD3.9 thru MZD200

Designers▲ Data Sheet

1.3 WATT SURMETIC▲ 30 SILICON ZENER DIODES

. . . a complete series of 1.3 Watt Zener Diodes with limits and operating characteristics that reflect the superior capabilities of silicon-oxide-passivated junctions. All this in an axial lead, transfer-molded plastic package offering protection in all common environmental conditions.

- To 80 Watts Surge Rating @ 1.0 ms
- Maximum Limits Guaranteed on Six Electrical Parameters
- Package No Larger Than the Conventional 400 mW Package

Designer's Data for "Worst Case" Conditions

The Designers▲ Data sheets permit the design of most circuits entirely from the information presented. Limit curves – representing boundaries on device characteristics – are given to facilitate "worst case" design.

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
DC Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.3 7.4	Watt mW/°C
DC Power Dissipation @ T_L = 75°C Lead Length = 10 mm Derate above 75°C	P_D	3.0 24	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

MECHANICAL CHARACTERISTICS

CASE: Void-free, transfer-molded, thermosetting plastic

FINISH: All external surfaces are corrosion resistant and leads are readily solderable and weldable

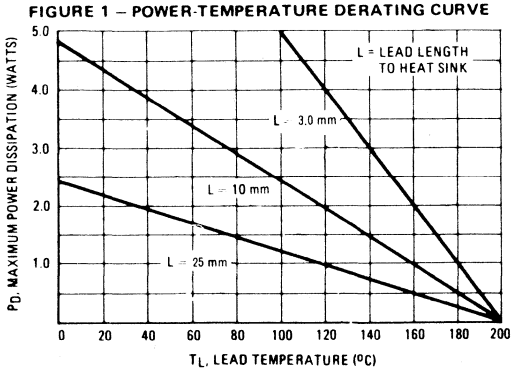
POLARITY: Cathode indicated by polarity band. When operated in zener mode, cathode will be positive with respect to anode

MOUNTING POSITION: Any

WEIGHT: 0.4 gram (approx)

Note 1: Lead Temperature not less than 2.0 mm from case for 10 seconds: 230°C.

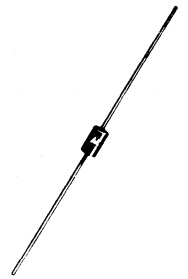
FIGURE 1 – POWER-TEMPERATURE DERATING CURVE

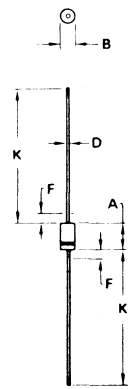


▲Trademark of Motorola Inc.

1.3 WATT, 5% ZENER REGULATOR DIODES

3.9-200 VOLTS





NOTE
1 POLARITY DENOTED BY CATHODE BAND

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.07	5.20	0.160	0.205
B	2.04	2.71	0.080	0.107
D	0.71	0.86	0.028	0.034
F	–	1.27	–	0.050
K	27.94	–	1.100	–

All JEDEC dimensions and notes apply.

CASE 59-03
DO-41
"SURMETIC"

7

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.) V_F = 1.5 V max, I_F = 200 mA for all types.

Type No. (Note 1)	Zener Voltage (Note 2)		Test Current I_{ZT}	Zener Impedance at I_{ZT} f = 1000 Hz		Blocking Voltage I_R = 1.0 μA	Typical T_C	Surge Current @ T_L = 25°C i_R – mA (Note 3)
	Min	Max	mA	Typ	Max		%/°C	
MZD3.9	3.7	4.1	100	3.8	7.0	–	-0.060	1380
MZD4.3	4.0	4.6	100	3.8	7.0	–	±0.055	1260
MZD4.7	4.4	5.0	100	3.8	7.0	–	±0.030	1190
MZD5.1	4.8	5.4	100	2.0	5.0	–	±0.030	1070
MZD5.6	5.2	6.0	100	1.0	2.0	1.5	+0.038	970
MZD6.2	5.8	6.6	100	1.0	2.0	1.5	+0.045	890
MZD6.8	6.4	7.2	100	1.0	2.0	2.0	+0.050	810
MZD7.5	7.0	7.9	100	1.0	2.0	2.0	+0.058	730
MZD8.2	7.7	8.7	100	1.0	2.0	3.5	+0.062	660
MZD9.1	8.5	9.6	50	2.0	4.0	3.5	+0.068	605
MZD10	9.4	10.6	50	2.0	4.0	5.0	+0.075	550
MZD11	10.4	11.6	50	4.0	7.0	5.0	+0.076	500
MZD12	11.4	12.7	50	4.0	7.0	7.0	+0.077	454
MZD13	12.4	14.1	50	5.0	10	7.0	+0.079	414
MZD15	13.8	15.8	50	5.0	10	10	+0.082	380
MZD16	15.3	17.1	25	6.0	15	10	+0.083	344
MZD18	16.8	19.1	25	6.0	15	10	+0.085	304
MZD20	18.8	21.2	25	6.0	15	10	+0.086	285
MZD22	20.8	23.3	25	6.0	15	12	+0.087	250
MZD24	22.8	25.6	25	7.0	15	12	+0.088	225
MZD27	25.1	28.9	25	7.0	15	14	+0.090	205
MZD30	28.0	32	25	8.0	15	14	+0.091	190
MZD33	31	35	25	8.0	15	17	+0.092	170
MZD36	34	38	10	21	40	17	+0.093	150
MZD39	37	41	10	21	40	20	+0.094	135
MZD43	40	46	10	24	45	20	+0.095	125
MZD47	44	50	10	24	45	24	+0.095	115
MZD51	48	54	10	25	60	24	+0.096	110
MZD56	52	60	10	25	60	28	+0.096	95
MZD62	58	66	10	25	80	28	+0.097	90
MZD68	64	72	10	25	80	34	+0.097	80
MZD75	70	79	10	30	100	34	+0.098	70
MZD82	77	88	10	30	100	41	+0.098	65
MZD91	85	96	5.0	60	200	41	+0.099	60
MZD100	94	106	5.0	60	200	50	+0.110	55
MZD110	104	116	5.0	80	250	50	+0.110	50
MZD120	114	127	5.0	80	250	60	+0.110	45
MZD130	124	141	5.0	110	300	60	+0.110	–
MZD150	138	156	5.0	110	300	75	+0.110	–
MZD160	153	171	5.0	150	350	75	+0.110	–
MZD180	168	191	5.0	150	350	90	+0.110	–
MZD200	188	212	5.0	150	350	90	+0.110	–

NOTE 1 – TOLERANCE AND TYPE NUMBER DESIGNATION

The type numbers listed have a standard tolerance on the nominal zener voltage of ±5%.

A suffix "C" indicates a ±2% tolerance; suffix "D" indicates a ±1% tolerance.

NOTE 2 – ZENER VOLTAGE (V_Z) MEASUREMENT

The zener voltage is measured after the test current (I_{ZT}) has been applied for 40 ± 10 milliseconds, while maintaining a lead temperature (T_L) of 30°C at a point of 10 mm from the diode body.

NOTE 3 – (I_R) NON-REPETITIVE SURGE CURRENT

Maximum peak, non-repetitive reverse surge current of half square wave or equivalent sine wave pulse of 50 ms duration, superimposed on the test current (I_{ZT}).

FIGURE 2 – TYPICAL THERMAL RESPONSE L, LEAD LENGTH = 10 mm

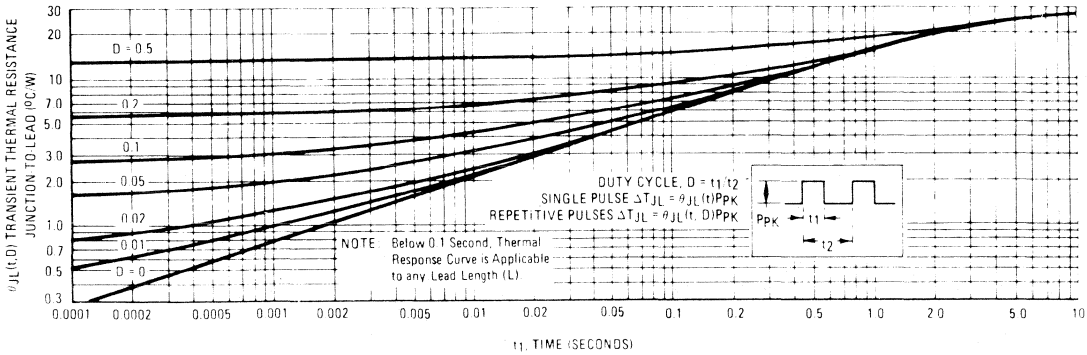


FIGURE 3 – TYPICAL THERMAL RESISTANCE

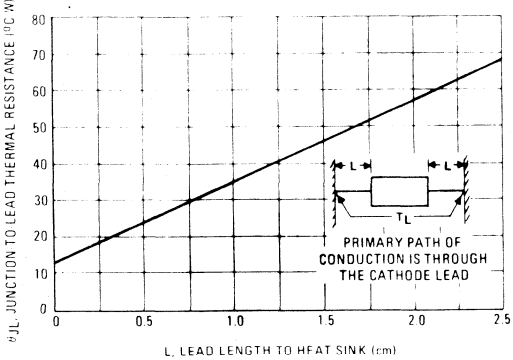


FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE POWER

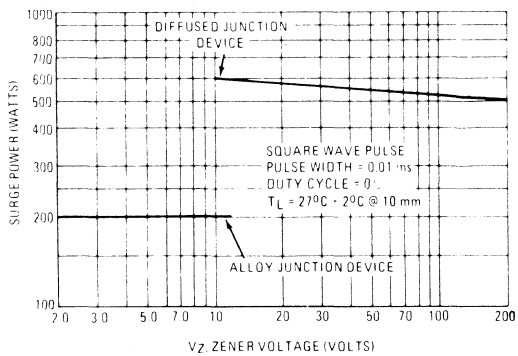
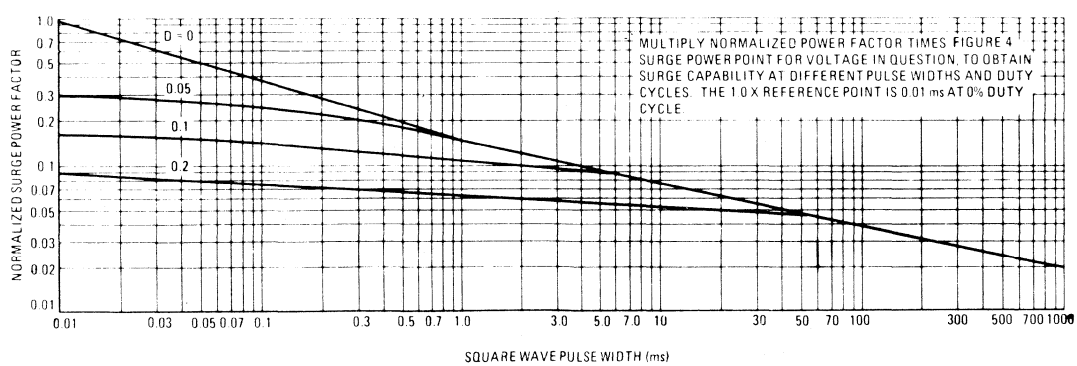


FIGURE 5 – SURGE POWER FACTOR



7

TEMPERATURE COEFFICIENTS AND VOLTAGE REGULATION

(90% OF THE UNITS ARE IN THE RANGES INDICATED)

FIGURE 6 – TEMPERATURE COEFFICIENT-RANGE FOR UNITS TO 12 VOLTS

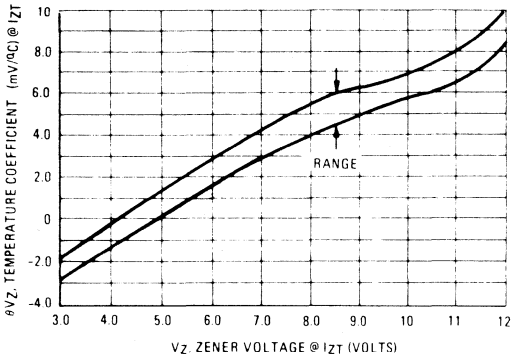


FIGURE 7 – TEMPERATURE COEFFICIENT-RANGE FOR UNITS 10 TO 200 VOLTS

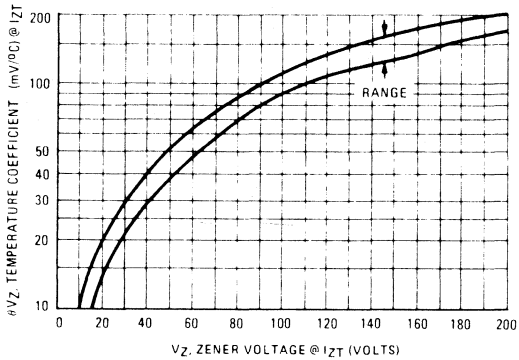
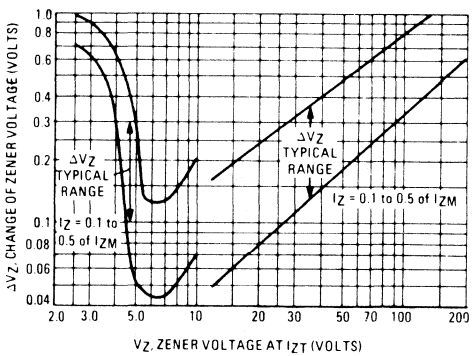


FIGURE 8 – VOLTAGE REGULATION



1 N4001, S thru 1 N4007, S

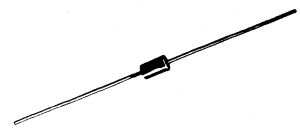
GENERAL-PURPOSE RECTIFIERS

. . . subminiature size, axial lead mounted rectifiers for general-purpose low-power applications.

1N4001S version has square dice

LEAD MOUNTED SILICON RECTIFIERS

50-1000 VOLTS
DIFFUSED JUNCTION



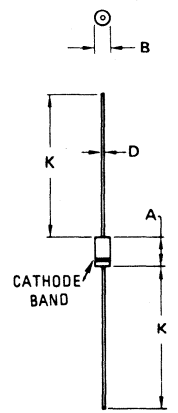
***MAXIMUM RATINGS**

Rating	Symbol	1N4001	1N4002	1N4003	1N4004	1N4005	1N4006	1N4007	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	400	600	800	1000	Volts
Non-Repetitive Peak Reverse Voltage (halfwave, single phase, 60 Hz)	V_{RSM}	60	120	240	480	720	1000	1200	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	35	70	140	280	420	560	700	Volts
Average Rectified Forward Current (single phase, resistive load, 60 Hz, see Figure 8, T_A = 75°C)	I_O	1.0							Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions, see Figure 2)	I_{FSM}	30 (for 1 cycle)							Amp
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +175							°C

***ELECTRICAL CHARACTERISTICS**

Characteristic and Conditions	Symbol	Typ	Max	Unit
Maximum Instantaneous Forward Voltage Drop (i_F = 1.0 Amp, T_J = 25°C) Figure 1	v_F	0.93	1.1	Volts
Maximum Full-Cycle Average Forward Voltage Drop (I_O = 1.0 Amp, T_L = 75°C, 1 inch leads)	$V_{F(AV)}$	–	0.8	Volts
Maximum Reverse Current (rated dc voltage) T_J = 25°C T_J = 100°C	I_R	 0.05 1.0	 10 50	μA
Maximum Full-Cycle Average Reverse Current (I_O = 1.0 Amp, T_L = 75°C, 1 inch leads	$I_{R(AV)}$	–	30	μA

*Indicates JEDEC Registered Data.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.70	5.20	0.185	0.205
B	2.79	3.05	0.110	0.120
D				0.034
K	25.4		1.000	

DOES NOT CONFORM TO JEDEC DO-41 OUTLINE 1N4001S SERIES

Case 59 - 4

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94	–	1.100	–

1N4001 SERIES

MECHANICAL CHARACTERISTICS

CASE: Void free, Transfer Molded
MAXIMUM LEAD TEMPERATURE FOR SOLDERING PURPOSES: 350°C, 3/8" from case for 10 seconds at 5 lbs. tension
FINISH: All external surfaces are corrosion-resistant, leads are readily solderable
POLARITY: Cathode indicated by color band
WEIGHT: 0.40 Grams (approximately)

7

1N4933 thru 1N4937

Designers Data Sheet

AXIAL-LEAD, FAST-RECOVERY RECTIFIERS

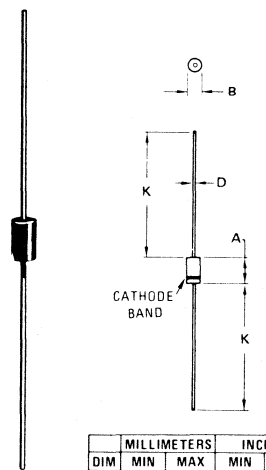
. . . designed for special applications such as dc power supplies, inverters, converters, ultrasonic systems, choppers, low RF interference and free wheeling diodes. A complete line of fast recovery rectifiers having typical recovery time of 150 nanoseconds providing high efficiency at frequencies to 250 kHz.

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing device characteristics boundaries — are given to facilitate "worst case" design.

FAST RECOVERY RECTIFIERS

50–600 VOLTS
1 AMPERE



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94	–	1.100	–

CASE 59-04
(Does not meet DO-41 outline)

***MAXIMUM RATINGS**

Rating	Symbol	1N4933	1N4934	1N4935	1N4936	1N4937	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	400	600	Volts
Nonrepetitive Peak Reverse Voltage RMS Reverse Voltage	V_{RSM} $V_{R(RMS)}$	75 35	150 70	250 140	450 280	650 420	Volts Volts
Average Rectified Forward Current (Single phase, resistive load, T_A = 75°C)	I_O	◄——— 1.0 ———►					Amp
Nonrepetitive Peak Surge Current (Surge applied at rated load conditions)	I_{FSM}	◄——— 30 ———►					Amps
Operating Junction Temperature Range Storage Temperature Range	T_J T_{stg}	◄——— -65 to +150 ———► ◄——— -65 to +175 ———►					°C °C

***THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient (Typical Printed Circuit-Board Mounting)	$R_{\theta JC}$	65	°C/W

***ELECTRICAL CHARACTERISTICS**

Characteristic	Symbol	Min	Typ	Max	Unit
*Instantaneous Forward Voltage (i_F = 3.14 Amp, T_J = 150°C)	v_F	–	1.0	1.2	Volts
Forward Voltage (I_F = 1.0 Amp, T_A = 25°C)	V_F	–	1.0	1.1	Volts
*Reverse Current (Rated dc Voltage) T_A = 25°C T_A = 100°C	I_R	– –	1.0 50	5.0 100	μA

***REVERSE RECOVERY CHARACTERISTICS**

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Recovery Time (I_F = 1.0 Amp to V_R = 30 Vdc) (Figure 21) (I_{FM} = 15 Amp, di/dt = 10A/μs (Figure 22)	t_{rr}	– –	150 175	200 300	ns
Reverse Recovery Current (I_F = 1.0 Amp to V_R = 30 Vdc) (Figure 21)	$I_{RM(REC)}$	–	1.0	2.0	Amp

*Indicates JEDEC Registered Data

MECHANICAL CHARACTERISTICS

CASE: Void free, transfer molded
FINISH: External leads are readily solderable
POLARITY: Cathode indicated by polarity band
WEIGHT: 0.4 Gram (approximately)

FIGURE 1 – FORWARD VOLTAGE

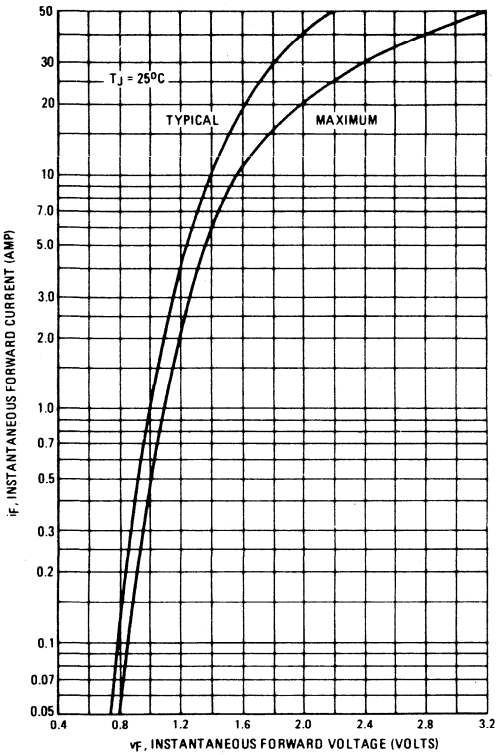


FIGURE 2 – MAXIMUM SURGE CAPABILITY

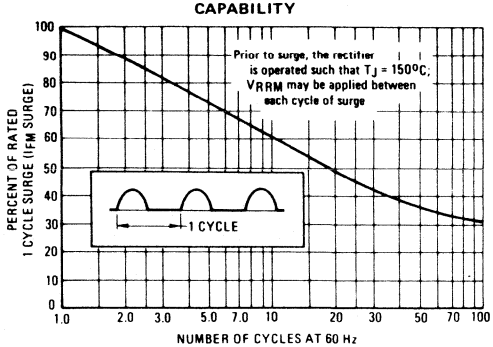
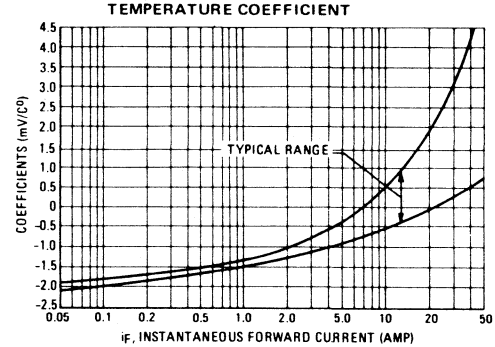
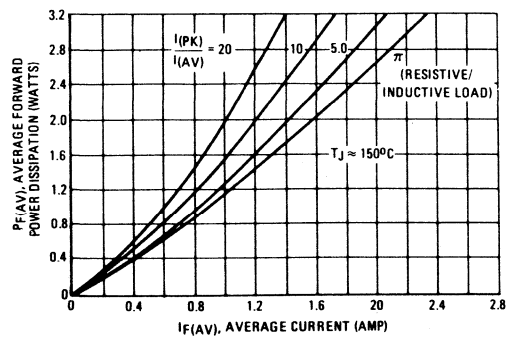


FIGURE 3 – FORWARD VOLTAGE TEMPERATURE COEFFICIENT



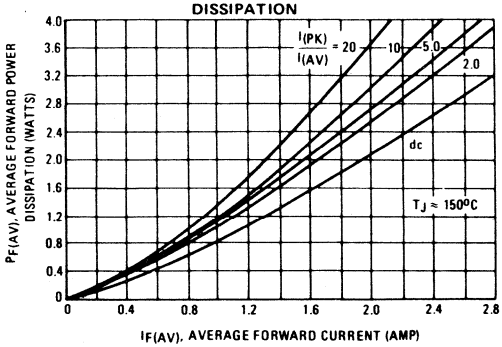
SINE WAVE INPUT

FIGURE 4 – FORWARD POWER DISSIPATION



SQUARE WAVE INPUT

FIGURE 5 – FORWARD POWER DISSIPATION



7

MAXIMUM CURRENT RATINGS

SINE WAVE INPUT

FIGURE 6 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

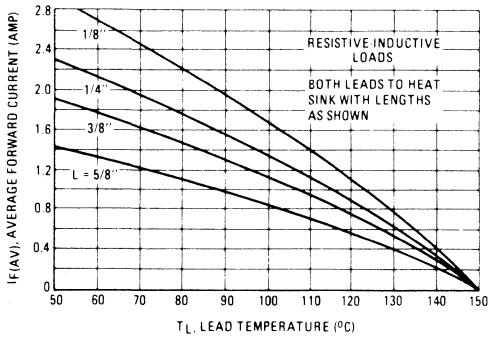


FIGURE 8 – 1/8" LEAD LENGTH, VARIOUS LOADS

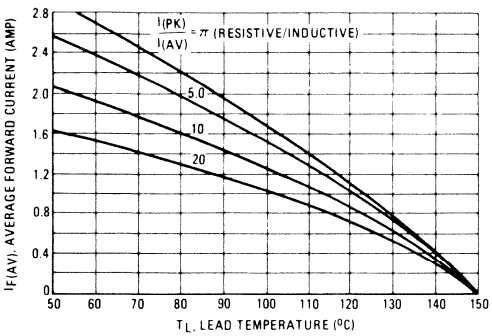
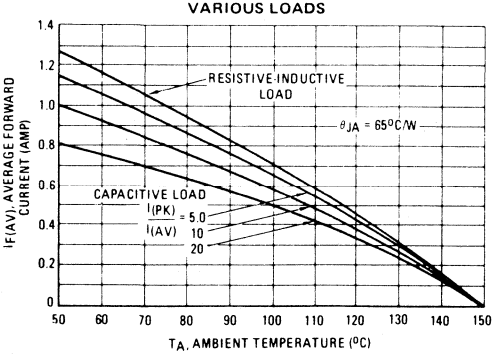


FIGURE 10 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS



SQUARE WAVE INPUT

FIGURE 7 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

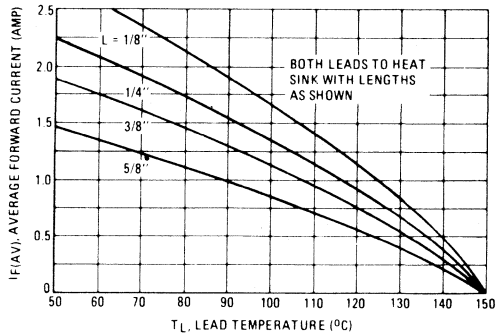


FIGURE 9 – 1/8" LEAD LENGTHS, VARIOUS LOADS

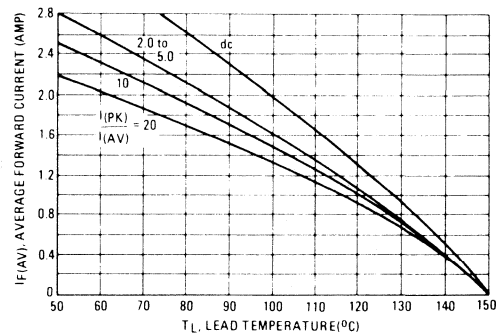


FIGURE 11 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS

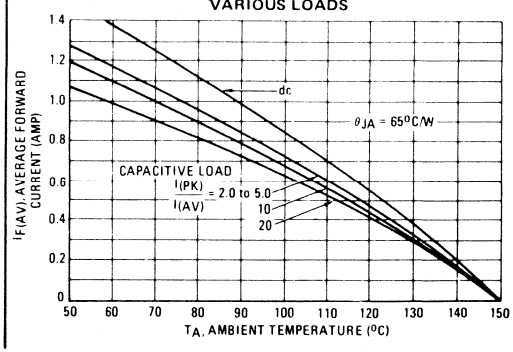


FIGURE 12 – THERMAL RESPONSE

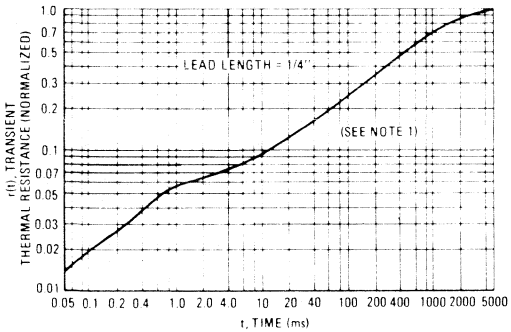
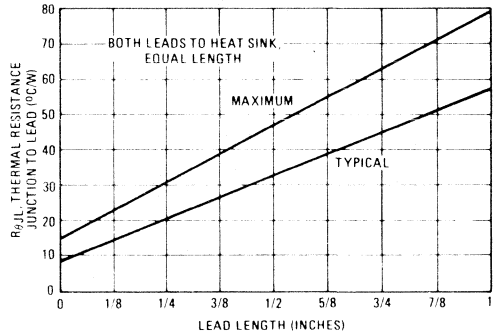
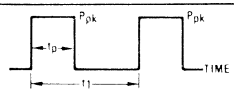


FIGURE 13 – THERMAL RESISTANCE



NOTE 1



DUTY CYCLE, $D = t_p/t_1$
PEAK POWER, P_{pk}, is peak of an equivalent square power pulse.

To determine maximum junction temperature of the diode in a given situation, the following procedure is recommended:

The temperature of the case should be measured using a thermocouple placed on the case at the temperature reference point (see Note 3). The thermal mass connected to the case is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady state conditions are achieved. Using the measured value of T_C, the junction temperature may be determined by:

$$T_J = T_C + \Delta T_{JC}$$

where ΔT_{JC} is the increase in junction temperature above the case temperature. It may be determined by:

$$\Delta T_{JC} = P_{pk} \cdot R_{\theta JC} [D + (1 - D) \cdot r(t_1 + t_p) + r(t_p) - r(t_1)]$$

where:

$r(t)$ = normalized value of transient thermal resistance at time, t, from Figure 3, i.e.:

$r(t_1 + t_p)$ = normalized value of transient thermal resistance at time $t_1 + t_p$.

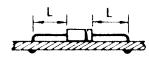
NOTE 2

Data shown for thermal resistance junction-to-ambient (θ_{JA}) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

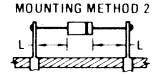
TYPICAL VALUES FOR θ_{JA} IN STILL AIR

MOUNTING METHOD	LEAD LENGTH, L (IN)				
	1/8	1/4	1/2	3/4	$R_{\theta JA}$
1	65	72	82	92	°C/W
2	74	81	91	101	°C/W
3	40				°C/W

MOUNTING METHOD 1



MOUNTING METHOD 2



Vector pin mounting

MOUNTING METHOD 3

P. C. Board with 1-1/2" x 1-1/2" copper surface

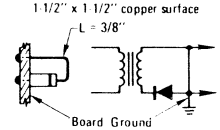
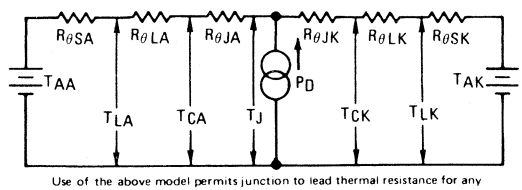


FIGURE 14 – THERMAL CIRCUIT MODEL
(For Heat Conduction Through The Leads)



Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heat sink. Terms in the model signify:

T_A = Ambient Temperature
T_L = Lead Temperature
T_C = Case Temperature
T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_D = Power Dissipation

(Subscripts A and K refer to anode and cathode sides respectively.)

Values for thermal resistance components are:

$R_{\theta L}$ = 112°C/W/IN. Typically and 128°C/W/IN Maximum

$R_{\theta J}$ = 18°C/W Typically and 30°C/W Maximum

The maximum lead temperature may be calculated as follows:

$$T_L = 150^{\circ} - \Delta T_{JL}$$

ΔT_{JL} can be calculated as shown in NOTE 1 or it may be approximated as follows:

$\Delta T_{JL} \approx R_{\theta JL} \bullet P_F$; P_F may be formulated for sine-wave operation from Figure 3 or from Figure 4 for square-wave operation.

7

TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 15 – FORWARD RECOVERY TIME

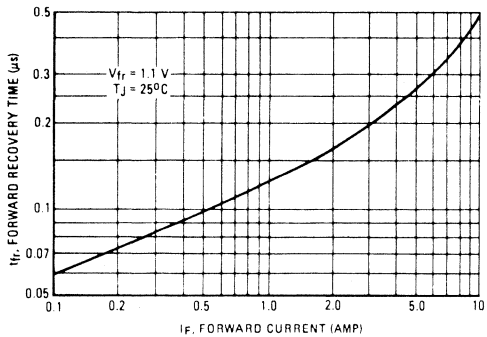
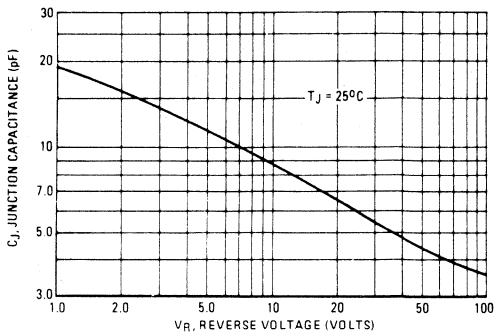


FIGURE 16 – JUNCTION CAPACITANCE



TYPICAL RECOVERED STORED CHARGED DATA

FIGURE 17 – T_J = 25°C

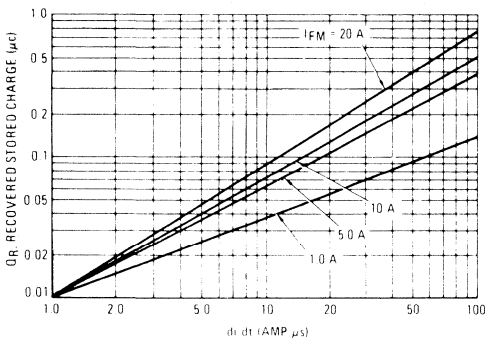


FIGURE 18 – T_J = 75°C

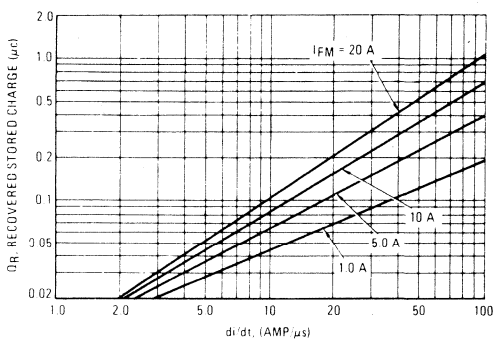


FIGURE 19 – T_J = 100°C

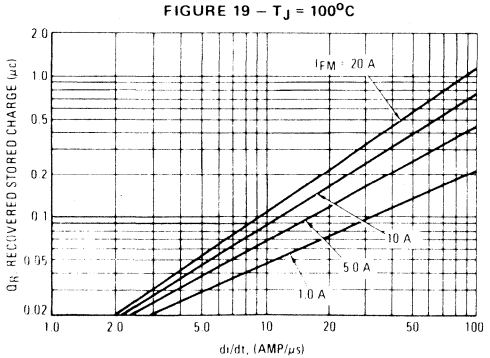
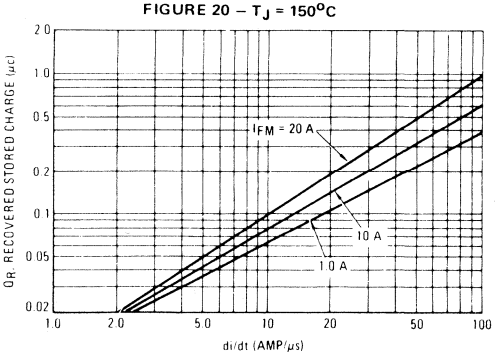


FIGURE 20 – T_J = 150°C



RECOVERY TIME

FIGURE 21 – REVERSE RECOVERY CIRCUIT

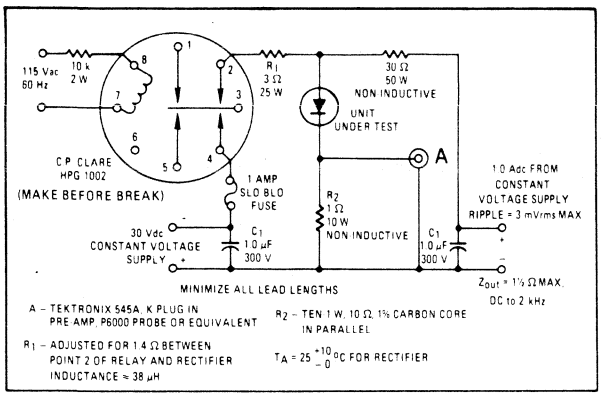
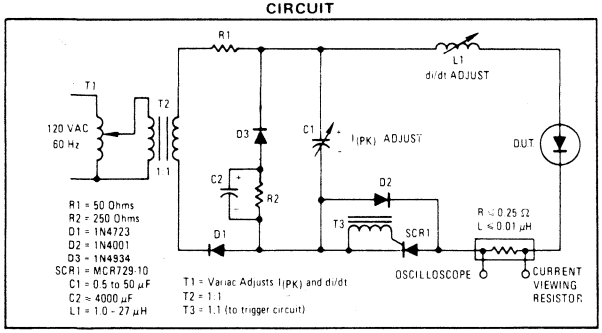


FIGURE 22 – JEDEC REVERSE RECOVERY CIRCUIT



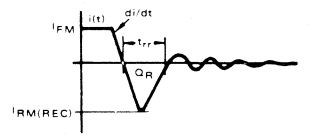
NOTE 3

Reverse recovery time is the period which elapses from the time that the current, thru a previously forward biased rectifier diode, passes thru zero going negatively until the reverse current recovers to a point which is less than 10% peak reverse current.

Reverse recovery time is a direct function of the forward current prior to the application of reverse voltage.

For any given rectifier, recovery time is very circuit dependent. Typical and maximum recovery time of all Motorola fast recovery power rectifiers are rated under a fixed set of conditions using I_F = 1.0 A, V_R = 30 V. In order to cover all circuit conditions, curves are given for typical recovered stored charge versus commutation di/dt for various levels of forward current and for junction temperatures of 25°C, 75°C, 100°C, and 150°C.

To use these curves, it is necessary to know the forward current level just before commutation, the circuit commutation di/dt, and the operating junction temperature. The reverse recovery test current waveform for all Motorola fast recovery rectifiers is shown.



From stored charge curves versus di/dt, recovery time (t_{rr}) and peak reverse recovery current ($I_{RM(REC)}$) can be closely approximated using the following formulas:

$$t_{rr} = 1.41 \times \left[\frac{Q_R}{di/dt}\right]^{1/2}$$

$$I_{RM(REC)} = 1.41 \times \left[Q_R \times di/dt\right]^{1/2}$$

FIGURE 23 – TYPICAL REVERSE LEAKAGE

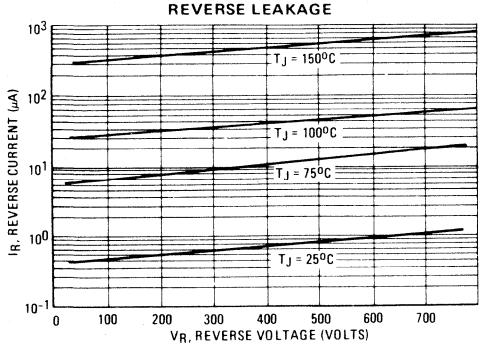
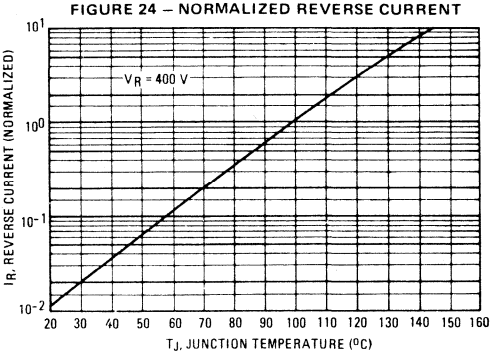


FIGURE 24 – NORMALIZED REVERSE CURRENT



7

1N5333 • 1N5388

5.0 WATT SURMETIC 40 SILICON ZENER DIODES (SILICON OXIDE PASSIVATED)

. . . a complete new series of 5.0 Watt Zener Diodes with tight limits and better operating characteristics that reflect the superior capabilities of silicon-oxide-passivated junctions. All this in an axial-lead, transfer-molded plastic package offering protection in all common environmental conditions.

- Up to 180 Watt Surge Rating @ 8.3 ms
- Maximum Limits Guaranteed on Seven Electrical Parameters

(5M3.3ZS10 thru 5M200ZS10 / 1N5333A thru 1N5388A)
(5M3.3ZS5 thru 5M200ZS5 / 1N5333B thru 1N5388B)

5.0 WATT
ZENER REGULATOR DIODES

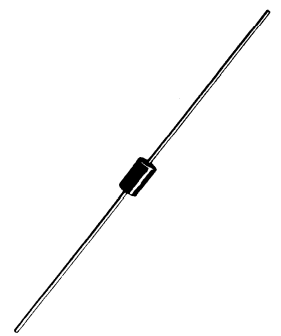
3.3 – 200 VOLTS

MAXIMUM RATINGS

Junction and Storage Temperature: -65 to +200°C

Lead Temperature not less than 1/16" from the case for 10 seconds: 230°C

DC Power Dissipation: 5.0 W @ T_L = 75°C, Lead Length = 3/8"
(Derate 40 mW/°C above 75°C)



MECHANICAL CHARACTERISTICS

CASE: Void-free, transfer-molded, thermosetting plastic

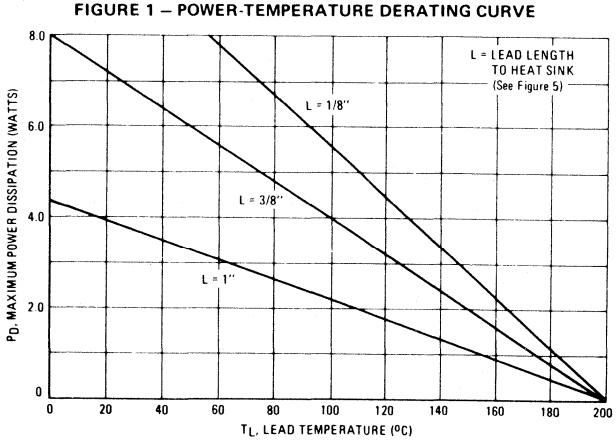
FINISH: All external surfaces are corrosion resistant. Leads are readily solderable

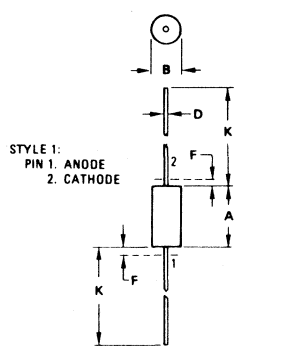
POLARITY: Cathode indicated by color band. When operated in zener mode, cathode will be positive with respect to anode.

MOUNTING POSITION: Any

WEIGHT: 0.7 gram (approx)

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.38	8.89	0.330	0.350
B	3.30	3.68	0.130	0.145
D	0.94	1.09	0.037	0.043
F	–	1.27	–	0.050
K	25.40	31.75	1.000	1.250

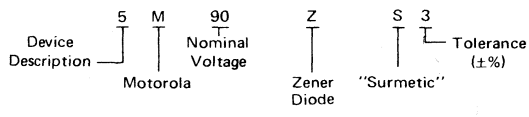
CASE 17

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) V_F = 1.2 Max @ I_F = 1.0 A for all types

JEDEC Type No. (Note 1 & 2)	Nominal Zener Voltage V_Z @ I_{ZT} Volts (Note 3)	Test Current I_{ZT} mA	Max Zener Impedance A & B Suffix Only		Max Reverse Leakage Current			Applies to all Suffix	A & B Suffix Only	Maximum Regulator Current I_{ZM} mA
			Z_{ZT} @ I_{ZT} Ohms (Note 3)	Z_{ZK} @ I_{ZK} = 1.0 mA Ohms (Note 3)	I_R μA	@ V_R Volts		Max Surge Current i_r, Amps	Max Voltage Regulation $\triangle V_Z$, Volts	
						Non & A Suffix	B Suffix	(Note 4)	(Note 5)	(Note 6)
1N5333	3.3	380	3.0	400	300	1.0	1.0	20.0	0.85	1440
1N5334	3.6	350	2.5	500	150	1.0	1.0	18.7	0.80	1320
1N5335	3.9	320	2.0	500	50	1.0	1.0	17.6	0.54	1220
1N5336	4.3	290	2.0	500	10	1.0	1.0	16.4	0.49	1100
1N5337	4.7	260	2.0	450	5.0	1.0	1.0	15.3	0.44	1010
1N5338	5.1	240	1.5	400	1.0	1.0	1.0	14.4	0.39	930
1N5339	5.6	220	1.0	400	1.0	2.0	2.0	13.4	0.25	865
1N5340	6.0	200	1.0	300	1.0	3.0	3.0	12.7	0.19	790
1N5341	6.2	200	1.0	200	1.0	3.0	3.0	12.4	0.10	765
1N5342	6.8	175	1.0	200	10	4.9	5.2	11.5	0.15	700
1N5343	7.5	175	1.5	200	10	5.4	5.7	10.7	0.15	630
1N5344	8.2	150	1.5	200	10	5.9	6.2	10.0	0.20	580
1N5345	8.7	150	2.0	200	10	6.3	6.6	9.5	0.20	545
1N5346	9.1	150	2.0	150	7.5	6.6	6.9	9.2	0.22	520
1N5347	10	125	2.0	125	5.0	7.2	7.6	8.6	0.22	475
1N5348	11	125	2.5	125	5.0	8.0	8.4	8.0	0.25	430
1N5349	12	100	2.5	125	2.0	8.6	9.1	7.5	0.25	395
1N5350	13	100	2.5	100	1.0	9.4	9.9	7.0	0.25	365
1N5351	14	100	2.5	75	1.0	10.1	10.6	6.7	0.25	340
1N5352	15	75	2.5	75	1.0	10.8	11.5	6.3	0.25	315
1N5353	16	75	2.5	75	1.0	11.5	12.2	6.0	0.30	295
1N5354	17	70	2.5	75	0.5	12.2	12.9	5.8	0.35	280
1N5355	18	65	2.5	75	0.5	13.0	13.7	5.5	0.40	264
1N5356	19	65	3.0	75	0.5	13.7	14.4	5.3	0.40	250
1N5357	20	65	3.0	75	0.5	14.4	15.2	5.1	0.40	237
1N5358	22	50	3.5	75	0.5	15.8	16.7	4.7	0.45	216
1N5359	24	50	3.5	100	0.5	17.3	18.2	4.4	0.55	198
1N5360	25	50	4.0	110	0.5	18.0	19.0	4.3	0.55	190
1N5361	27	50	5.0	120	0.5	19.4	20.6	4.1	0.60	176
1N5362	28	50	6.0	130	0.5	20.1	21.2	3.9	0.60	170
1N5363	30	40	8.0	140	0.5	21.6	22.8	3.7	0.60	158
1N5364	33	40	10	150	0.5	23.8	25.1	3.5	0.60	144
1N5365	36	30	11	160	0.5	25.9	27.4	3.3	0.65	132
1N5366	39	30	14	170	0.5	28.1	29.7	3.1	0.65	122
1N5367	43	30	20	190	0.5	31.0	32.7	2.8	0.70	110
1N5368	47	25	25	210	0.5	33.8	35.8	2.7	0.80	100
1N5369	51	25	27	230	0.5	36.7	38.8	2.5	0.90	93.0
1N5370	56	20	35	280	0.5	40.3	42.6	2.3	1.00	86.0
1N5371	60	20	40	350	0.5	43.0	45.5	2.2	1.20	79.0
1N5372	62	20	42	400	0.5	44.6	47.1	2.1	1.35	76.0
1N5373	68	20	44	500	0.5	49.0	51.7	2.0	1.50	70.0
1N5374	75	20	45	620	0.5	54.0	56.0	1.9	1.60	63.0
1N5375	82	15	65	720	0.5	59.0	62.2	1.8	1.80	58.0
1N5376	87	15	75	760	0.5	63.0	66.0	1.7	2.00	54.5
1N5377	91	15	75	760	0.5	65.5	69.2	1.6	2.20	52.5
1N5378	100	12	90	800	0.5	72.0	76.0	1.5	2.50	47.5
1N5379	110	12	125	1000	0.5	79.2	83.6	1.4	2.50	43.0
1N5380	120	10	170	1150	0.5	86.4	91.2	1.3	2.50	39.5
1N5381	130	10	190	1250	0.5	93.6	98.8	1.2	2.50	36.6
1N5382	140	8.0	230	1500	0.5	101	106	1.2	2.50	34.0
1N5383	150	8.0	330	1500	0.5	108	114	1.1	3.00	31.6
1N5384	160	8.0	350	1650	0.5	115	122	1.1	3.00	29.4
1N5385	170	8.0	380	1750	0.5	122	129	1.0	3.00	28.0
1N5386	180	5.0	430	1750	0.5	130	137	1.0	4.00	26.4
1N5387	190	5.0	450	1850	0.5	137	144	0.9	5.00	25.0
1N5388	200	5.0	480	1850	0.5	144	152	0.9	5.00	23.6

NOTE 1 – TOLERANCE AND VOLTAGE DESIGNATION

TOLERANCE DESIGNATION – The JEDEC type numbers shown indicate a tolerance of ±20% with guaranteed limits on only V_Z, I_R, i_r, and V_F as shown in the electrical characteristics table. Units with guaranteed limits on all seven parameters are indicated by suffix "A" for ±10% tolerance and suffix "B" for ±5.0% units.



Example: **5M90ZS3**

NOTE 2 – SPECIALS AVAILABLE INCLUDE:

(A) NOMINAL ZENER VOLTAGES BETWEEN THE VOLTAGES SHOWN AND TIGHTER VOLTAGE TOLERANCES: To designate units with zener voltages other than those assigned JEDEC numbers and/or tight voltage tolerances (±3%, ±2%, ±1%), the Motorola type number should be used.

(B) MATCHED SETS: (Standard Tolerances are ±5.0%, ±2.0%, ±1.0%).

Zener diodes can be obtained in sets consisting of two or more matched devices. The method for specifying such matched sets is similar to the one described in (A) for specifying units

7

with a special voltage and/or tolerance except that two extra suffixes are added to the code number described.

These units are marked with code letters to identify the matched sets and, in addition, each unit in a set is marked with the same serial number, which is different for each set being ordered.

5	M	5 1	Z	S	5	B	1
Device Description	Motorola	51 Volts (each device)	Zener Diodes	"Surmetic"	Tolerance per device (±5%) (omit for ±20% units)	Code* (A-Not used)	Overall Tolerance of set (±1%)

*Code:
B – Two devices in series
C – Three devices in series
D – Four devices in series

Example: **5M51ZS5B1**

(C) ZENER CLIPPERS: (Standard Tolerance ±10% and ±5%).

Special clipper diodes with opposing Zener junctions built into the device are available by using the following nomenclature:

5	M	20,	Z	Z	10
Device Description	Motorola	Nominal Voltage	Zener Diodes	Clipper	Tolerance for each of the two Zener voltages (not a matching requirement)

Example: **5M20ZZ10**

NOTE 3 – ZENER VOLTAGE (V_Z) AND IMPEDANCE (Z_{ZT} & Z_{ZK})

Test conditions for Zener voltage and impedance are as follows: I_Z is applied 40 ± 10 ms prior to reading. Mounting contacts are located 3/8" to 1/2" from the inside edge of mounting clips to the body of the diode. ($T_A = 25^oC \, ^{+8}_{-2}{}^oC$).

NOTE 4 – SURGE CURRENT (i_r)

Surge current is specified as the maximum allowable peak, non-recurrent square-wave current with a pulse width, PW, of 8.3 ms. The data given in Figure 6 may be used to find the maximum surge current for a square wave of any pulse width between 1.0 ms and 1000 ms by plotting the applicable points on logarithmic paper. Examples of this, using the 3.3 V and 200 V zeners, are shown in Figure 7. Mounting contact located as specified in Note 3. ($T_A = 25^oC \, ^{+8}_{-2}{}^oC$).

NOTE 5 – VOLTAGE REGULATION ($\triangle V_Z$)

Test conditions for voltage regulation are as follows: V_Z measurements are made at 10% and then at 50% of the I_Z max value listed in the electrical characteristics table. The test currents are the same for the 5% and 10% tolerance devices. The test current time duration for each V_Z measurement is 40 ± 10 ms. ($T_A = 25^oC \, ^{+8}_{-2}{}^oC$). Mounting contact located as specified in Note 3.

NOTE 6 – MAXIMUM REGULATOR CURRENT (I_{ZM})

The maximum current shown is based on the maximum voltage of a 5% type unit, therefore, it applies only to the B-suffix device. The actual I_{ZM} for any device may not exceed the value of 5.0 watts divided by the actual V_Z of the device. $T_L = 75^oC$ at 3/8" maximum from the device body.

TEMPERATURE COEFFICIENTS

FIGURE 2 – TEMPERATURE COEFFICIENT-RANGE FOR UNITS 3.0 TO 10 VOLTS

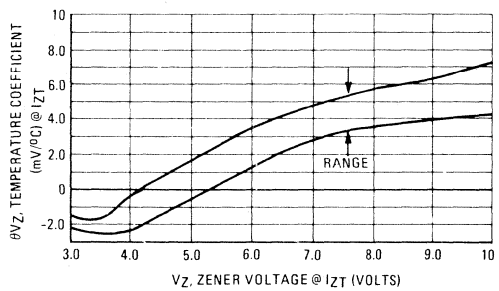


FIGURE 3 – TEMPERATURE COEFFICIENT-RANGE FOR UNITS 10 TO 220 VOLTS

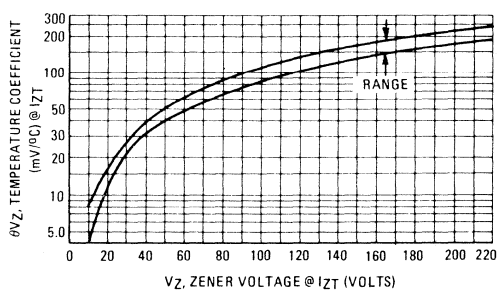


FIGURE 4 – TYPICAL THERMAL RESPONSE

L, LEAD LENGTH = 3/8 INCH

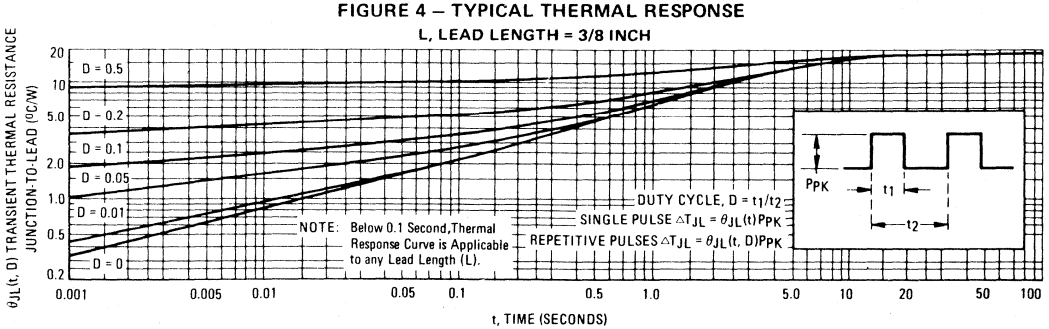


FIGURE 5 – TYPICAL THERMAL RESISTANCE

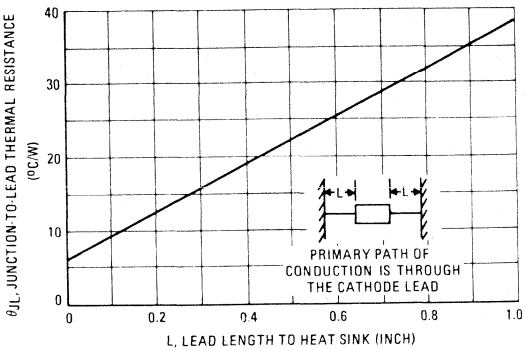


FIGURE 6 – MAXIMUM NON-REPETITIVE SURGE CURRENT versus NOMINAL ZENER VOLTAGE

(See Note 4)

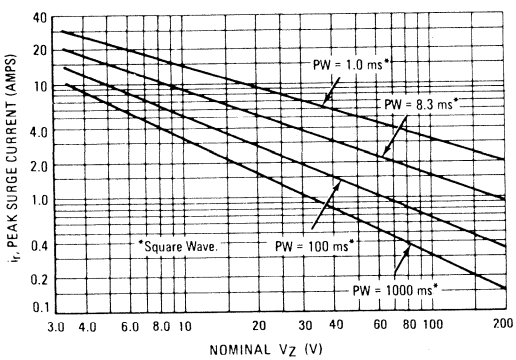
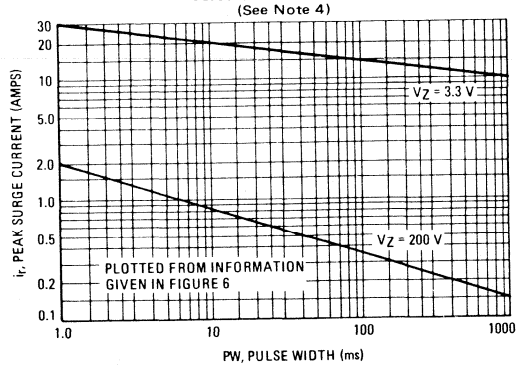


FIGURE 7 – PEAK SURGE CURRENT versus PULSE WIDTH

(See Note 4)



APPLICATION NOTE

Since the actual voltage available from a given zener diode is temperature dependent, it is necessary to determine junction temperature under any set of operating conditions, in order to calculate its value. The following procedure is recommended:

Lead Temperature, T_L, should be determined from:

$$T_L = \theta_{LA} P_D + T_A$$

θ_{LA} is the lead-to-ambient thermal resistance and P_D is the power dissipation. θ_{LA} is generally 30-40°C/W for the various clips and tie points in common use and for printed circuit board wiring.

Junction Temperature, T_J, may be found from:

$$T_J = T_L + \Delta T_{JL}$$

ΔT_{JL} is the increase in junction temperature above the lead temperature and may be found from Figure 4 for a train of power pulses or from Figure 5 for dc power.

$$\Delta T_{JL} = \theta_{JL} P_D$$

For worst-case design, using expected limits of I_Z, limits of P_D and the extremes of $T_J(\Delta T_J)$ may be estimated. Changes in voltage, V_Z, can then be found from:

$$\Delta V = \theta_{VZ} \Delta T_J$$

θ_{VZ}, the zener voltage temperature coefficient, is found from Figures 2 and 3.

Under high power-pulse operation, the zener voltage will vary with time and may also be affected significantly by the zener resistance. For best regulation, keep current excursions as low as possible.

Data of Figure 4 should not be used to compute surge capability. Surge limitations are given in Figure 6. They are lower than would be expected by considering only junction temperature, as current crowding effects cause temperatures to be extremely high in small spots resulting in device degradation should the limits of Figure 6 be exceeded.

1N5400 thru 1N5408

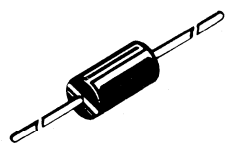
LEAD MOUNTED STANDARD RECOVERY RECTIFIERS

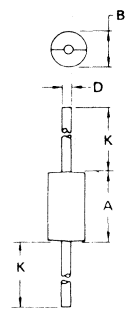
. . . designed for use in power supplies and other applications having need of a device with the following features:

- High Current to Small Size
- High Surge Current Capability
- Low Forward Voltage Drop
- Void-Free Economical Plastic Package
- Available in Volume Quantities

STANDARD RECOVERY RECTIFIERS

50–1000 VOLTS
3 AMPERES





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.65	0.370	0.380
B	4.83	5.33	0.190	0.210
D	1.22	1.32	0.048	0.052
K	26.97	27.23	1.062	1.072

CASE 267-01

MAXIMUM RATINGS

Rating	Symbol	1N5400	1N5401	1N5402	1N5404	1N5406	1N5407	1N5408	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	400	600	800	1000	Volts
Nonrepetitive Peak Reverse Voltage	V_{RSM}	100	200	300	525	800	1000	1200	Volts
Average Rectified Foward Current (Single Phase Resistive Load, (1/2" Leads, T_L = 105°C)	I_O	3.0							Amp
Nonrepetitive Peak Surge Current (Surge Applied at Rated Load Conditions)	I_{FSM}	200 (one cycle)							Amp
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +175							°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Unit
Thermal Resistance, Junction to Ambient (PC Board Mount, 1/2" Leads)	$R_{\theta JA}$	53	°C/W

*ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Instantaneous Forward Voltage (1) (i_F = 9.4 Amp)	v_F	–	–	1.2	Volts
Average Reverse Current (1) DC Reverse Current (Rated dc Voltage, T_L = 150°C)	$I_{R(AV)}$ I_R	– –	– –	500 500	μA

*JEDEC Registered Data.

(1) Measured in a single-phase half-wave circuit such as shown in Figure 6.25 of EIA RS-282, November 1963. Operated at rated load conditions T_L=105°C, I_O=3.0 A, V_r=V_{RWM}.

MECHANICAL CHARACTERISTICS

Case: Void Free, Transfer Molded
Finish: External Leads are Plated, Leads are readily Solderable
Polarity: Indicated by Cathode Band
Weight: 1.1 Grams (Approximately)
Maximum Lead Temperature for Soldering Purposes:
240°C, 1/8" from case for 10 s at 5.0 lb. tension

FIGURE 1 – FORWARD VOLTAGE

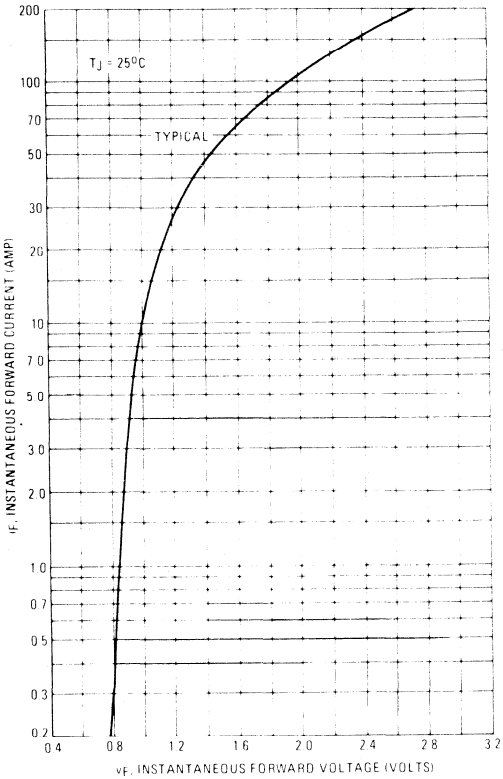


FIGURE 2 – MAXIMUM NONREPETITIVE SURGE CURRENT

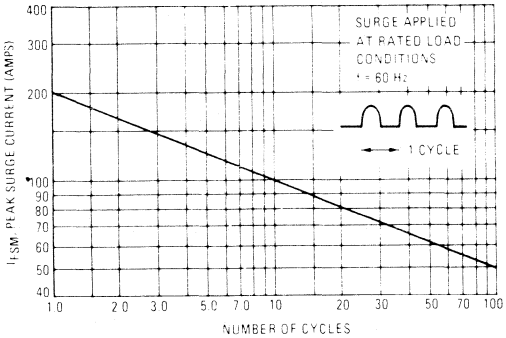
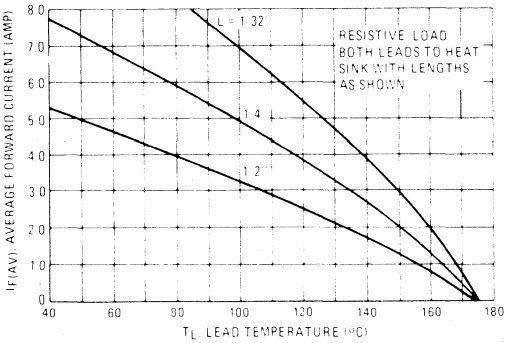


FIGURE 3 – CURRENT DERATING VARIOUS LEAD LENGTHS



NOTE 1 – AMBIENT MOUNTING DATA

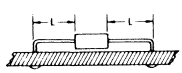
Data shown for thermal resistance junction to ambient ($R_{\theta JA}$) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

TYPICAL VALUES FOR $R_{\theta JA}$ IN STILL AIR

MOUNTING METHOD	LEAD LENGTH, L (IN)				$R_{\theta JA}$
	1/8	1/4	1/2	3/4	
1	50	51	53	55	°C/W
2	58	59	61	63	°C/W
3	28				°C/W

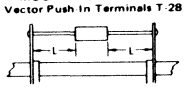
MOUNTING METHOD 1

P.C. Board Where Available Copper Surface area is small.



MOUNTING METHOD 2

Vector Push In Terminals T-28



MOUNTING METHOD 3

P.C. Board with 1-1/2" x 1-1/2" Copper Surface

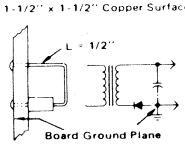
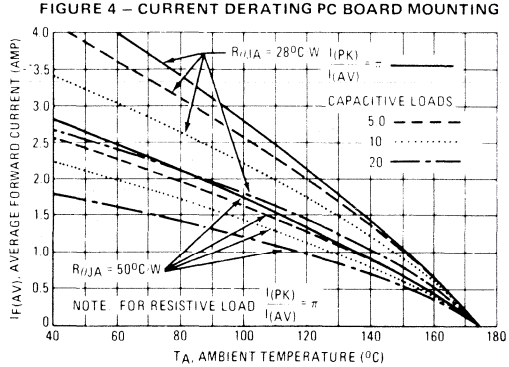


FIGURE 4 – CURRENT DERATING PC BOARD MOUNTING

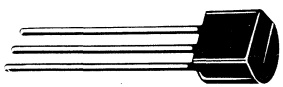


7

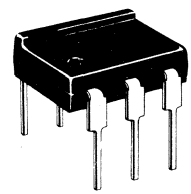
SECTION 8 — OPTO DEVICES

- **Opto couplers**
- **IR emitting diodes**
- **Photodarlingtons**
- **Phototransistors**

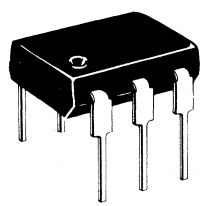
Section 8—Packages



Case 29.02
TO 92



Case 673.03
Case 673.04



730
730.01

8 OPTO DEVICES

Opto Couplers

Device	V_{iso} Min. V	V_R Max. V	BV_{CEO} Min. V	I_C @ I_F = 10 mA Min. mA	I_C @ I_F = 10 mA Typ. mA	Package	Page
4N25, 4N25A	2500	3	30	2	3.5	673-04	8-22
4N26	1500	3	30	2	3.5	673-04	8-22
4N27	1500	3	30	1	2.0	673-04	8-22
4N28	500	3	30	1	2.0	673-04	8-22
4N29	2500	3	30	10	—	673-03	8-26
4N31	1500	3	30	5	—	673-03	8-26
4N32	2500	3	30	50	—	673-03	8-26
4N33	1500	3	30	50	—	673-03	8-26
4N38	1500	3	80	—	3.5	673-04	8-30
4N38A	2500	3	80	—	3.5	673-04	8-30

Opto couplers with Triac Driver Output

Device	V_{ISO} Min. V	V_R Max. V	V_{DRM} Max. V	I_{FT} Max. mA	Package	Page
MOC3010	7500	3	250	15	730	8-9
MOC3011	7500	3	250	10	730	8-9
MOC3020S	7500	3	400	20	730	8-13
MOC3021S	7500	3	400	15	730	8-13
MOC3030	7500	3	250	30	730.01	8-17
MOC3031	7500	3	250	15	730.01	8-17

Infrared Emitting Diodes

Device	Emission Angle ∝	Instantaneous Power Output Typ			Package	Page
MLED92	110°	650 µW	@	100 mA	T092	8-5
MLED93	110°	3.0 mW	@	100 mA	29-02	8-7
MLED94	110°	5.0 mW	@	100 mA	29-02	8-7
MLED95	110°	8.0 mW	@	100 mA	29-02	8-7

Photodarlingtons

Device	Light Current Typ uA @ mW/cm² H		BV_{CEO} Min. V	Dark Current Max. nA @ V_{CE} V		Package	Page
2N5777	4.0	2.0	25	100	12	T092	8-20
2N5778	4.0	2.0	40	100	12	T092	8-20
2N5779	8.0	2.0	25	100	12	T092	8-20
2N5780	8.0	2.0	40	100	12	T092	8-20

Phototransistors

Device	Light Current Typ uA @ mW/cm² H		BV_{CEO} Min. V	Dark Current Max. nA @ V_{CE} V		Package	Page
L14H1	0.5	10	60	100	10	T092	8-3
L14H2	2.0	10	30	100	10	T092	8-3
L14H3	2.0	10	60	100	10	T092	8-3
L14H4	0.5	10	30	100	10	T092	8-3

L14H1 thru L14H4

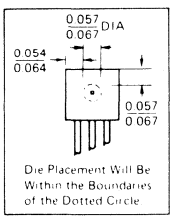
PLASTIC NPN SILICON PHOTO TRANSISTORS

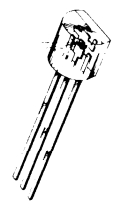
. . . designed for applications in industrial inspection, processing and control, counters, sorters, switching and logic circuits or any design requiring extremely high radiation sensitivity, and stable characteristics.

- Economical Plastic Package
- Sensitive Throughout Visible and Near Infra-Red Spectral Range for Wide Application
- Range of Radiation Sensitivities and Voltages for Design Flexibility
- TO-92 Clear Plastic Package for Standard Mounting
- Annular Passivated Structure for Stability and Reliability
- Ideal Companion to the MLED92 IR Emitter

TO-92 PHOTO TRANSISTORS

NPN SILICON





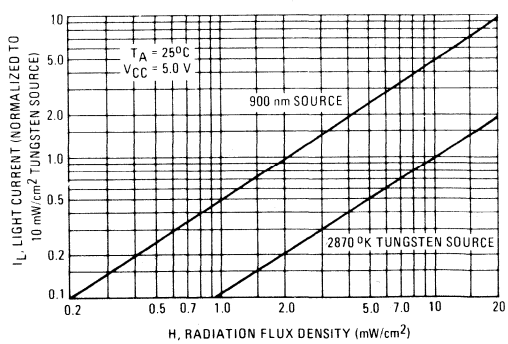
MAXIMUM RATINGS

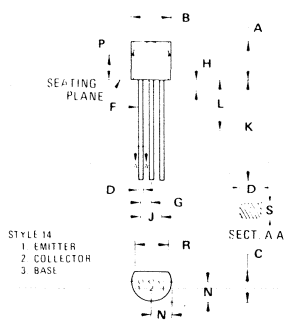
Rating	Symbol	L14H1,3	L14H2,4	Unit
Collector-Emitter Voltage	V_{CEO}	60	30	Volts
Collector-Base Voltage	V_{CBO}	60	30	Volts
Emitter-Base Voltage	V_{EBO}	5.0	5.0	Volts
Light Current	I_L	← 100 →		mA
Total Device Dissipation @ $T_A = 25^oC$	P_D	← 200 →		mW
Derate above 25^oC		← 2.67 →		$mW/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg} (1)	-65 to +100		^oC

*Indicates JEDEC Registered Data.

(1) Heat Sink should be applied to leads during soldering to prevent case temperature from exceeding 100^oC.

FIGURE 1 – NORMALIZED LIGHT CURRENT versus RADIATION FLUX DENSITY





DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

CASE 29-02
TO-92

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DS2650

8

STATIC ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Collector Dark Current (Note 2) (V_{CE} = 10 V)		I_D	–	–	100	nA
Collector-Emitter Breakdown Voltage (Note 2) (I_C = 10 mA)	L14H2, 4 L14H1, 3	BV_{CEO}	 30 60	 – –	 – –	Volts
Collector-Base Breakdown Voltage (Note 2) (I_C = 100 μA) (I_E = 0)	L14H2, 4 L14H1, 3	BV_{CBO}	 30 60	 – –	 – –	Volts
Emitter-Base Breakdown Voltage (Note 2) (I_E = 100 μA, I_C = 0)		BV_{EBO}	5.0	–	–	Volts
Saturation Voltage (I_C = 10 mA, I_B = 1.0 mA)		$V_{CE(sat)}$	–	–	0.4	Volts

OPTICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Collector Light Current (Notes 1, 4, 5) (V_{CE} = 5.0 V, R_L = 100 Ω)	L14H1, 4 L14H2, 3	I_L	 0.5 2.0	 – –	 – –	mA
Turn-On Time (Note 3)	(V_{CE} = 30 V, I_L = 800 μA, R_L = 1.0 kΩ)	t_{on}	–	–	8.0	μs
Turn-Off Time (Note 3)		t_{off}	–	–	7.0	μs

NOTES:

1. Radiation Flux Density (H) equal to 10 mW/cm^2 emitted from a tungsten source at a color temperature of 2870 K.
2. Measured under dark conditions. (H≈0).
3. For unsaturated rise time measurements, radiation is provided by a pulsed GaAs (gallium-arsenide) light-emitting diode (λ ≈ 0.9 μm) with a pulse width equal to or greater than 500 microseconds.
4. Measurement mode with no electrical connection to the base lead.
5. Die faces curved side of package.

FIGURE 2 – CONTINUOUS LIGHT CURRENT versus DISTANCE

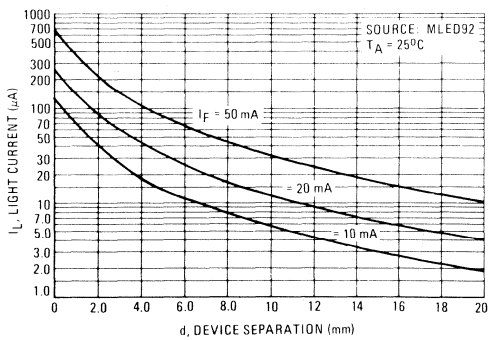
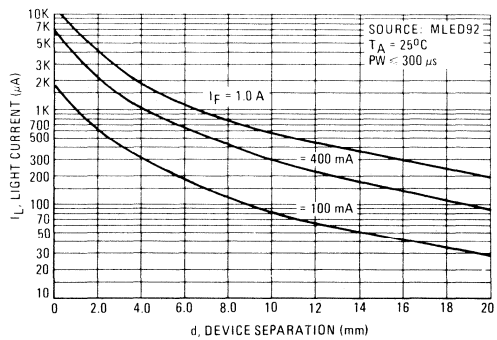


FIGURE 3 – PULSED LIGHT CURRENT versus DISTANCE



MLED92

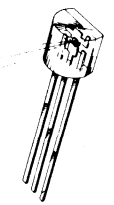
INFRARED-EMITTING DIODE

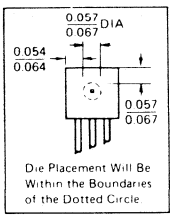
. . . designed for industrial processing and control applications such as light modulators, shaft or position encoders, end of tape detectors, and optical coupler applications. Supplied in TO-92 package for ease of mounting and compatibility with existing automatic insertion equipment.

- High Power Output—
  P_O = 150 μW (Typ) @ I_F = 50 mA
- Infrared-Emission — 9000 Å (Typ)
- One-Piece, Unibloc▲ Package for High Reliability

LOW COST INFRARED-EMITTING DIODE

PN GALLIUM ARSENIDE





MAXIMUM RATINGS

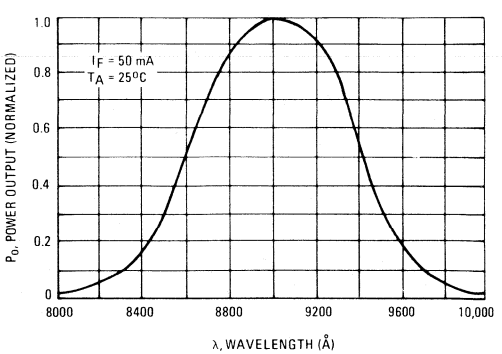
Rating	Symbol	Value	Unit
Reverse Voltage	V_R	3.0	Volts
Forward Current-Continuous	I_F	100	mA
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D(1)	215 2.86	mW mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +100	°C

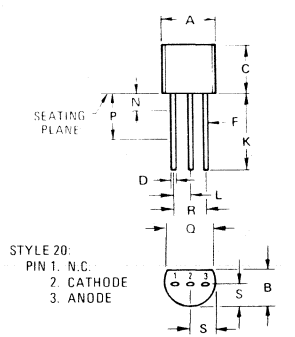
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction to Ambient	$R_{\theta JA}$(1)	350	°C/W

(1) $R_{\theta JA}$(1) is measured with the device soldered into a typical printed circuit board.

FIGURE 1 – RELATIVE SPECTRAL OUTPUT





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

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8

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Fig. No.	Symbol	Min	Typ	Max	Unit
Reverse Leakage Current (V_R = 3.0 V, R_L = 1.0 Megohm)	–	I_R	–	50	–	nA
Reverse Breakdown Voltage (I_R = 100 μA)	–	BV_R	3.0	–	–	Volts
Instantaneous Forward Voltage (Note 3) (I_F = 50 mA)	2	v_F	–	1.2	1.5	Volts
Total Capacitance (V_R = 0 V, f = 1.0 MHz)	–	C_T	–	150	–	pF

OPTICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Fig. No.	Symbol	Min	Typ	Max	Unit
Total Power Output (Notes 1 and 3) (I_F = 50 mA)	3, 4	P_O	50	150	–	μW
Radiant Intensity (Note 2) (I_F = 50 mA)		I_O	–	0.66	–	mW/steradian
Peak Emission Wavelength	1	λ_P		9000		Å
Spectral Line Half Width	1	$\Delta\lambda$		400		Å

NOTE:

1. Power Output, P_O, is the total power radiated by the device into a solid angle of 2π steradians. It is measured by directing all radiation leaving the device, within this solid angle, onto a calibrated silicon solar cell.
2. Irradiance from a Light Emitting Diode (LED) can be calculated by:

   $H = \frac{I_O}{d^2}$ where H is irradiance in mW/cm^2, I_O is radiant intensity in mW/steradian; d is distance from LED to the detector in cm.
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – FORWARD CHARACTERISTICS

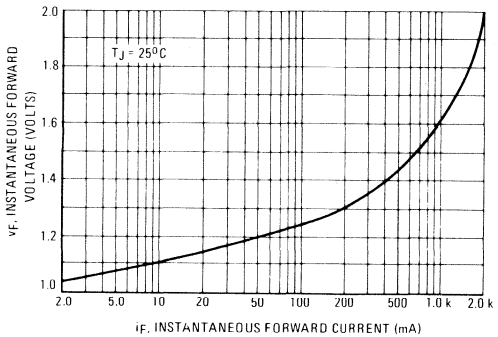


FIGURE 3 – POWER OUTPUT versus JUNCTION TEMPERATURE

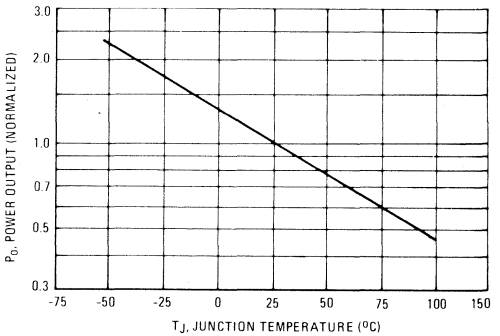


FIGURE 4 – INSTANTANEOUS POWER OUTPUT

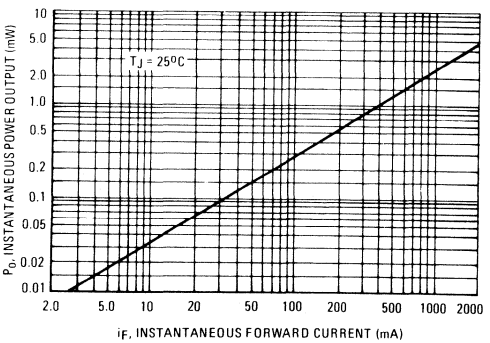
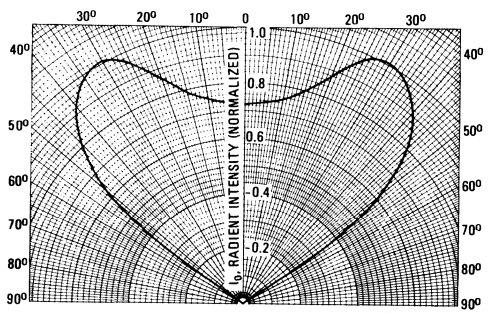


FIGURE 5 – SPATIAL RADIATION PATTERN



MLED93
MLED94
MLED95

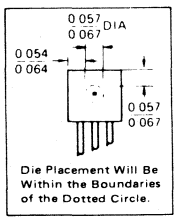
INFRARED-EMITTING DIODE

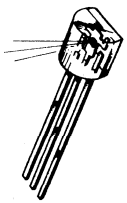
. . . designed for industrial processing and control applications such as light modulators, shaft or position encoders, end of tape detectors, and optical coupler applications. Supplied in TO-92 package for ease of mounting and compatibility with existing automatic insertion equipment.

- High Power Output — (Typ)
  MLED93 — 3.0 mW
  MLED94 — 5.0 mW
  MLED95 — 7.0 mW
  @ I_F = 100 mA (duty cycle ≤2.0%)
- Infrared-Emission — 9300 Å (Typ)
- One-Piece, Unibloc Package for High Reliability

LOW COST INFRARED-EMITTING DIODE

PN GALLIUM ARSENIDE





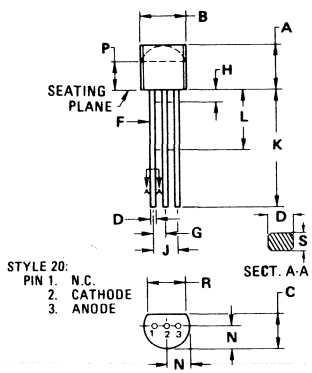
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	6.0	Volts
Forward Current-Continuous	I_F	100	mA
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D(1)	215 2.86	mW mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +100	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction to Ambient	$R_{\theta JA}$(1)	350	°C/W

(1)$R_{\theta JA}$(1) is measured with the device soldered into a typical printed circuit board.

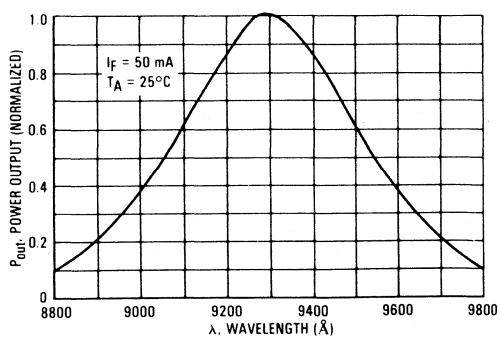


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

CASE 29-02

FIGURE 1 — RELATIVE SPECTRAL OUTPUT



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DS 2543R1

8

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Fig. No.	Symbol	Min	Typ	Max	Unit
Reverse Leakage Current (V_R = 6.0 V, R_L = 1.0 Megohm)	—	I_R	—	50	—	nA
Reverse Breakdown Voltage (I_R = 100 μA)	—	$V_{(BR)}$	6.0	—	—	Volts
Instantaneous Forward Voltage (I_F = 50 mA)	2	v_F	—	1.3	1.8	Volts
Total Capacitance (V_R = 0 V, f = 1.0 MHz)	—	C_T	—	150	—	pF

OPTICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Typ	Max	Unit
Total Power Output (Notes 1 and 3)		3, 4	P_o				mW
(I_F = 100 mA)	MLED93			2.0	3.0	—	
	MLED94			4.0	5.0	—	
	MLED95			6.0	7.0	—	
Radiant Intensity (Notes 2 and 3)			I_o				mW/steradian
(I_F = 100 mA)	MLED93			—	13.2	—	
	MLED94			—	22.0	—	
	MLED95			—	30.8	—	
Peak Emission Wavelength		1	λP	—	9300	—	Å
Spectral Line Half Width		1	$\Delta\lambda$	—	480	—	Å

NOTE:

1. Power Output, P_o, is the total power radiated by the device. It is measured by directing all radiation leaving the device onto a calibrated integrating sphere.
2. Irradiance from a Light Emitting Diode (LED) can be calculated by:

$$H = \frac{I_o}{d_2}$$

where H is irradiance in mW/cm^2, I_o is radiant intensity in mW/steradian; d_2 is distance from LED to the detector in cm.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 — FORWARD CHARACTERISTICS

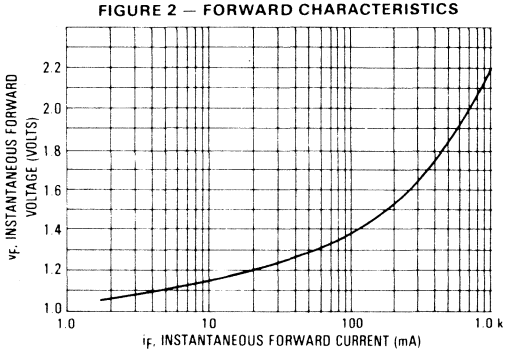


FIGURE 3 — POWER OUTPUT versus JUNCTION TEMPERATURE

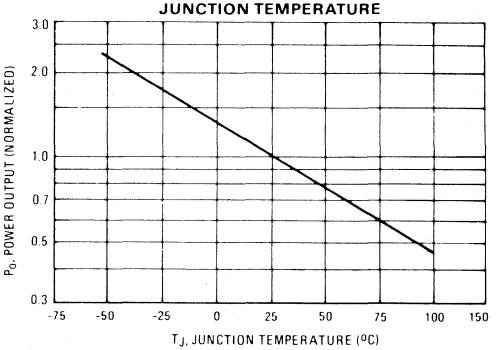


FIGURE 4 — INSTANTANEOUS POWER OUTPUT

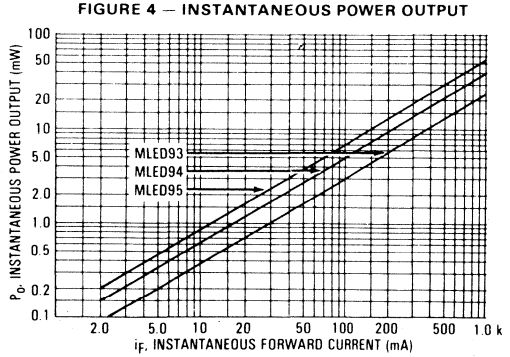
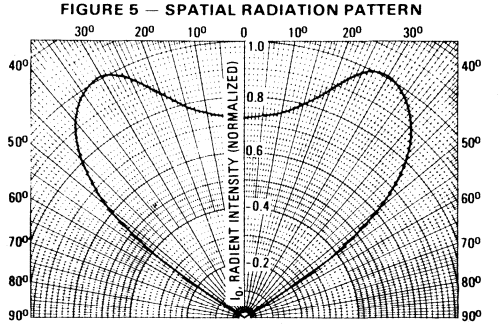


FIGURE 5 — SPATIAL RADIATION PATTERN



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MOC3009
MOC3010
MOC3011

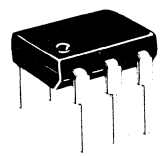
OPTICALLY ISOLATED TRIAC DRIVER

These devices consist of a gallium-arsenide infrared emitting diode, optically coupled to a silicon bilateral switch and are designed for applications requiring isolated triac triggering, low-current isolated ac switching, high electrical isolation (to 7500 V peak), high detector standoff voltage, small size, and low cost.

- UL Recognized File Number 54915

OPTO COUPLER

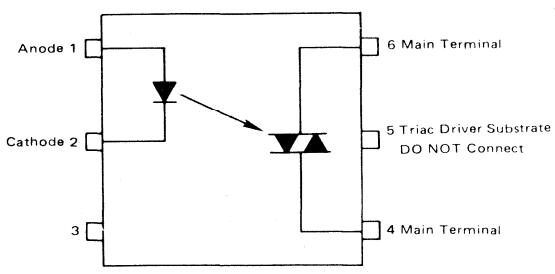
PHOTO TRIAC DRIVER OUTPUT

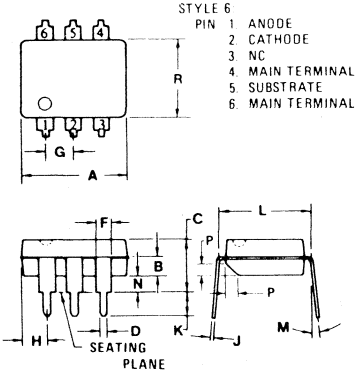


MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INFRARED EMITTING DIODE MAXIMUM RATINGS			
Reverse Voltage	V_R	3.0	Volts
Forward Current — Continuous	I_F	50	mA
Total Power Dissipation @ T_A = 25°C Negligible Power in Transistor Derate above 25°C	P_D	100 1.33	mW mW/°C
OUTPUT DRIVER MAXIMUM RATINGS			
Off-State Output Terminal Voltage	V_{DRM}	250	Volts
On-State RMS Current T_A = 25°C (Full Cycle, 50 to 60 Hz) T_A = 70°C	$I_{T(RMS)}$	100 50	mA mA
Peak Nonrepetitive Surge Current (PW = 10 ms, DC = 10%)	I_{TSM}	1.2	A
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 4.0	mW mW/°C
TOTAL DEVICE MAXIMUM RATINGS			
Isolation Surge Voltage (1) (Peak ac Voltage, 60 Hz, 5 Second Duration)	V_{ISO}	7500	Vac
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	330 4.4	mW mW/°C
Junction Temperature Range	T_J	-40 to +100	°C
Ambient Operating Temperature Range	T_A	-40 to +70	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C
Soldering Temperature (10 s)	—	260	°C

(1) Isolation surge voltage, V_{ISO}, is an internal device dielectric breakdown rating.





NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIAMETER OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.13	8.89	0.320	0.350
B	1.27	2.03	0.050	0.080
C	2.92	5.08	0.115	0.200
D	0.41	0.51	0.016	0.020
F	1.02	1.78	0.040	0.070
G	2.54	BSC	0.100	BSC
H	1.02	2.16	0.040	0.085
J	0.20	0.30	0.008	0.012
K	2.54	3.81	0.100	0.150
L	7.62	BSC	0.300	BSC
M	0°	15°	0°	15°
N	0.38	2.54	0.015	0.100
P	0.81	0.97	0.032	0.038
R	6.10	6.60	0.240	0.260

CASE 730

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
LED CHARACTERISTICS						
Reverse Leakage Current (V_R = 3.0 V)		I_R	–	0.05	100	μA
Forward Voltage (I_F = 10 mA)		V_F	–	1.2	1.5	Volts
DETECTOR CHARACTERISTICS (I_F = 0 unless otherwise noted)						
Peak Blocking Current, Either Direction (Rated V_{DRM}, Note 1)		I_{DRM}	–	10	100	nA
Peak On-State Voltage, Either Direction (I_{TM} = 100 mA Peak)		V_{TM}	–	2.5	3.0	Volts
Critical Rate of Rise of Off-State Voltage, Figure 3		dv/dt	–	2.0	–	V/μs
Critical Rate of Rise of Commutation Voltage, Figure 3 (I_{load} = 15 mA)		dv/dt	–	0.15	–	V/μs
COUPLED CHARACTERISTICS						
LED Trigger Current, Current Required to Latch Output (Main Terminal Voltage = 3.0 V)	MOC3009	I_{FT}		15	30	mA
	MOC3010		–	8.0	15	
	MOC3011		–	5.0	10	
Holding Current, Either Direction		I_H	–	100	–	μA

Note 1. Test voltage must be applied within dv/dt rating.

2. Additional information on the use of the MOC3009/3010/3011 is available in Application Note AN-780A.

TYPICAL ELECTRICAL CHARACTERISTICS
T_A = 25°C

FIGURE 1 – ON-STATE CHARACTERISTICS

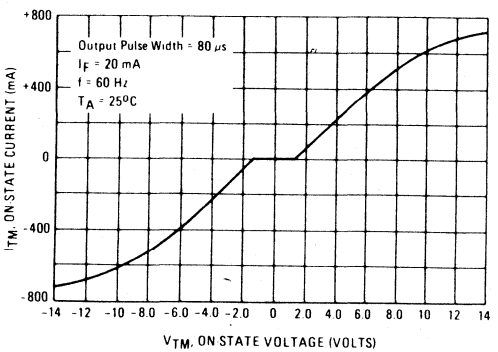


FIGURE 2 – TRIGGER CURRENT versus TEMPERATURE

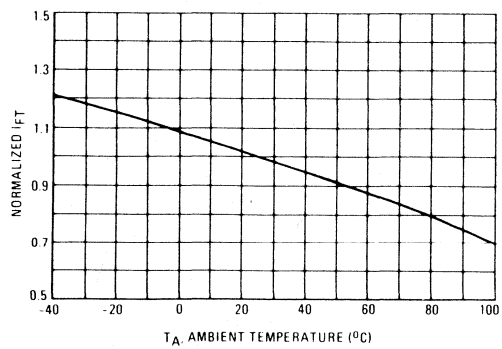


FIGURE 3 – dv/dt TEST CIRCUIT

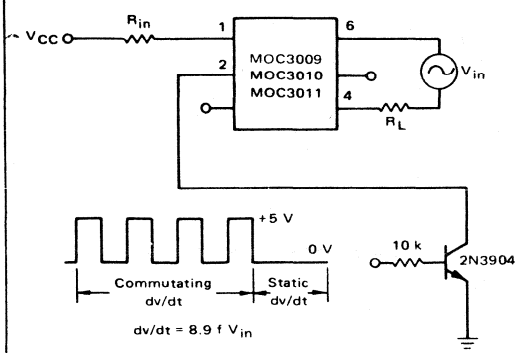


FIGURE 4 – dv/dt versus LOAD RESISTANCE

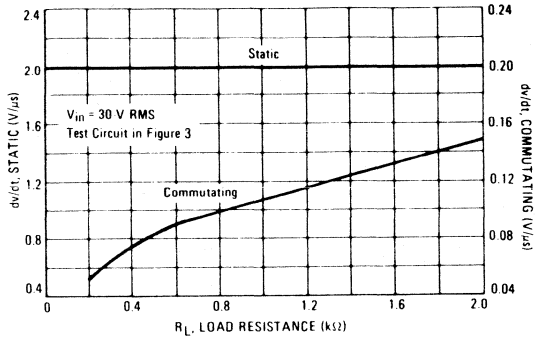


FIGURE 5 – dv/dt versus TEMPERATURE

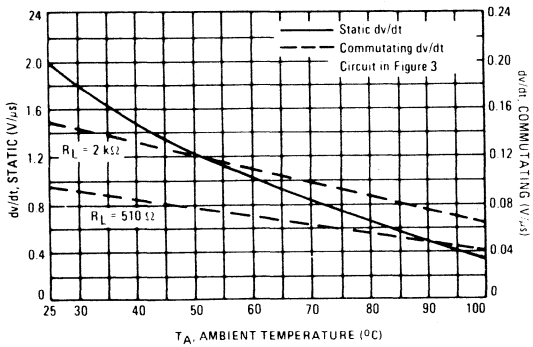


FIGURE 6 – COMMUTATING dv/dt versus FREQUENCY

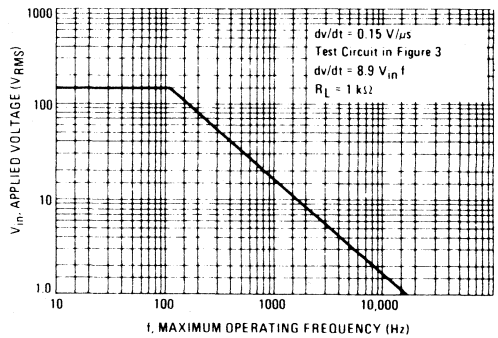
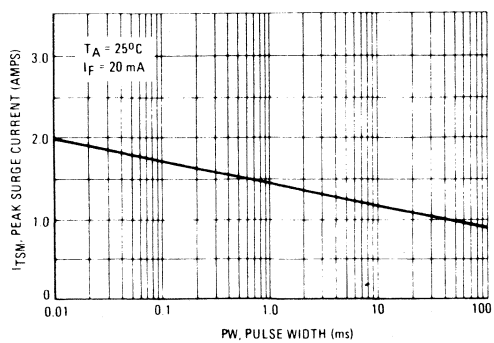


FIGURE 7 – MAXIMUM NONREPETITIVE SURGE CURRENT



8

TYPICAL APPLICATION CIRCUITS

FIGURE 8 – RESISTIVE LOAD

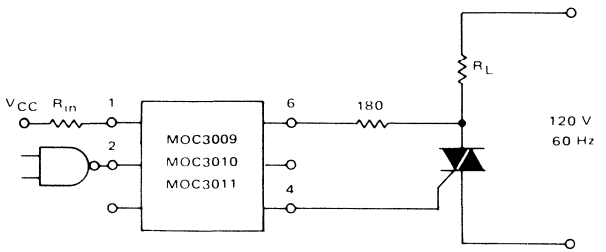


FIGURE 9 – INDUCTIVE LOAD WITH SENSITIVE GATE TRIAC
(I_{GT} 15 mA)

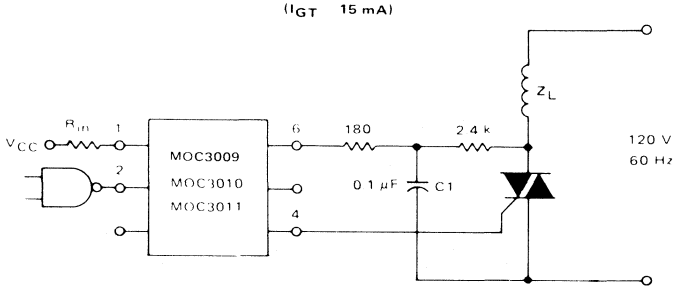
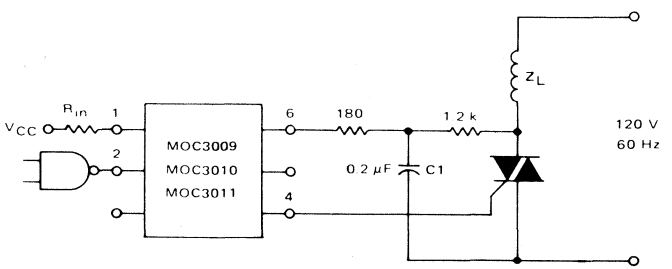


FIGURE 10 – INDUCTIVE LOAD WITH NON-SENSITIVE GATE TRIAC
(15 mA < I_{GT} < 50 mA)



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MOC3020S
MOC3021S

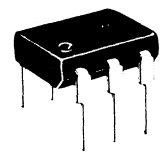
OPTICALLY ISOLATED TRIAC DRIVER

These devices consist of a gallium-arsenide infrared emitting diode, optically coupled to a silicon bilateral switch and are designed for applications requiring isolated triac triggering, low-current isolated ac switching, high electrical isolation (to 7500 V peak), high detector standoff voltage, small size, and low cost.

- UL Recognized File Number 54915

OPTO COUPLER

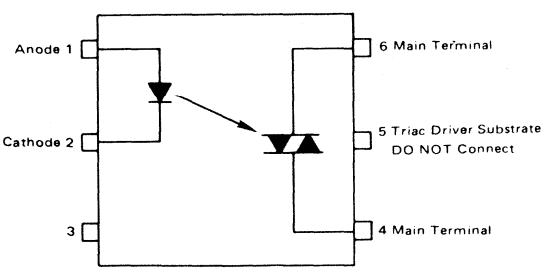
PHOTO TRIAC DRIVER OUTPUT

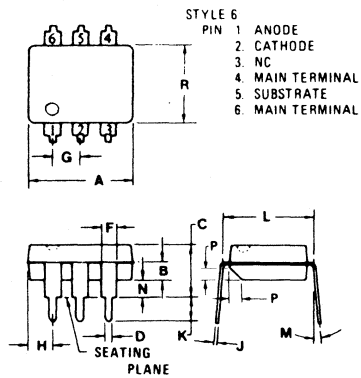


MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INFRARED EMITTING DIODE MAXIMUM RATINGS			
Reverse Voltage	V_R	3.0	Volts
Forward Current – Continuous	I_F	50	mA
Total Power Dissipation @ T_A = 25°C Negligible Power in Transistor Derate above 25°C	P_D	100 1.33	mW mW/°C
OUTPUT DRIVER MAXIMUM RATINGS			
Off-State Output Terminal Voltage	V_{DRM}	400	Volts
On-State RMS Current T_A = 25°C (Full Cycle, 50 to 60 Hz) T_A = 70°C	$I_{T(RMS)}$	100 50	mA mA
Peak Nonrepetitive Surge Current (PW = 10 ms, DC = 10%)	I_{TSM}	1.2	A
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 4.0	mW mW/°C
TOTAL DEVICE MAXIMUM RATINGS			
Isolation Surge Voltage (1) (Peak ac Voltage, 60 Hz, 5 Second Duration)	V_{ISO}	7500	Vac
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	330 4.4	mW mW/°C
Junction Temperature Range	T_J	-40 to +100	°C
Ambient Operating Temperature Range	T_A	-40 to +70	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C
Soldering Temperature (10 s)	–	260	°C

(1) Isolation surge voltage, V_{ISO}, is an internal device dielectric breakdown rating.





NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIAMETER OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.13	8.89	0.320	0.350
B	1.27	2.03	0.050	0.080
C	2.92	5.08	0.115	0.200
D	0.41	0.51	0.016	0.020
F	1.02	1.78	0.040	0.070
G	2.54	BSC	0.100	BSC
H	1.02	2.16	0.040	0.085
J	0.20	0.30	0.008	0.012
K	2.54	3.81	0.100	0.150
L	7.62	BSC	0.300	BSC
M	0°	15°	0°	15°
N	0.38	2.54	0.015	0.100
P	0.81	0.97	0.032	0.038
R	6.10	6.60	0.240	0.260

CASE 730

E-139 – September 1979

8

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
LED CHARACTERISTICS						
Reverse Leakage Current (V_R = 3.0 V)		I_R	–	0.05	100	μA
Forward Voltage (I_F = 10 mA)		V_F	–	1.2	1.5	Volts
DETECTOR CHARACTERISTICS (I_F = 0 unless otherwise noted)						
Peak Blocking Current, Either Direction (Rated V_{DRM}, Note 1)		I_{DRM}	–	10	100	nA
Peak On-State Voltage, Either Direction (I_{TM} = 100 mA Peak)		V_{TM}	–	2.5	3.0	Volts
Critical Rate of Rise of Off-State Voltage, Figure 3		dv/dt		2.0	–	V/μs
Critical Rate of Rise of Commutation Voltage, Figure 3 (I_{load} = 15 mA)		dv/dt		0.15	–	V/μs
COUPLED CHARACTERISTICS						
LED Trigger Current, Current Required to Latch Output (Main Terminal Voltage = 3.0 V)	MOC3020S	I_{FT}	–	10	20	mA
	MOC3021S			8.0	15	
Holding Current, Either Direction		I_H	–	100	–	μA

Note 1. Test voltage must be applied within dv/dt rating.

TYPICAL ELECTRICAL CHARACTERISTICS
T_A = 25°C

FIGURE 1 – ON-STATE CHARACTERISTICS

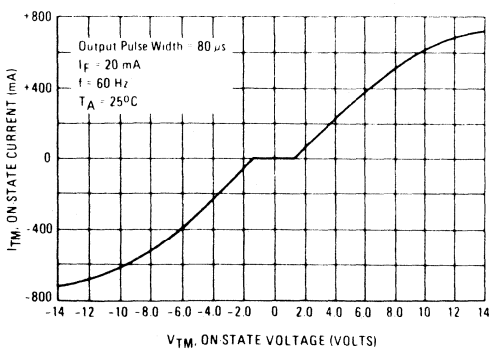


FIGURE 2 – TRIGGER CURRENT versus TEMPERATURE

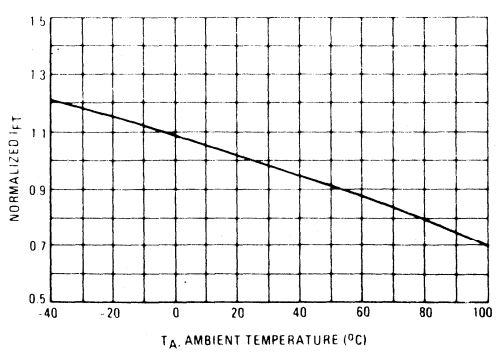


FIGURE 3 – dv/dt TEST CIRCUIT

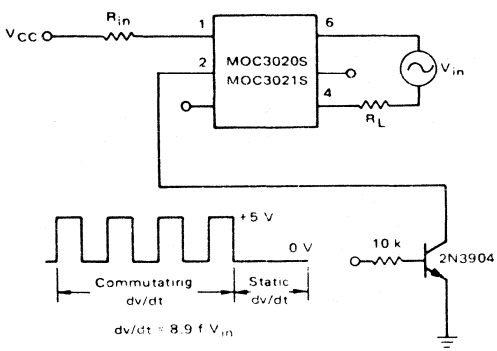


FIGURE 4 – dv/dt versus LOAD RESISTANCE

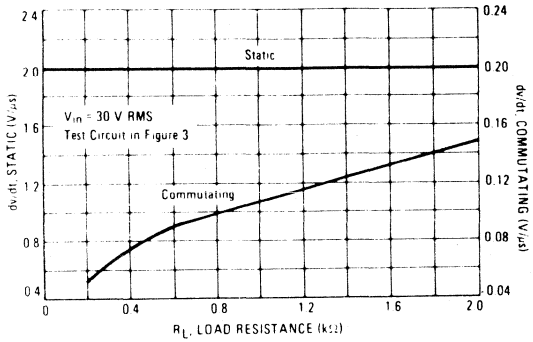


FIGURE 5 – dv/dt versus TEMPERATURE

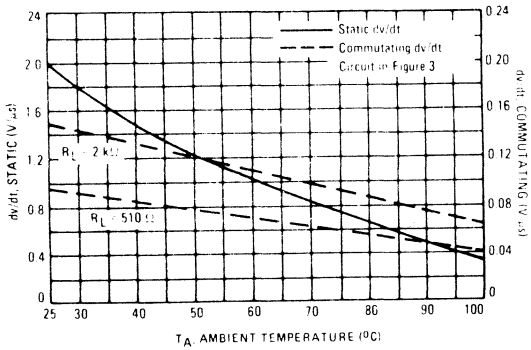
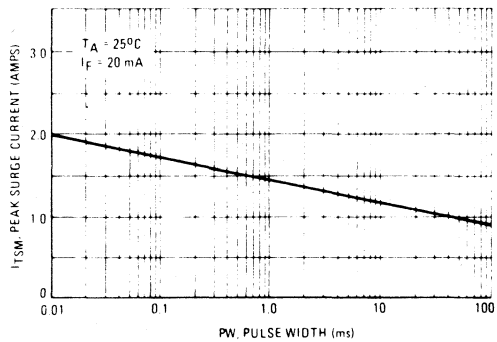


FIGURE 6 – MAXIMUM NON-REPETITIVE SURGE CURRENT



8

TYPICAL APPLICATION CIRCUITS

FIGURE 7 – RESISTIVE LOAD

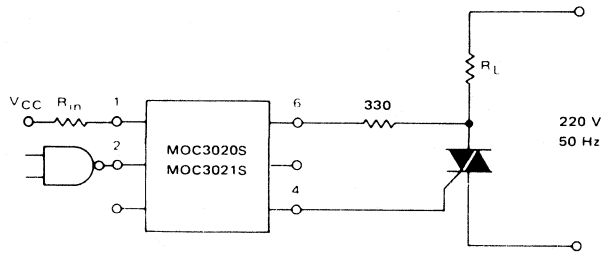


FIGURE 8 – INDUCTIVE LOAD WITH SENSITIVE GATE TRIAC
($I_{GT} \leq 15$ mA)

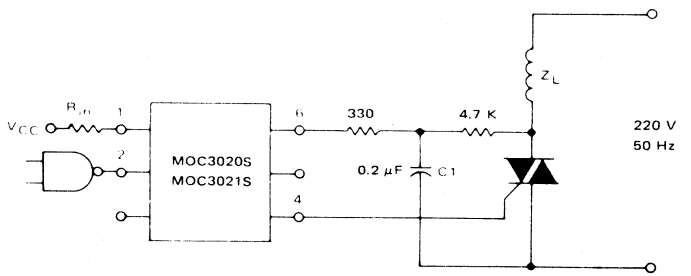
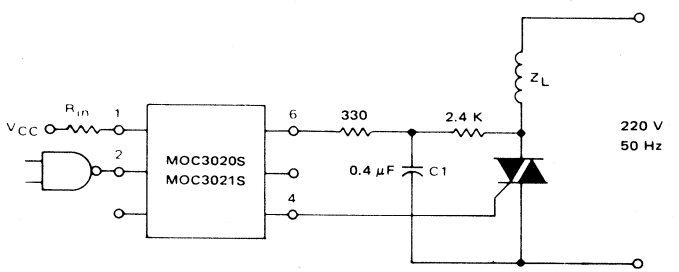


FIGURE 9 – INDUCTIVE LOAD WITH NON-SENSITIVE GATE TRIAC
(15 mA < I_{GT} < 50 mA)



MOC3030
MOC3031

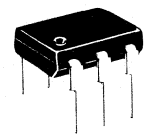
ZERO VOLTAGE CROSSING OPTICALLY ISOLATED TRIAC DRIVER

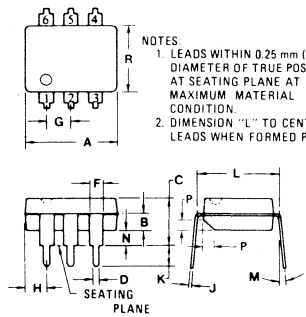
This device consists of a gallium arsenide infrared emitting diode optically coupled to a monolithic silicon detector performing the function of a Zero Voltage crossing bilateral triac driver.

They are designed for use with a triac in the interface of logic systems to equipment powered from 115 Vac lines, such as teletypewriters, CRTs, printers, motors, solenoids and consumer appliances, etc.

- Simplifies Logic Control of 110 Vac Power
- Zero Voltage Crossing
- High Breakdown Voltage: V_{DRM} = 250 V Min
- High Isolation Voltage: V_{ISO} = 7500 V Min
- Small, Economical, 6-Pin DIP Package
- Same Pin Configuration as MOC3010/3011
- UL Recognized, File No. E54915
- dv/dt of 100 V/μs Typ

OPTO COUPLER
ZERO CROSSING TRIAC DRIVER





NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIAMETER OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.13	8.89	0.320	0.350
B	1.27	2.03	0.050	0.080
C	2.92	5.08	0.115	0.200
D	0.41	0.51	0.016	0.020
F	1.02	1.78	0.040	0.070
G	2.54	BSC	0.100	BSC
H	1.02	2.16	0.040	0.085
J	0.20	0.30	0.008	0.012
K	2.54	3.81	0.100	0.150
L	7.62	BSC	0.300	BSC
M	0°	15°	0°	15°
N	0.38	2.54	0.015	0.100
P	0.81	0.97	0.032	0.038
R	6.10	6.60	0.240	0.260

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. NC
4. MAIN TERMINAL
5. SUBSTRATE
6. MAIN TERMINAL

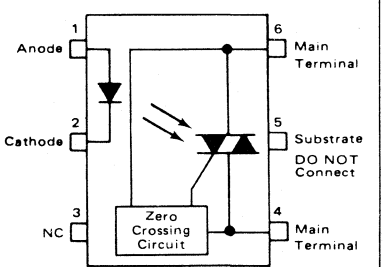
CASE 730-01

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INFRARED EMITTING DIODE MAXIMUM RATINGS			
Reverse Voltage	V_R	3.0	Volts
Forward Current – Continuous	I_F	50	mA
Total Power Dissipation @ T_A = 25°C Negligible Power in Output Driver Derate above 25°C	P_D	120 1.33	mW mW/°C
OUTPUT DRIVER MAXIMUM RATINGS			
Off-State Output Terminal Voltage	V_{DRM}	250	Volts
On-State RMS Current T_A = 25°C (Full Cycle, 50 to 60 Hz) T_A = 85°C	$I_{T(RMS)}$	100 50	mA mA
Peak Nonrepetitive Surge Current (PW = 10 ms)	I_{TSM}	1.2	A
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 4.0	mW mW/°C
TOTAL DEVICE MAXIMUM RATINGS			
Isolation Surge Voltage (1) (Peak ac Voltage, 60 Hz, 5 Second Duration)	V_{ISO}	7500	Vac
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	330 4.4	mW mW/°C
Junction Temperature Range	T_J	-40 to +100	°C
Ambient Operating Temperature Range	T_A	-40 to + 85	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C
Soldering Temperature (10 s)	–	260	°C

(1) Isolation surge voltage, V_{ISO}, is an internal device dielectric breakdown rating.

COUPLER SCHEMATIC



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DS2541
(Replaces ADI-543)

8

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
LED CHARACTERISTICS						
Reverse Leakage Current (V_R = 3.0 V)		I_R	–	0.05	100	μA
Forward Voltage (I_F = 30 mA)		V_F	–	1.3	1.5	Volts
DETECTOR CHARACTERISTICS (I_F = 0 unless otherwise noted)						
Peak Blocking Current, Either Direction (Rated V_{DRM}, Note 1)		I_{DRM}	–	10	100	nA
Peak On-State Voltage, Either Direction (I_{TM} = 100 mA Peak)		V_{TM}	–	1.8	3.0	Volts
Critical Rate of Rise of Off-State Voltage		dv/dt	–	100	–	V/μs
COUPLED CHARACTERISTICS						
LED Trigger Current, Current Required to Latch Output (Main Terminal Voltage = 3.0 V, Note 2)	MOC3030	I_{FT}	–	–	30	mA
	MOC3031		–	–	15	
Holding Current, Either Direction		I_H	–	100	–	μA
ZERO CROSSING CHARACTERISTICS						
Inhibit Voltage (I_F = Rated I_{FT}, MT1-MT2 Voltage above which device will not trigger.)		V_{IH}	–	15	25	Volts
Leakage in Inhibited State (I_F = Rated I_{FT}, Rated V_{DRM}, Off State)		I_R	–	100	200	μA

Note 1. Test voltage must be applied within dv/dt rating.

2. All devices are guaranteed to trigger at an I_F value less than or equal to max I_{FT}. Therefore, recommended operating I_F lies between max I_{FT} (30 mA for MOC3030, 15 mA for MOC3031) and absolute max I_F (50 mA).

TYPICAL ELECTRICAL CHARACTERISTICS
T_A = 25°C

FIGURE 1 – ON-STATE CHARACTERISTICS

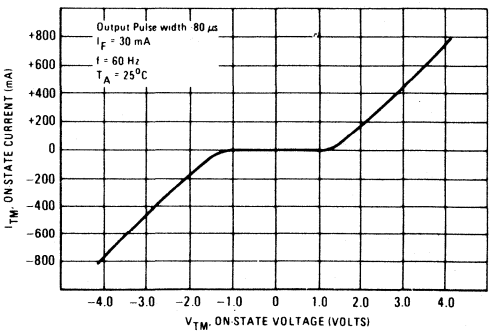


FIGURE 2 – TRIGGER CURRENT versus TEMPERATURE

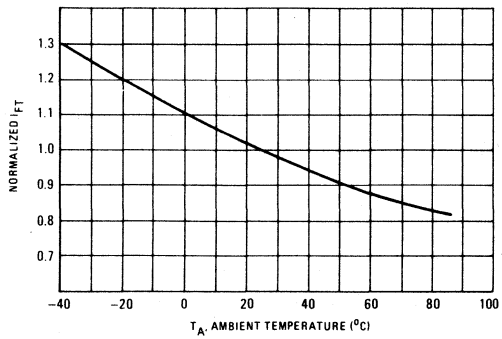
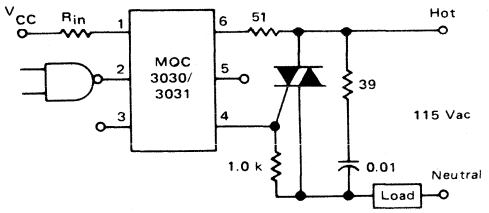


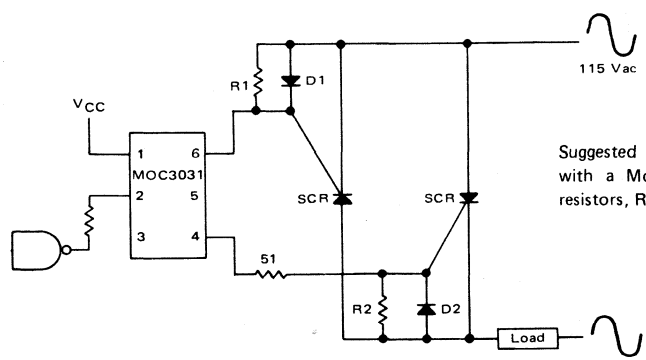
FIGURE 3 – HOT-LINE SWITCHING APPLICATION CIRCUIT



Typical circuit for use when hot line switching is required. In this circuit the "hot" side of the line is switched and the load connected to the cold or neutral side. The load may be connected to either the neutral or hot line.

R_{in} is calculated so that I_F is equal to the rated I_{FT} of the part, 15 mA for the MOC3031 or 30 mA for the MOC3030. The 39 ohm resistor and 0.01 μF capacitor are for snubbing of the triac and may or may not be necessary depending upon the particular triac and load used.

FIGURE 4 – INVERSE-PARALLEL SCR DRIVER CIRCUIT



Suggested method of firing two, back-to-back SCR's, with a Motorola triac driver. Diodes can be 1N4001; resistors, R1 and R2, are optional 1 k ohm.

Motorola reserves the right to make changes to any products herein to improve reliability, function or design. Motorola does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights nor the rights of others.

2N5777 thru 2N5780
MRD14B

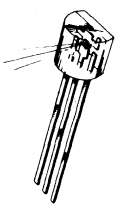
PLASTIC NPN SILICON PHOTO DARLINGTON AMPLIFIERS

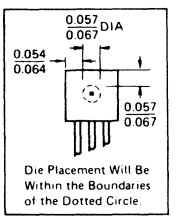
. . . designed for applications in industrial inspection, processing and control, counters, sorters, switching and logic circuits or any design requiring extremely high radiation sensitivity, and stable characteristics.

- Economical Plastic Package
- Sensitive Throughout Visible and Near Infra-Red Spectral Range for Wide Application
- Range of Radiation Sensitivities and Voltages for Design Flexibility
- TO-92 Clear Plastic Package for Standard Mounting
- Annular Passivated Structure for Stability and Reliability
- Precision Die Placement

12, 25, 40 VOLT PHOTO DARLINGTON AMPLIFIERS NPN SILICON

200 MILLIWATTS





Die Placement Will Be Within the Boundaries of the Dotted Circle.

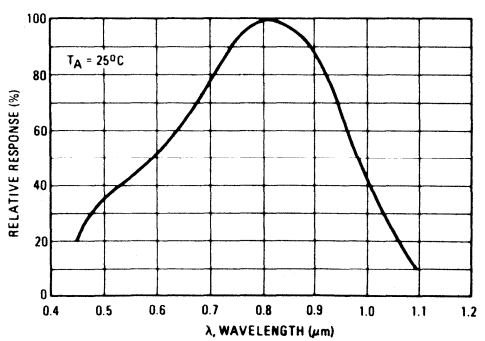
MAXIMUM RATINGS

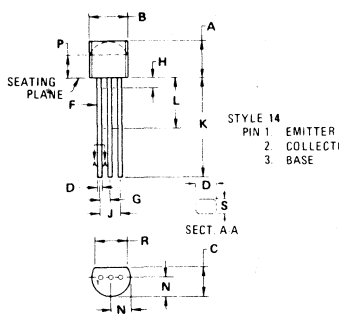
Rating	Symbol	MRD14B	2N5777* 2N5779	2N5778* 2N5780	Unit
Collector-Emitter Voltage	V_{CEO}	12	25	40	Volts
Collector-Base Voltage	V_{CBO}	18	25	40	Volts
Emitter-Base Voltage	V_{EBO}	8.0	8.0	12	Volts
Light Current	I_L	← 250 →			mA
Total Device Dissipation @ $T_A = 25^oC$	P_D	← 200 →			mW
Derate above 25^oC		← 2.67 →			$mW/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg} (1)	-65 to +100			^oC

*Indicates JEDEC Registered Data.

(1) Heat Sink should be applied to leads during soldering to prevent case temperature from exceeding 100^oC.

FIGURE 1 – CONSTANT ENERGY SPECTRAL RESPONSE





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

CASE 29-02
TO-92

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DS 2617 R1

* STATIC ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Collector Dark Current (Note 2) (V_{CE} = 12 V)		I_{CEO}	–	–	0.1	μA
Collector-Emitter Breakdown Voltage (Note 2) (I_C = 10 mA)		BV_{CEO}				Volts
	MRD14B		12	–	–	
	2N5777, 2N5779		25	–	–	
	2N5778, 2N5780		40	–	–	
Collector-Base Breakdown Voltage (Note 2) (I_C = 100 μA)		BV_{CBO}				Volts
	MRD14B		18	–	–	
	2N5777, 2N5779		25	–	–	
	2N5778, 2N5780		40	–	–	
Emitter-Base Breakdown Voltage (Note 2) (I_E = 100 μA)		BV_{EBO}				Volts
	MRD14B		8.0	–	–	
	2N5777, 2N5779		8.0	–	–	
	2N5778, 2N5780		12	–	–	

* OPTICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Typ	Max	Unit
Collector Light Current (Notes 1,4,5) (V_{CE} = 5.0 V)		–	I_L				mA
	MRD14B			0.5	2.0	–	
	2N5777, 2N5778			0.5	4.0	–	
	2N5779, 2N5780			2.0	8.0	–	
DC Current Gain (Note 2) (V_{CE} = 5.0 V, I_C = 0.5 mA)		–	h_{FE}				–
	2N5777, 2N5778			2.5 k	–	–	
	2N5779, 2N5780			5.0 k	–	–	
Wave Length of Maximum Sensitivity		1	λ_s	0.7	0.8	1.0	μm
Turn-On Delay Time (Notes 3, 4)		2,3	t_{d1}	–	–	100	μs
Rise Time (Notes 3, 4)		2,3	t_r	–	–	250	μs
Turn-Off Delay Time (Notes 3, 4)		2,3	t_{d2}	–	–	5.0	μs
Fall Time (Notes 3, 4)		2,3	t_f	–	–	150	μs
Collector-Base Capacitance (V_{CB} = 10 V, f = 1.0 MHz, I_E = 0)	2N5777 thru 2N5780	–	C_{cb}	–	–	10	pF

*Indicates JEDEC Registered Data.

NOTES:

1. Radiation Flux Density (H) equal to 2.0 mW/cm^2 emitted from a tungsten source at a color temperature of 2870 K.
2. Measured under dark conditions. (H≈0).
3. For unsaturated rise time measurements, radiation is provided by a pulsed GaAs (gallium-arsenide) light-emitting diode (λ ≈ 0.9 μm) with a pulse width equal to or greater than 500 microseconds (see Figures 2 and 3).
4. Measurement mode with no electrical connection to the base lead.
5. Die faces curved side of package.

FIGURE 2 – PULSE RESPONSE TEST CIRCUIT

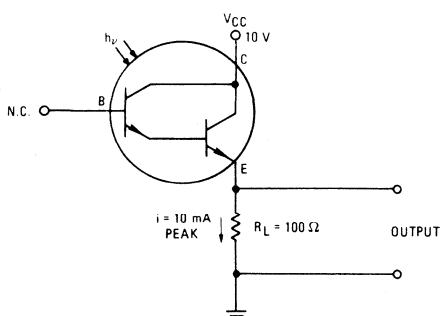
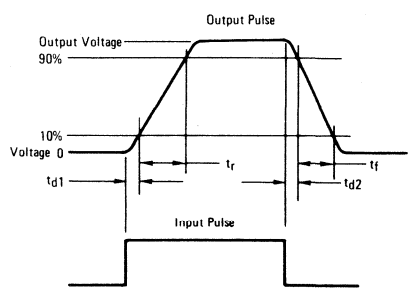


FIGURE 3 – PULSE RESPONSE TEST WAVEFORM



8

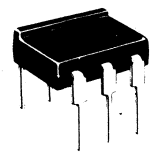
4N25 • 4N25A
4N26 • 4N27 • 4N28

NPN PHOTOTRANSISTOR AND PN INFRARED EMITTING DIODE

...Gallium Arsenide LED optically coupled to a Silicon Photo Transistor designed for applications requiring electrical isolation, high-current transfer ratios, small package size and low cost; such as interfacing and coupling systems, phase and feedback controls, solid-state relays and general-purpose switching circuits.

- High Isolation Voltage —
  V_{ISO} = 2500 V (Min) — 4N25,A
  1500 V (Min) — 4N26,4N27
  500 V (Min) — 4N28
- High Collector Output Current @ I_F = 10 mA —
  I_C = 3.5 mA (Typ) — 4N25,A,4N26
  2.0 mA (Typ) — 4N27,4N28
- Economical, Compact, Dual-In-Line Package
- Excellent Frequency Response — 300 kHz (Typ)
- Fast Switching Times @ I_C = 10 mA
  t_{on} = 0.87 μs (Typ) — 4N25,A,4N26
  2.1 μs (Typ) — 4N27,4N28
  t_{off} = 11 μs (Typ) — 4N25,A,4N26
  5.0 μs (Typ) — 4N27,4N28
- 4N25A is UL Recognized

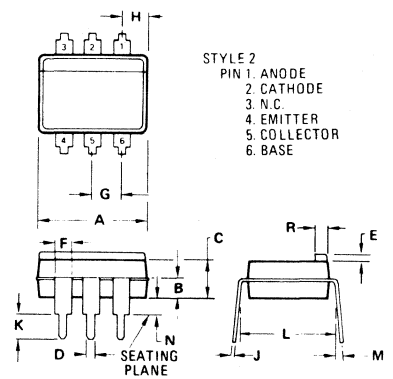
INFRARED LIGHT EMITTING DIODE
PHOTOTRANSISTOR
COUPLED PAIR



***MAXIMUM RATINGS** (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INFRARED EMITTING DIODE MAXIMUM RATINGS			
Reverse Voltage	V_R	3.0	Volts
Forward Current — Continuous	I_F	80	mA
Forward Current — Peak (Pulse Width = 300 μs, 2.0% Duty Cycle)	I_F	3.0	Amp
Total Power Dissipation @ T_A = 25°C (Negligible Power in Transistor)	P_D	150	mW
Derate above 25°C		2.0	mW/°C
PHOTOTRANSISTOR MAXIMUM RATINGS			
Collector-Emitter Voltage	V_{CEO}	30	Volts
Emitter-Collector Voltage	V_{ECO}	7.0	Volts
Collector-Base Voltage	V_{CBO}	70	Volts
Total Device Dissipation @ T_A = 25°C	P_D	150	mW
Negligible Power in Diode			
Derate above 25°C		2.0	mW/°C
TOTAL DEVICE RATINGS			
Total Device Dissipation @ T_A = 25°C	P_D	250	mW
Equal Power Dissipation in Each Element			
Derate above 25°C		3.3	mW/°C
Junction Temperature Range	T_J	-55 to +100	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Soldering Temperature (10 s)		260	°C

*Indicates JEDEC Registered Data.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.38	8.89	0.330	0.350
B	1.40	1.65	0.055	0.065
C	2.92	3.18	0.115	0.125
D	0.38	0.53	0.015	0.021
E	—	1.02	—	0.040
F	1.02	1.27	0.040	0.050
G	2.54 BSC		0.100 BSC	
H	1.57	1.83	0.062	0.072
J	0.23	0.28	0.009	0.011
K	2.92	3.30	0.115	0.130
L	7.37	7.87	0.290	0.310
M	—	10°	—	10°
N	0.51	1.27	0.020	0.050
R	—	1.90	—	0.075

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. INDEX FOR PIN NO. 1 ORIENT.

CASE 673-04

FIGURE 1 — MAXIMUM POWER DISSIPATION

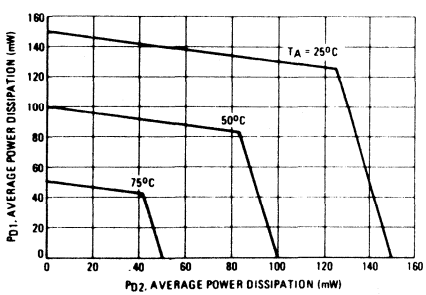


Figure 1 is based upon using limit values in the equation:

$T_{J1} - T_A = R_{\theta JA} (P_{D1} + K_\theta P_{D2})$

where:

T_{J1} Junction Temperature (100°C)
T_A Ambient Temperature
$R_{\theta JA}$ Junction to Ambient Thermal Resistance (500°C/W)
P_{D1} Power Dissipation in One Chip
P_{D2} Power Dissipation in Other Chip
K_θ Thermal Coupling Coefficient (20%)

Example:
With P_{D1} = 90 mW in the LED @ T_A = 50°C, the transistor P_D (P_{D2}) must be less than 50 mW.

LED CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
*Reverse Leakage Current (V_R = 3.0 V, R_L = 1.0 M ohms)	I_R	–	0.05	100	μA
*Forward Voltage (I_F = 10 mA)	V_F	–	1.2	1.5	Volts
Capacitance (V_R = 0 V, f = 1.0 MHz)	C	–	150	–	pF

PHOTOTRANSISTOR CHARACTERISTICS (T_A = 25°C and I_F = 0 unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
*Collector-Emitter Dark Current (V_{CE} = 10 V, Base Open)	4N25,A, 4N26, 4N27	I_{CEO}	–	3.5	50	nA
	4N28		–	–	100	
*Collector-Base Dark Current (V_{CB} = 10 V, Emitter Open)		I_{CBO}	–	–	20	nA
*Collector-Base Breakdown Voltage (I_C = 100 μA, I_E = 0)		BV_{CBO}	70	–	–	Volts
*Collector-Emitter Breakdown Voltage (I_C = 1.0 mA, I_B = 0)		BV_{CEO}	30	–	–	Volts
*Emitter-Collector Breakdown Voltage (I_E = 100 μA, I_B = 0)		BV_{ECO}	7.0	–	–	Volts
DC Current Gain (V_{CE} = 5.0 V, I_C = 500 μA)		h_{FE}	–	250	–	–

COUPLED CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
*Collector Output Current (1) (V_{CE} = 10 V, I_F = 10 mA, I_B = 0)	4N25,A, 4N26	I_C	2.0	3.5	–	mA
	4N27,4N28		1.0	2.0	–	
*Isolation Voltage (2) (60 Hz Peak)	4N25,A	V_{ISO}	2500	–	–	Volts
	4N26,4N27		1500	–	–	
	4N28		500	–	–	
(60 Hz RMS For 1 Second) (3)	4N25A		1775	–	–	
Isolation Resistance (2) (V = 500 V)		–	–	10^{11}	–	Ohms
*Collector-Emitter Saturation (I_C = 2.0 mA, I_F = 50 mA)		$V_{CE(sat)}$	–	0.2	0.5	Volts
Isolation Capacitance (2) (V = 0, f = 1.0 MHz)		–	–	1.3	–	pF
Bandwidth (4) (I_C = 2.0 mA, R_L = 100 ohms, Figure 11) Note 2		–	–	300	–	kHz

SWITCHING CHARACTERISTICS

Delay Time	(I_C = 10 mA, V_{CC} = 10 V) Figures 6 and 8	4N25,A,4N26	t_d	–	0.07	–	μs
		4N27,4N28		–	0.10	–	
Rise Time		4N25,A,4N26	t_r	–	0.8	–	μs
		4N27,4N28		–	2.0	–	
Storage Time	(I_C = 10 mA, V_{CC} = 10 V) Figures 7 and 8	4N25,A,4N26	t_s	–	4.0	–	μs
		4N27,4N28		–	2.0	–	
Fall Time		4N25,A,4N26	t_f	–	7.0	–	μs
		4N27,4N28		–	3.0	–	

*Indicates JEDEC Registered Data (1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%
(2) For this test, LED pins 1 and 2 are common and Photo Transistor pins 4, 5 and 6 are common
(3) RMS Volts, 60 Hz, For this test, pins 1, 2, and 3 are common and pins 4, 5, and 6 are common
(4) I_F adjusted to yield I_C = 2.0 mA and i_c = 2.0 mA p-p at 10 kHz

DC CURRENT TRANSFER CHARACTERISTICS

FIGURE 2 – 4N25,A,4N26

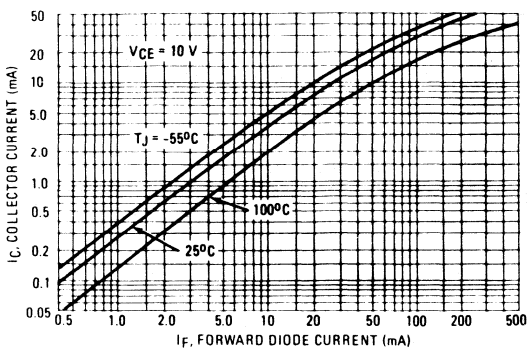
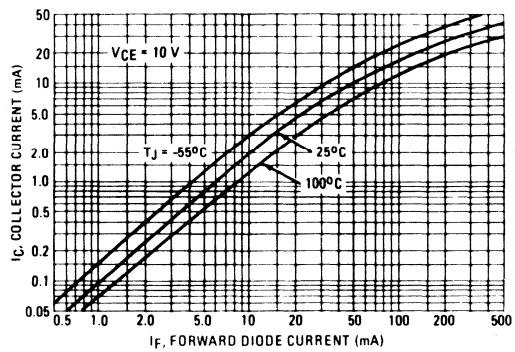


FIGURE 3 – 4N27, 4N28



8

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 4 – DIODE FORWARD CHARACTERISTICS

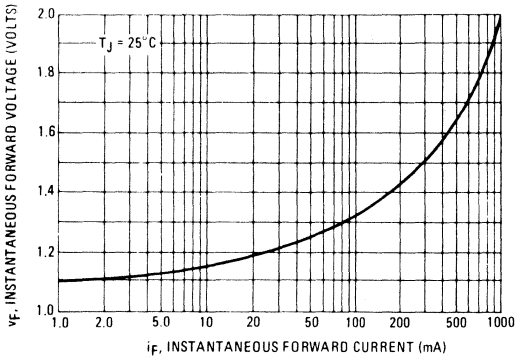


FIGURE 5 – COLLECTOR SATURATION VOLTAGE

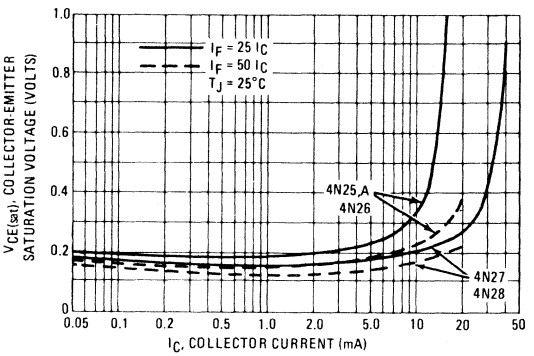


FIGURE 6 – TURN-ON TIME

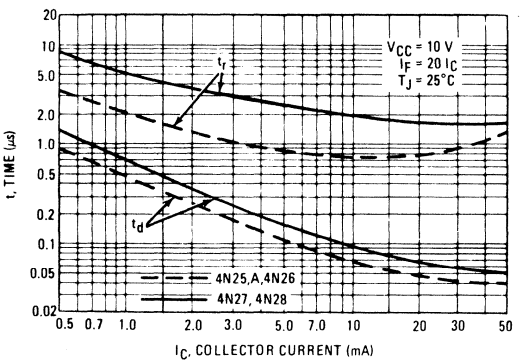


FIGURE 7 – TURN-OFF TIME

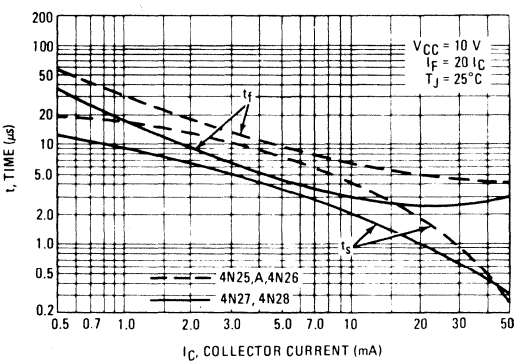


FIGURE 8 – SATURATED SWITCHING TIME TEST CIRCUIT

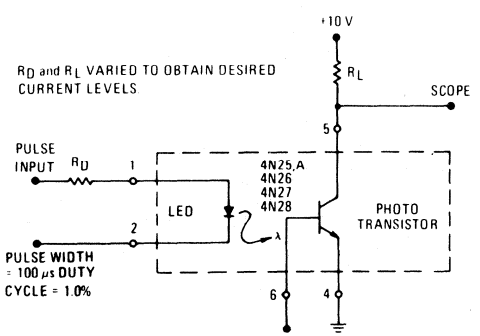


FIGURE 9 – DARK CURRENT versus AMBIENT TEMPERATURE

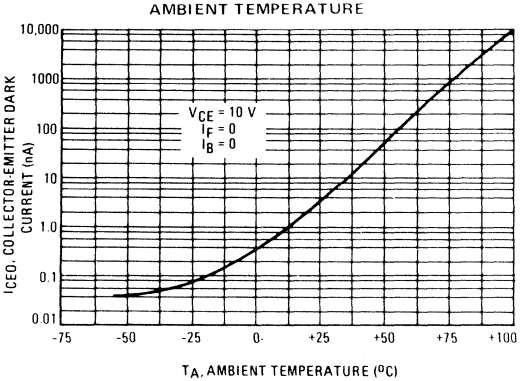


FIGURE 10 – FREQUENCY RESPONSE

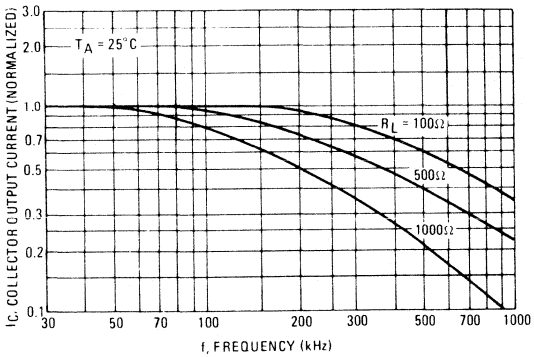
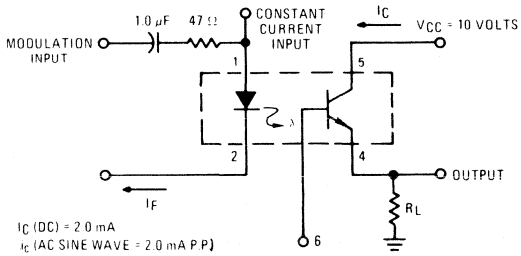


FIGURE 11 – FREQUENCY RESPONSE TEST CIRCUIT



TYPICAL APPLICATIONS

FIGURE 12 – ISOLATED MTTL TO MOS (P-CHANNEL) LEVEL TRANSLATOR

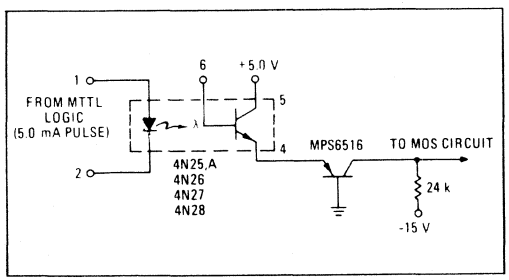


FIGURE 13 – COMPUTER/PERIPHERAL INTERCONNECT

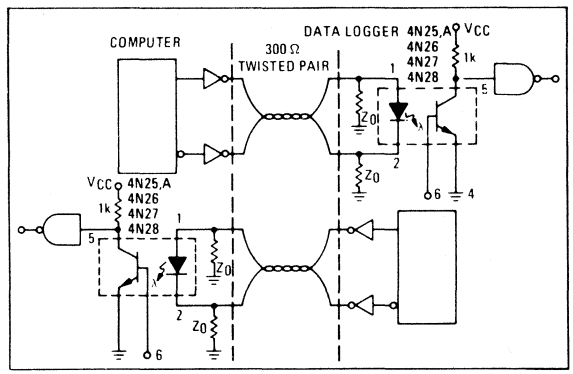


FIGURE 14 – POWER AMPLIFIER

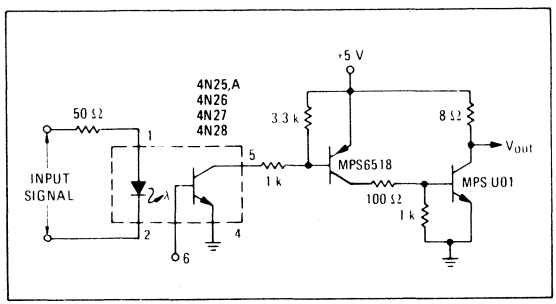
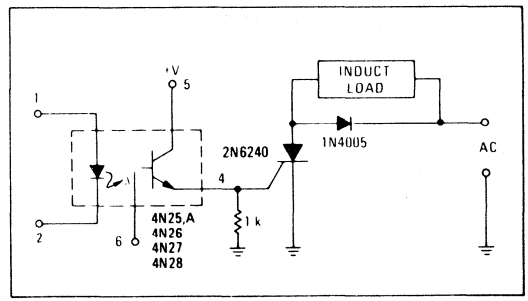


FIGURE 15 – INTERFACE BETWEEN LOGIC AND LOAD



8

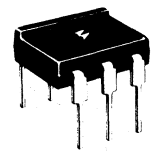
4N29 • 4N30 (MOC1200)
4N31 • 4N32 • 4N33

NPN PHOTOTRANSISTOR AND PN INFRARED EMITTING DIODE

. . . Gallium Arsenide LED optically coupled to a Silicon Photo Darlington Transistor designed for applications requiring electrical isolation, high-current transfer ratios, small package size and low cost; such as interfacing and coupling systems, phase and feedback controls, solid-state relays and general-purpose switching circuits.

- High Isolation Voltage — V_{ISO} = 2500 V (Min) — 4N29,32; 1500 V (Min) — 4N30,31,33
- Excellent Frequency Response — 30 kHz (Typ)
- High Collector Output Current @ I_F = 10 mA — I_C = 50 mA (Min) — 4N32,33; 10 mA (Min) — 4N29,30; 5.0 mA (Min) — 4N31
- Fast Switching Times @ I_C = 50 mA t_{on} = 0.6 μs (Typ) t_{off} = 17 μs (Typ) — 4N29,30,31; 45 μs (Typ) — 4N32,33
- Economical, Compact, Dual-In-Line Package

INFRARED LIGHT EMITTING DIODE PHOTO DARLINGTON TRANSISTOR COUPLED PAIR



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INFRARED EMITTING DIODE MAXIMUM RATINGS			
Reverse Voltage	V_R	3.0	Volts
Forward Current — Continuous	I_F	80	mA
Forward Current — Peak (Pulse Width = 300 μs, 2.0% Duty Cycle)	I_F	3.0	Amp
Total Power Dissipation @ T_A = 25°C Negligible Power in Transistor Derate above 25°C	P_D	150 2.0	mW mW/°C
PHOTOTRANSISTOR MAXIMUM RATINGS			
Collector-Emitter Voltage	V_{CEO}	30	Volts
Emitter-Collector Voltage	V_{ECO}	5.0	Volts
Collector-Base Voltage	V_{CBO}	30	Volts
Total Power Dissipation @ T_A = 25°C Negligible Power in Diode Derate above 25°C	P_D	150 2.0	mW mW/°C
TOTAL DEVICE RATINGS			
Total Device Dissipation @ T_A = 25°C Equal Power Dissipation in Each Element Derate above 25°C	P_D	250 3.3	mW mW/°C
Operating Junction Temperature Range	T_J	-55 to +100	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Soldering Temperature (10 s)	—	260	°C

FIGURE 1 — MAXIMUM POWER DISSIPATION

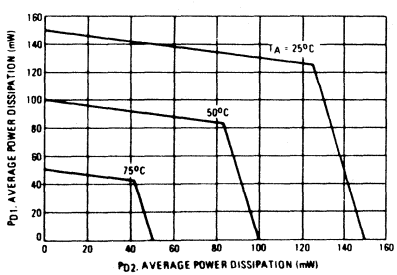


Figure 1 is based upon using limit values in the equation:

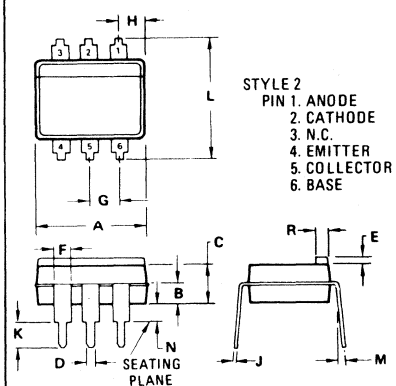
$T_{J1} - T_A = R_{\theta JA} (P_{D1} + K_\theta P_{D2})$

where:

T_{J1} Junction Temperature (100°C)
T_A Ambient Temperature
$R_{\theta JA}$ Junction to Ambient Thermal Resistance (500°C/W)
P_{D1} Power Dissipation in One Chip
P_{D2} Power Dissipation in Other Chip
K_θ Thermal Coupling Coefficient (20%)

Example:

With P_{D1} = 90 mW in the LED @ T_A = 50°C, the Darlington P_D (P_{D2}) must be less than 50 mW.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.38	8.89	0.330	0.350
B	1.40	1.65	0.055	0.065
C	2.92	3.18	0.115	0.125
D	0.41	0.51	0.016	0.020
E	0.64	0.89	0.025	0.035
F	1.14	1.40	0.045	0.055
G	2.54 BSC		0.100 BSC	
H	1.57	1.83	0.062	0.072
J	0.23	0.28	0.009	0.011
K	2.54	3.30	0.100	0.130
L	7.37	7.87	0.290	0.310
M	—	5°	—	5°
N	—	1.27	—	0.050
R	1.52	1.78	0.060	0.070

CASE 673-03

LED CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Reverse Leakage Current (V_R = 3.0 V, R_L = 1.0 M ohms)	I_R	–	0.05	100	μA
*Forward Voltage (I_F = 50 mA)	V_F	–	1.2	1.5	Volts
Capacitance (V_R = 0 V, f = 1.0 MHz)	C	–	150	–	pF

PHOTOTRANSISTOR CHARACTERISTICS (T_A = 25°C and I_F = 0 unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Collector-Emitter Dark Current (V_{CE} = 10 V, Base Open)	I_{CEO}	–	–	100	nA
*Collector-Base Breakdown Voltage (I_C = 100 μA, I_E = 0)	BV_{CBO}	30	–	–	Volts
*Collector-Emitter Breakdown Voltage (I_C = 100 μA, I_B = 0)	BV_{CEO}	30	–	–	Volts
*Emitter-Collector Breakdown Voltage (I_E = 100 μA, I_B = 0)	BV_{ECO}	5.0	–	–	Volts
DC Current Gain (V_{CE} = 5.0 V, I_C = 500 μA)	h_{FE}	–	5000	–	–

COUPLED CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
*Collector Output Current (1) (V_{CE} = 10 V, I_F = 10 mA, I_B = 0)	4N32, 4N33	I_C	50	–	–	mA
	4N29, 4N30		10	–	–	
	4N31		5.0	–	–	
*Isolation Voltage (2)	4N29, 4N32	V_{ISO}	2500	–	–	Volts
	4N30, 4N31, 4N33		1500	–	–	
Isolation Resistance (2) (V = 500 V)		–	–	10^{11}	–	Ohms
*Collector-Emitter Saturation Voltage (1)	4N31	$V_{CE(sat)}$	–	–	1.2	Volts
(I_C = 2.0 mA, I_F = 8.0 mA)	4N29, 4N30, 4N32, 4N33		–	–	1.0	
Isolation Capacitance (2) (V = 0, f = 1.0 MHz)		–	–	0.8	–	pF
Bandwidth (3) (I_C = 2.0 mA, R_L = 100 ohms, Figures 6 and 8)		–	–	30	–	kHz

SWITCHING CHARACTERISTICS (Figures 7 and 9), (4)

Turn-On Time (I_C = 50 mA, I_F = 200 mA, V_{CC} = 10 V)		t_{on}	–	0.6	5.0	μs
Turn-Off Time (I_C = 50 mA, I_F = 200 mA, V_{CC} = 10 V)	4N29,30,31	t_{off}	–	17	40	μs
	4N32,33		–	45	100	

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%

(2) For this test LED pins 1 and 2 are common and Photo Transistor pins 4,5 and 6 are common.

(3) I_F adjusted to yield I_C = 2.0 mA and i_c = 2.0 mA P-P at 10 kHz.

(4) t_d and t_r are inversely proportional to the amplitude of I_F; t_s and t_f are not significantly affected by I_F.

DC CURRENT TRANSFER CHARACTERISTICS

FIGURE 2 – 4N29, 4N30, 4N31

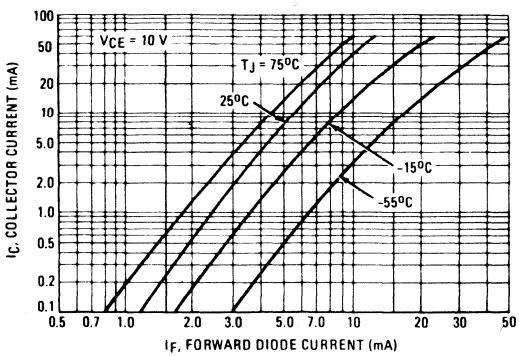
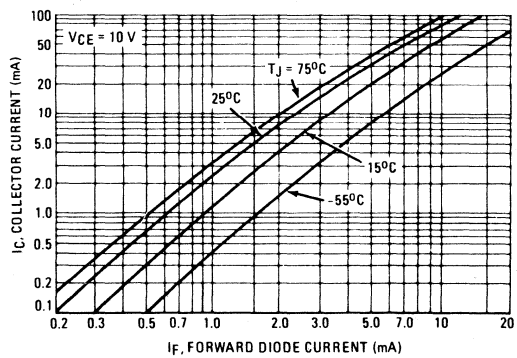


FIGURE 3 – 4N32, 4N33



8

TYPICAL ELECTRICAL CHARACTERISTICS
(Printed Circuit Board Mounting)

FIGURE 4 – DIODE FORWARD CHARACTERISTIC

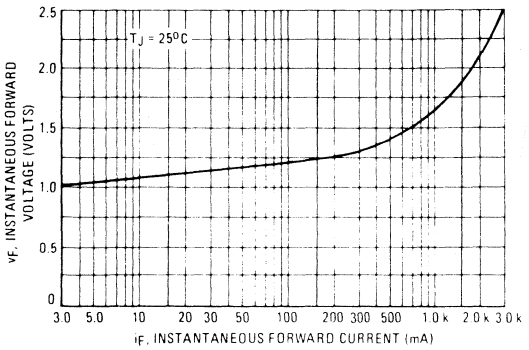


FIGURE 5 – COLLECTOR-EMITTER CUTOFF CURRENT

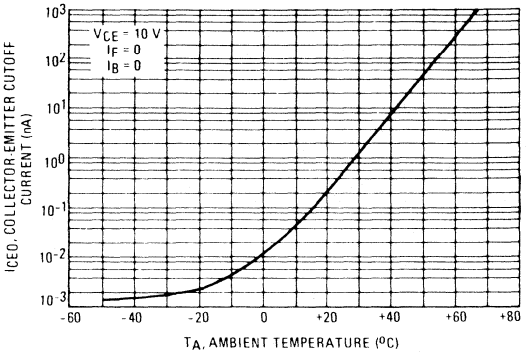


FIGURE 6 – FREQUENCY RESPONSE

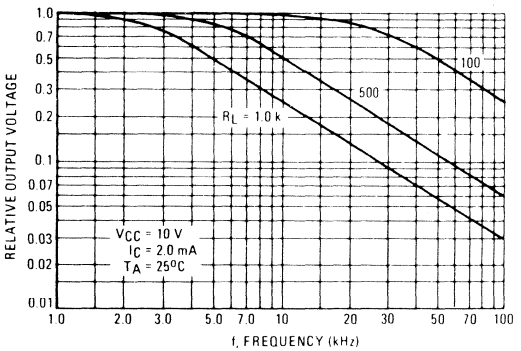


FIGURE 7 – SWITCHING TIMES

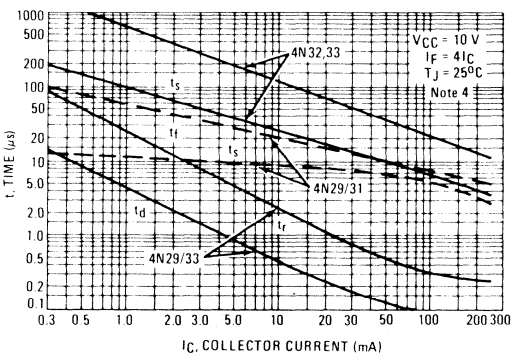


FIGURE 8 – FREQUENCY RESPONSE TEST CIRCUIT

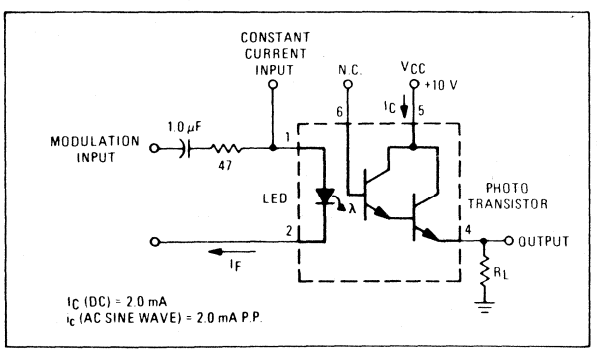
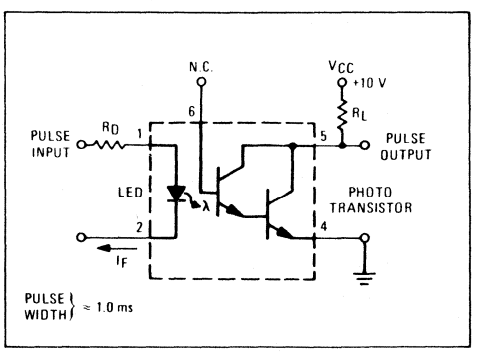


FIGURE 9 – SWITCHING TIME TEST CIRCUIT



TYPICAL APPLICATIONS

FIGURE 10 – VOLTAGE CONTROLLED TRIAC

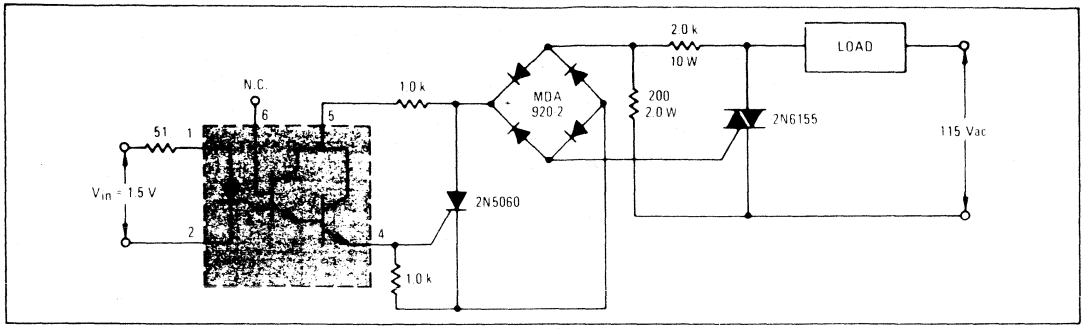


FIGURE 11 – AC SOLID STATE RELAY

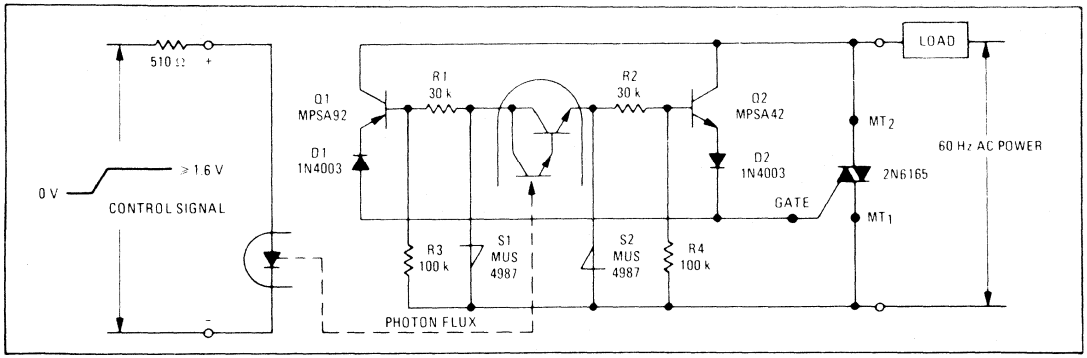


FIGURE 12 – OPTICALLY COUPLED ONE SHOT

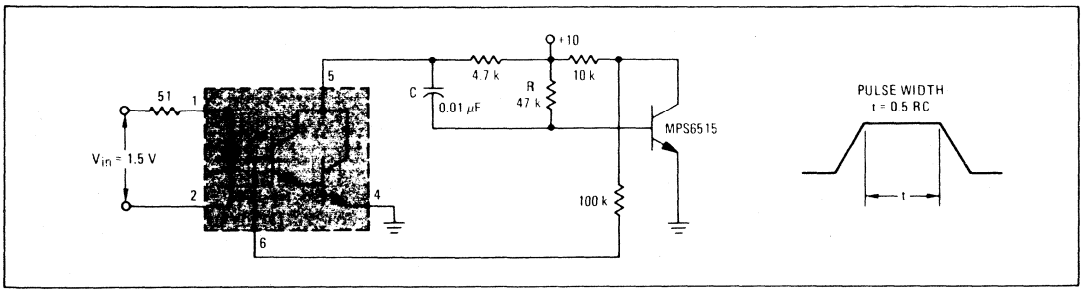
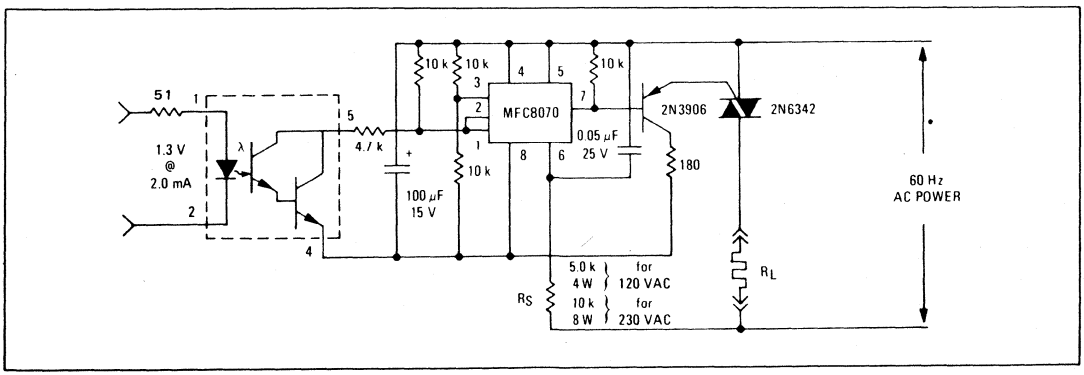


FIGURE 13 – ZERO VOLTAGE SWITCH



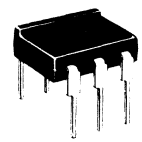
8

OPTICAL COUPLER WITH NPN TRANSISTOR OUTPUT

. . . Gallium Arsenide LED optically coupled to a Silicon Photo Transistor. Designed for applications requiring electrical isolation, high breakdown voltage and low leakage, such as Teletype Interfacing, Telephone Line pulsing and driving high voltage relays.

- High Isolation Voltage –
  V_{ISO} = 1500 V (Min) – 4N38
  = 2500 V (Min) – 4N38A
- High Collector Emitter Breakdown Voltage –
  BV_{CEO} = 80 V (Min)
- Economical Dual-In-Line Package
- 4N38A UL Recognized

INFRARED LIGHT EMITTING DIODE
PHOTOTRANSISTOR
COUPLED PAIR



***MAXIMUM RATINGS** (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INFRARED EMITTING DIODE MAXIMUM RATINGS			
Reverse Voltage	V_R	3.0	Volts
Forward Current – Continuous	I_F	80	mA
Forward Current – Peak Pulse Width = 300 μs, 2.0% Duty Cycle	I_F	3.0	Amp
Total Device Dissipation @ T_A = 25°C Negligible Power in Transistor Derate above 25°C	P_D	150 2.0	mW mW/°C
PHOTOTRANSISTOR MAXIMUM RATINGS			
Collector Emitter Voltage	V_{CEO}	80	Volts
Emitter Collector Voltage	V_{ECO}	7.0	Volts
Collector Base Voltage	V_{CBO}	80	Volts
Total Device Dissipation @ T_A = 25°C Negligible Power in Diode Derate above 25°C	P_D	150 2.0	mW mW/°C
TOTAL DEVICE RATINGS			
Total Device Dissipation @ T_A = 25°C Equal Power Dissipation in Each Element Derate above 25°C	P_D	250 3.3	mW mW/°C
Junction Temperature Range	T_J	-55 to +100	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Soldering Temperature (10 s)		260	°C

*Indicates JEDEC Registered Data.

FIGURE 1 – MAXIMUM POWER DISSIPATION

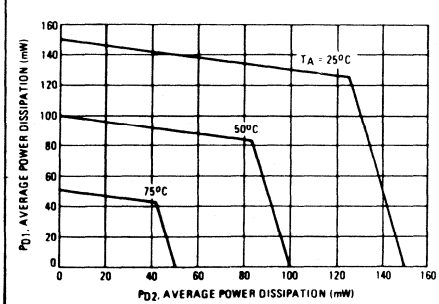


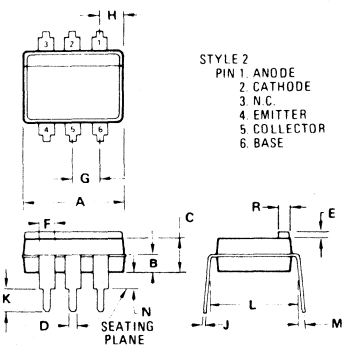
Figure 1 is based upon using limit values in the equation:

$T_{J1} - T_A = R_{\theta JA} (P_{D1} + K_\theta P_{D2})$

where:

T_{J1} Junction Temperature (100°C)
T_A Ambient Temperature
$R_{\theta JA}$ Junction to Ambient Thermal Resistance (500°C/W)
P_{D1} Power Dissipation in One Chip
P_{D2} Power Dissipation in Other Chip
K_θ Thermal Coupling Coefficient (20%)

Example:
With P_{D1} = 90 mW in the LED @ T_A = 50°C, the transistor P_D (P_{D2}) must be less than 50 mW.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.38	8.89	0.330	0.350
B	1.40	1.65	0.055	0.065
C	2.92	3.18	0.115	0.125
D	0.38	0.53	0.015	0.021
E	–	1.02	–	0.040
F	1.02	1.27	0.040	0.050
G	2.54 BSC		0.100 BSC	
H	1.57	1.83	0.062	0.072
J	0.23	0.28	0.009	0.011
K	2.92	3.30	0.115	0.130
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.27	0.020	0.050
R	–	1.90	–	0.075

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DOT OR INDEX FOR PIN NO. 1 ORIENT.

CASE 673-04

LED CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Reverse Leakage Current (V_R = 3.0 V)	I_R	–	0.05	100	μA
*Forward Voltage (I_F = 10 mA)	V_F	–	1.2	1.5	Volts
Capacitance (V_R = 0 V, f = 1.0 MHz)	C	–	150	–	pF

PHOTOTRANSISTOR CHARACTERISTICS (T_A = 25°C and I_F = 0 unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Collector-Emitter Dark Current (V_{CE} = 60 V, Base Open)	I_{CEO}	–	3.5	50	nA
*Collector-Base Dark Current (V_{CB} = 60 V, Emitter Open)	I_{CBO}	–	–	–	nA
*Collector-Base Breakdown Voltage (I_C = 100 μA, I_E = 0)	BV_{CBO}	80	–	–	Volts
*Collector-Emitter Breakdown Voltage (I_C = 1.0 mA, I_B = 0)	BV_{CEO}	80	–	–	Volts
*Emitter-Collector Breakdown Voltage (I_E = 100 μA, I_B = 0)	BV_{ECO}	7.0	–	–	Volts
DC Current Gain (V_{CE} = 5.0 V, I_C = 500 μA)	h_{FE}	–	250	–	–

COUPLED CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
*Isolation Voltage (2)		V_{ISO}				Volts
(60 Hz Peak ac)	4N38		1500	–	–	
	4N38A		2500	–	–	
(60 Hz RMS for 1 second)	4N38A		1775	–	–	
Isolation Resistance (2) (V = 500 V)		–	–	10^{11}	–	Ohms
*Collector-Emitter Saturation (I_C = 4.0 mA, I_F = 20 mA)		$V_{CE(sat)}$	–	–	1.0	Volts
Isolation Capacitance (2) (V = 0, f = 1.0 MHz)		–	–	1.3	–	pF

SWITCHING CHARACTERISTICS

Delay Time	(I_C = 10 mA, V_{CC} = 10 V)	t_d	–	0.07	–	μs
Rise Time	Figures 6 and 8	t_r	–	0.8	–	μs
Storage Time	(I_C = 10 mA, V_{CC} = 10 V)	t_s	–	4.0	–	μs
Fall Time	Figures 7 and 8	t_f	–	7.0	–	μs

*Indicates JEDEC Registered Data. (1) Pulse Test; Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.
(2) For this test LED pins 1 and 2 are common and Photo Transistor pins 4, 5 and 6 are common.

TYPICAL TRANSFER CHARACTERISTICS

FIGURE 2 – COLLECTOR-CURRENT versus DIODE FORWARD CURRENT

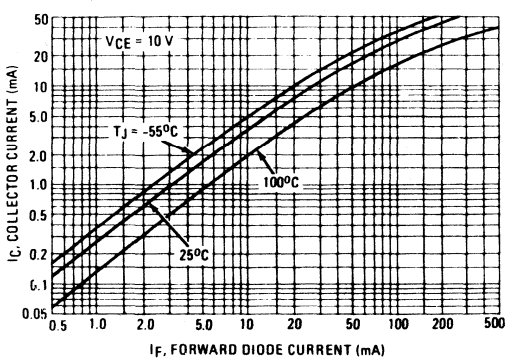
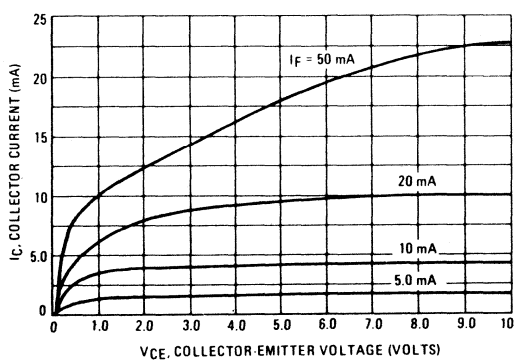


FIGURE 3 – COLLECTOR-CURRENT versus COLLECTOR-EMITTER VOLTAGE



8

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 4 – DIODE FORWARD CHARACTERISTICS

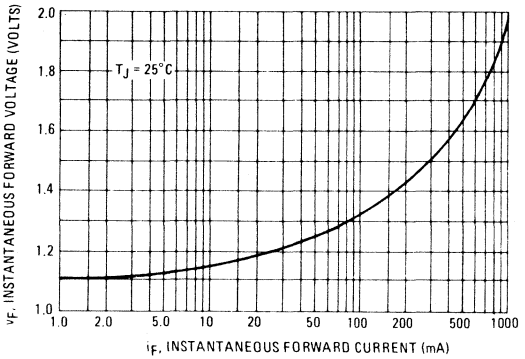


FIGURE 5 – COLLECTOR SATURATION VOLTAGE

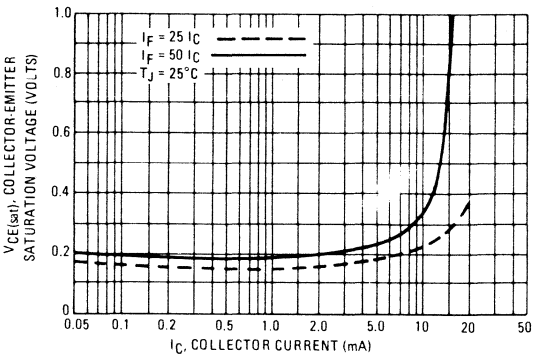


FIGURE 6 – TURN-ON TIME

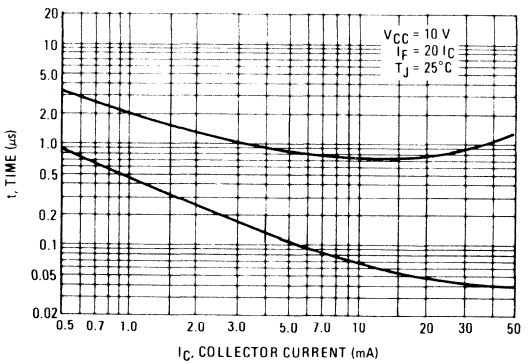


FIGURE 7 – TURN-OFF TIME

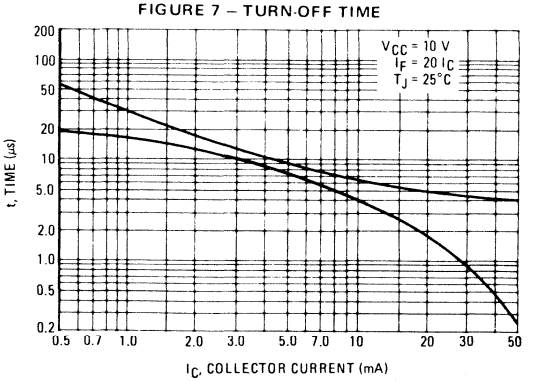


FIGURE 8 – SATURATED SWITCHING TIME TEST CIRCUIT

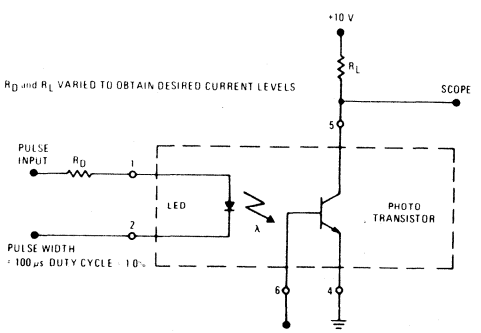
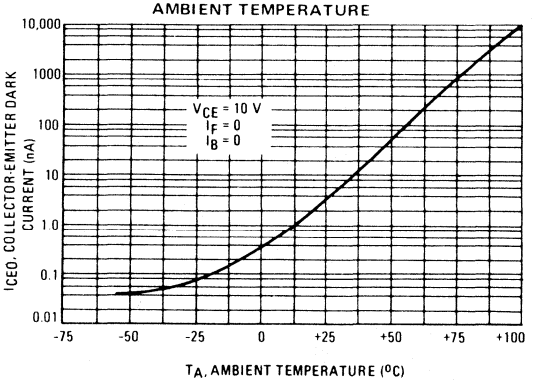


FIGURE 9 – DARK CURRENT versus AMBIENT TEMPERATURE



TYPICAL APPLICATIONS

The applications below utilize the 80 volt breakdown capability of the 4N38 and 4N38A eliminating the need for divider networks, zener diodes and the associated assembly costs.

FIGURE 10 – TYPICAL TELETYPE INTERFACE

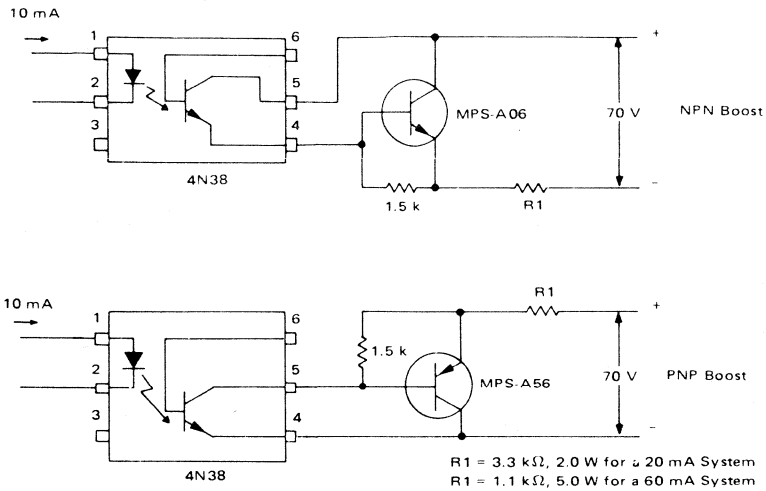


FIGURE 11 – TELEPHONE LINE PULSE CIRCUIT

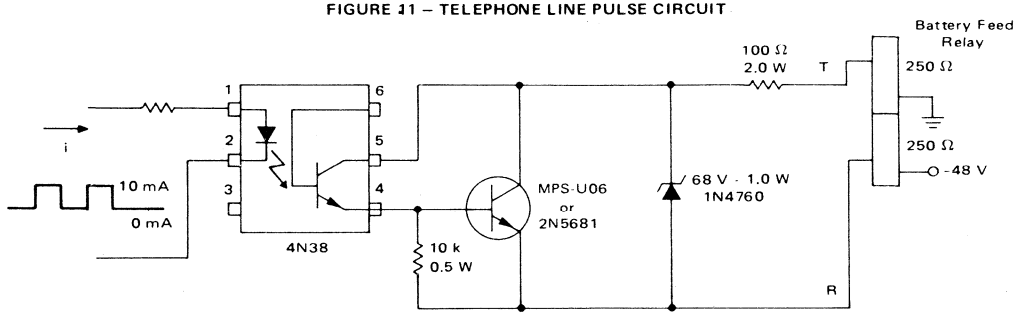
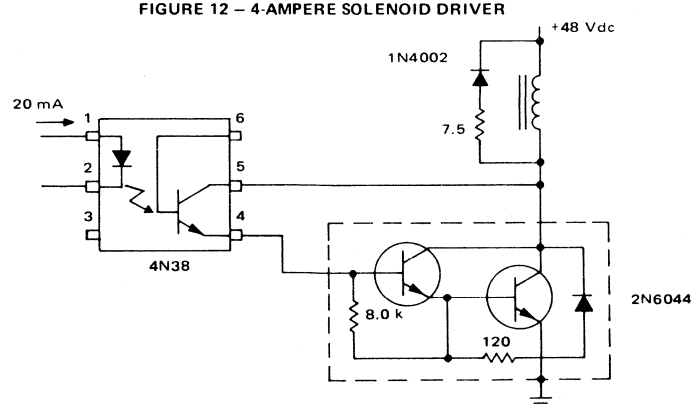


FIGURE 12 – 4-AMPERE SOLENOID DRIVER



NOTES